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# **12-Bit Binary Counter**

The MC14040B 12-stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

#### **Features**

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

| Symbol                             | Parameter   | Value                         | Unit |
|------------------------------------|---|-------------------------------|------|
| $V_{DD}$                           | DC Supply Voltage Range                           | -0.5 to +18.0                 | V    |
| V <sub>in</sub> , V <sub>out</sub> | Input or Output Voltage Range (DC or Transient)   | -0.5 to V <sub>DD</sub> + 0.5 | V    |
| I <sub>in</sub> , I <sub>out</sub> | Input or Output Current (DC or Transient) per Pin | ±10                           | mA   |
| P <sub>D</sub>                     | Power Dissipation, per Package (Note 1)           | 500                           | mW   |
| T <sub>A</sub>                     | Ambient Temperature Range                         | -55 to +125                   | °C   |
| T <sub>stg</sub>                   | Storage Temperature Range                         | -65 to +150                   | °C   |
| TL                                 | Lead Temperature<br>(8–Second Soldering)          | 260                           | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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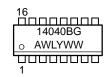


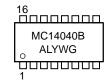
SOIC-16 D SUFFIX CASE 751B SOEIAJ-16 F SUFFIX CASE 966 TSSOP-16 DT SUFFIX CASE 948F

#### **PIN ASSIGNMENT**

| Q12 [             | 1● | 16 | V <sub>DD</sub> |
|-------------------|----|----|-----------------|
| Q6 [              | 2  | 15 | Q11             |
| Q5 [              | 3  | 14 | Q10             |
| Q7 [              | 4  | 13 | Q8              |
| Q4 [              | 5  | 12 | Q9              |
| Q3 [              | 6  | 11 | ] R             |
| Q2 [              | 7  | 10 | ] C             |
| V <sub>SS</sub> [ | 8  | 9  | Q1              |

#### **MARKING DIAGRAMS**





SOIC-16

SOEIAJ-16



= Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

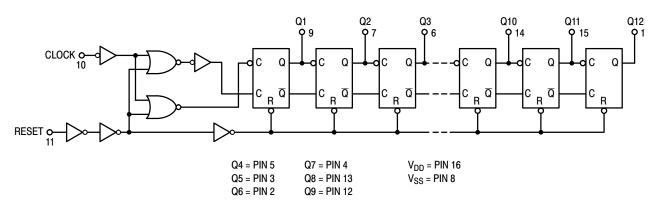
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

#### **TRUTH TABLE**

| Clock Reset |   | Output State          |
|-------------|---|-----------------------|
|             | 0 | No Change             |
| \           | 0 | Advance to next state |
| X           | 1 | All Outputs are low   |

X = Don't Care

#### **LOGIC DIAGRAM**



#### **ORDERING INFORMATION**

| Device          | Package                | Shipping <sup>†</sup>    |
|-----------------|------------------------|--------------------------|
| MC14040BDG      | SOIC-16<br>(Pb-Free)   | 48 Units / Rail          |
| NLV14040BDG*    | SOIC-16<br>(Pb-Free)   | 48 Units / Rail          |
| MC14040BDR2G    | SOIC-16<br>(Pb-Free)   | 2500 Units / Tape & Reel |
| NLV14040BDR2G*  | SOIC-16<br>(Pb-Free)   | 2500 Units / Tape & Reel |
| MC14040BDTR2G   | TSSOP-16<br>(Pb-Free)  | 2500 Units / Tape & Reel |
| NLV14040BDTR2G* | TSSOP-16<br>(Pb-Free)  | 2500 Units / Tape & Reel |
| MC14040BFELG    | SOEIAJ-16<br>(Pb-Free) | 2000 Units / Tape & Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

#### **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

|   |           |                 |                        | -55                           | 5° <b>C</b>          |                               | 25°C                                      |                      | 125                           | 5°C                  |      |
|---|-----------|-----------------|------------------------|-------------------------------|----------------------|-------------------------------|---|----------------------|-------------------------------|----------------------|------|
| Characteristic  |           | Symbol          | V <sub>DD</sub><br>Vdc | Min                           | Max                  | Min                           | Typ<br>(Note 2)                           | Max                  | Min                           | Max                  | Unit |
| Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0   | "0" Level | V <sub>OL</sub> | 5.0<br>10<br>15        | -<br>-<br>-                   | 0.05<br>0.05<br>0.05 | -<br>-<br>-                   | 0<br>0<br>0                               | 0.05<br>0.05<br>0.05 | -<br>-<br>-                   | 0.05<br>0.05<br>0.05 | Vdc  |
| V <sub>in</sub> = 0 or V <sub>DD</sub>  | "1" Level | V <sub>OH</sub> | 5.0<br>10<br>15        | 4.95<br>9.95<br>14.95         | -<br>-<br>-          | 4.95<br>9.95<br>14.95         | 5.0<br>10<br>15                           | -<br>-<br>-          | 4.95<br>9.95<br>14.95         | -<br>-<br>-          | Vdc  |
| Input Voltage<br>( $V_O = 4.5 \text{ or } 0.5 \text{ Vdc}$ )<br>( $V_O = 9.0 \text{ or } 1.0 \text{ Vdc}$ )<br>( $V_O = 13.5 \text{ or } 1.5 \text{ Vdc}$ ) | "0" Level | V <sub>IL</sub> | 5.0<br>10<br>15        | -<br>-<br>-                   | 1.5<br>3.0<br>4.0    | -<br>-<br>-                   | 2.25<br>4.50<br>6.75                      | 1.5<br>3.0<br>4.0    | -<br>-<br>-                   | 1.5<br>3.0<br>4.0    | Vdc  |
| $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$<br>$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$<br>$(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$                        | "1" Level | V <sub>IH</sub> | 5.0<br>10<br>15        | 3.5<br>7.0<br>11              |                      | 3.5<br>7.0<br>11              | 2.75<br>5.50<br>8.25                      | 1 1                  | 3.5<br>7.0<br>11              | -<br>-<br>-          | Vdc  |
| Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$                   | Source    | I <sub>OH</sub> | 5.0<br>5.0<br>10<br>15 | -3.0<br>-0.64<br>-1.6<br>-4.2 | -<br>-<br>-          | -2.4<br>-0.51<br>-1.3<br>-3.4 | -4.2<br>-0.88<br>-2.25<br>-8.8            | -<br>-<br>-          | -1.7<br>-0.36<br>-0.9<br>-2.4 | -<br>-<br>-          | mAdc |
| $(V_{OL} = 0.4 \text{ Vdc})$<br>$(V_{OL} = 0.5 \text{ Vdc})$<br>$(V_{OL} = 1.5 \text{ Vdc})$  | Sink      | I <sub>OL</sub> | 5.0<br>10<br>15        | 0.64<br>1.6<br>4.2            | -<br>-<br>-          | 0.51<br>1.3<br>3.4            | 0.88<br>2.25<br>8.8                       | -<br>-<br>-          | 0.36<br>0.9<br>2.4            | -<br>-<br>-          | mAdc |
| Input Current   |           | I <sub>in</sub> | 15                     | -                             | ±0.1                 | -                             | ±0.00001                                  | ±0.1                 | _                             | ±1.0                 | μAdc |
| Input Capacitance (V <sub>in</sub> = 0)   |           | C <sub>in</sub> | -                      | -                             | -                    | _                             | 5.0                                       | 7.5                  | -                             | -                    | pF   |
| Quiescent Current<br>(Per Package)  |           | I <sub>DD</sub> | 5.0<br>10<br>15        | -<br>-<br>-                   | 5.0<br>10<br>20      | -<br>-<br>-                   | 0.005<br>0.010<br>0.015                   | 5.0<br>10<br>20      | -<br>-<br>-                   | 150<br>300<br>600    | μAdc |
| Total Supply Current (Note (Dynamic plus Quiesce Per Package) (C <sub>L</sub> = 50 pF on all output buffers switching)                                      | nt,       | I <sub>T</sub>  | 5.0<br>10<br>15        |                               |                      | $I_{T} = (0$                  | .42 μA/kHz)<br>.85 μA/kHz)<br>.43 μA/kHz) | f + I <sub>DD</sub>  |                               |                      | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

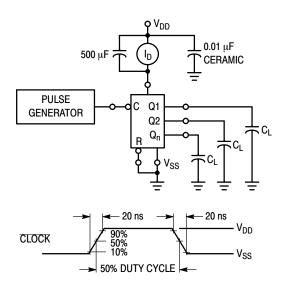
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.001.

<sup>3.</sup> The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

### **SWITCHING CHARACTERISTICS** (Note 5) ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}C$ )

| Characteristic   | Symbol                                 | V <sub>DD</sub><br>Vdc | Min               | Typ<br>(Note 6)    | Max                  | Unit |
|--|--|------------------------|-------------------|--------------------|----------------------|------|
| Output Rise and Fall Time $T_{TLH}, T_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $T_{TLH}, T_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $T_{TLH}, T_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$        | t <sub>TLH</sub> ,<br>t <sub>THL</sub> | 5.0<br>10<br>15        | -<br>-<br>-       | 100<br>50<br>40    | 200<br>100<br>80     | ns   |
| Propagation Delay Time Clock to Q1 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$ | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | 5.0<br>10<br>15        | -<br>-<br>-       | 260<br>115<br>80   | 520<br>230<br>160    | ns   |
| Clock to Q12 $t_{PHL}$ , $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 2415 ns $t_{PHL}$ , $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 867 ns $t_{PHL}$ , $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 475 ns  |  | 5.0<br>10<br>15        | -<br>-<br>-       | 1625<br>720<br>500 | 3250<br>1440<br>1000 | ns   |
| Propagation Delay Time Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 485 \text{ ns}$ $t_{PHL} = (0.86 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$                        | t <sub>PHL</sub>                       | 5.0<br>10<br>15        | -<br>-<br>-       | 370<br>155<br>115  | 740<br>310<br>230    | ns   |
| Clock Pulse Width  | t <sub>WH</sub>                        | 5.0<br>10<br>15        | 385<br>150<br>115 | 140<br>55<br>38    | -<br>-<br>-          | ns   |
| Clock Pulse Frequency  | f <sub>cl</sub>                        | 5.0<br>10<br>15        | -<br>-<br>-       | 2.1<br>7.0<br>10.0 | 1.5<br>3.5<br>4.5    | MHz  |
| Clock Rise and Fall Time   | t <sub>TLH</sub> , t <sub>THL</sub>    | 5.0<br>10<br>15        |                   | No Limit           |                      | ns   |
| Reset Pulse Width  | t <sub>WH</sub>                        | 5.0<br>10<br>15        | 960<br>360<br>270 | 320<br>120<br>80   | -<br>-<br>-          | ns   |
| Reset Removal Time   | t <sub>rem</sub>                       | 5.0<br>10<br>15        | 130<br>50<br>30   | 65<br>25<br>15     | -<br>-<br>-          | ns   |

- 5. The formulas given are for the typical characteristics only at 25°C.6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



**Figure 1. Power Dissipation Test Circuit** and Waveform

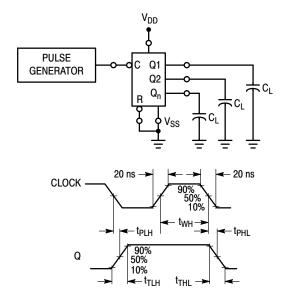


Figure 2. Switching Time Test Circuit and Waveforms

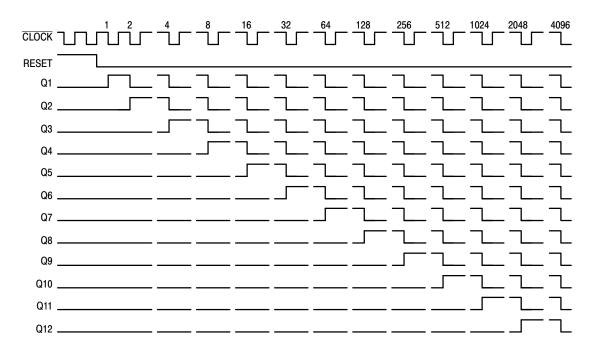


Figure 3. Timing Diagram

#### **APPLICATIONS INFORMATION**

#### **TIME-BASE GENERATOR**

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting

outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

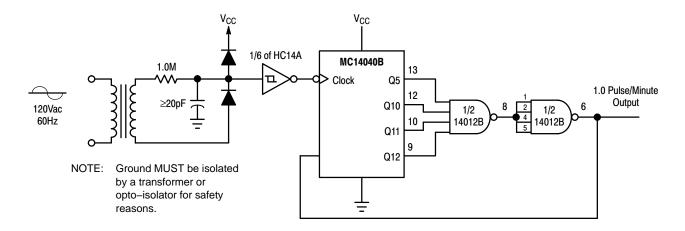
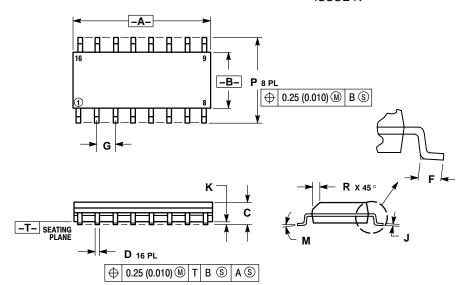


Figure 4. Time-Base Generator

#### **PACKAGE DIMENSIONS**

#### SOIC-16 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE K



- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

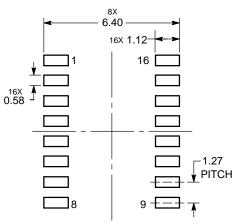
  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTEINSION.
  - PROTRUSION.

    MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- MAXIMUM MOLD PHO HUSION 0.15 (0.006) PER SIDE DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

|     | MILLIN | IETERS | INC       | HES   |
|-----|--------|--------|-----------|-------|
| DIM | MIN    | MAX    | MIN       | MAX   |
| Α   | 9.80   | 10.00  | 0.386     | 0.393 |
| В   | 3.80   | 4.00   | 0.150     | 0.157 |
| С   | 1.35   | 1.75   | 0.054     | 0.068 |
| D   | 0.35   | 0.49   | 0.014     | 0.019 |
| F   | 0.40   | 1.25   | 0.016     | 0.049 |
| G   | 1.27   | BSC    | 0.050 BSC |       |
| J   | 0.19   | 0.25   | 0.008     | 0.009 |
| K   | 0.10   | 0.25   | 0.004     | 0.009 |
| M   | 0 °    | 7°     | 0°        | 7°    |
| P   | 5.80   | 6.20   | 0.229     | 0.244 |
| R   | 0.25   | 0.50   | 0.010     | 0.019 |

#### **SOLDERING FOOTPRINT\***

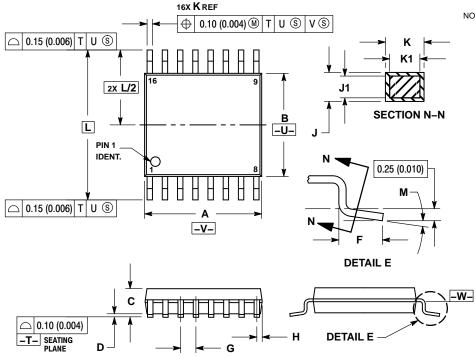


DIMENSIONS: MILLIMETERS

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### **PACKAGE DIMENSIONS**

#### TSSOP-16 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948F **ISSUE B**

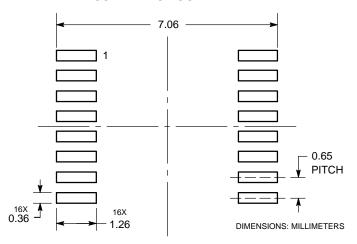


#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08
  (0.003) TOTAL IN EXCESS OF THE K
  DIMENSION AT MAXIMUM MATERIAL
  CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

|     | MILLIN   | IETERS | INC       | HES   |
|-----|----------|--------|-----------|-------|
| DIM | MIN      | MAX    | MIN       | MAX   |
| Α   | 4.90     | 5.10   | 0.193     | 0.200 |
| В   | 4.30     | 4.50   | 0.169     | 0.177 |
| C   |          | 1.20   |           | 0.047 |
| D   | 0.05     | 0.15   | 0.002     | 0.006 |
| F   | 0.50     | 0.75   | 0.020     | 0.030 |
| G   | 0.65     | BSC    | 0.026 BSC |       |
| Н   | 0.18     | 0.28   | 0.007     | 0.011 |
| L   | 0.09     | 0.20   | 0.004     | 0.008 |
| J1  | 0.09     | 0.16   | 0.004     | 0.006 |
| Κ   | 0.19     | 0.30   | 0.007     | 0.012 |
| K1  | 0.19     | 0.25   | 0.007     | 0.010 |
| L   | 6.40 BSC |        | 0.252     | BSC   |
| М   | 0°       | 8°     | 0°        | 8 °   |

#### **SOLDERING FOOTPRINT\***

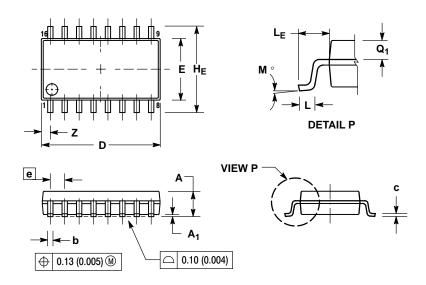


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

#### SOEIAJ-16 **F SUFFIX**

PLASTIC EIAJ SOIC PACKAGE **CASE 966 ISSUE A** 



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
- CONTROLLING DIMENSION: MILLIMETER.
- B. DIMENSIONS D AND E DO NOT INCLUDE
  MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- I. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- i. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

  DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

|                | MILLIN | IETERS | INC       | HES   |
|----------------|--------|--------|-----------|-------|
| DIM            | MIN    | MAX    | MIN       | MAX   |
| Α              |        | 2.05   |           | 0.081 |
| A <sub>1</sub> | 0.05   | 0.20   | 0.002     | 0.008 |
| b              | 0.35   | 0.50   | 0.014     | 0.020 |
| С              | 0.10   | 0.20   | 0.007     | 0.011 |
| D              | 9.90   | 10.50  | 0.390     | 0.413 |
| Е              | 5.10   | 5.45   | 0.201     | 0.215 |
| е              | 1.27   | BSC    | 0.050 BSC |       |
| HE             | 7.40   | 8.20   | 0.291     | 0.323 |
| L              | 0.50   | 0.85   | 0.020     | 0.033 |
| LE             | 1.10   | 1.50   | 0.043     | 0.059 |
| M              | 0 °    | 10 °   | 0 °       | 10°   |
| Q <sub>1</sub> | 0.70   | 0.90   | 0.028     | 0.035 |
| Z              | -      | 0.78   |           | 0.031 |

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