# Automotive Logic Gates

# NLV18VHC1Gxx, NLV18VHC1GTxx

The NLV18VHC1Gxx and NLV18VHC1GTxx are automotive−grade CMOS logic gates.

The NLV18VHC1Gxx devices have CMOS input voltage levels while the NLV18VHC1GTxx devices have TTL input voltage levels.

### Features

- High Speed: $t_{PD}$ = 7 ns (Typ) at $V_{CC}$ = 5.5 V
- Low Power Dissipation: $I_{CC}$ = 1 μA (Max) at $T_A$ = 25°C
- High Noise Immunity
- Balanced Propagation Delays ($t_{PLH} = t_{PHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL}$ = 8 mA)
- Operating Temperature: −55°C to +125°C
  AEC Grade 1−Compliant: −40°C to +125°C
- Tiny SC−88A Package (other package offerings may be available upon request)
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and RoHS Compliant

### FUNCTION LIST

| xx | Function |
|---|---|
| 00 | 2−Input NAND |
| 02 | 2−Input NOR |
| 04 | Inverter |
| 05 | Open−Drain Inverter |
| 07 | Open−Drain Buffer |
| 08 | 2−Input AND |
| 09 | 2−Input AND Gate with Open−Drain Output |
| 14 | Schmitt−Trigger Inverter |
| 17 | Schmitt−Trigger Buffer |
| 32 | 2−Input OR |
| 50 | Buffer |
| 86 | 2−Input XOR |
| 125 | Tri−State Buffer |
| 126 | Tri−State Buffer |
| 132 | 2−Input Schmitt−Trigger NAND |
| U04 | Unbuffered Inverter |

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

**ON Semiconductor®**

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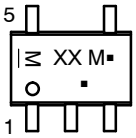
**SC−88A**
**DF SUFFIX**
**CASE 419A**

**MARKING DIAGRAM**




XX = Device Code
M = Date Code*
▪ = Pb−Free Package

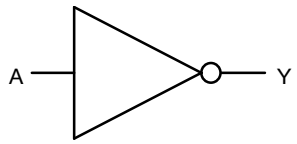
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

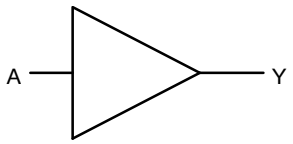
See detailed ordering and shipping information on page 11 of this data sheet.

## FUNCTIONS AND FUNCTION TABLES – BUFFERS AND INVERTERS



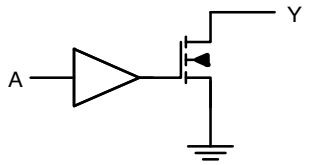

**04 – Inverter**
**U04 – Unbuffered Inverter**

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |



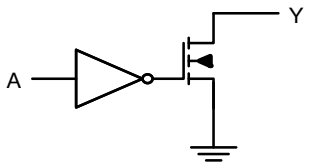

**50 – Buffer**

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |



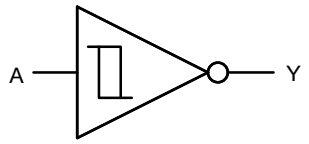

**05 – Open–Drain Inverter**

| A | Y |
|---|---|
| 0 | Hi–Z |
| 1 | 0 |



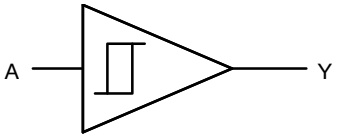

**07 – Open–Drain Buffer**

| A | Y |
|---|---|
| 0 | 0 |
| 1 | Hi–Z |




**14 – Schmitt–Trigger Inverter**

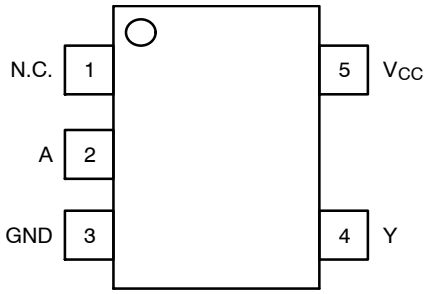
| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |




**17 – Schmitt–Trigger Buffer**

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

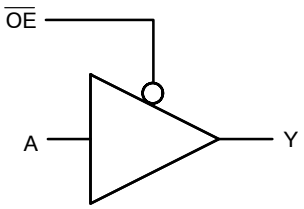
### Pin Assignment




**Pinout (Buffers and Inverters)**

| Pin | Name | Description |
|---|---|---|
| 1 | N.C. | No Connection |
| 2 | A | Input |
| 3 | GND | Ground |
| 4 | Y | Output |
| 5 | $V_{CC}$ | Supply |

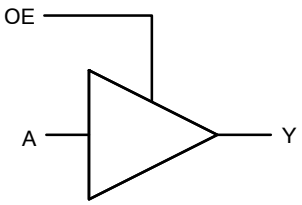
## FUNCTIONS AND FUNCTION TABLES – TRI−STATE BUFFERS AND BUS DRIVERS




**125 − Tri−State Buffer**

| $\overline{OE}$ | A | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | X | Hi−Z |

X = Don't Care

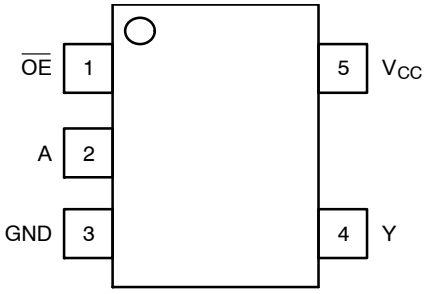



**126 − Tri−State Buffer**

| OE | A | Y |
|---|---|---|
| 0 | X | Hi−Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

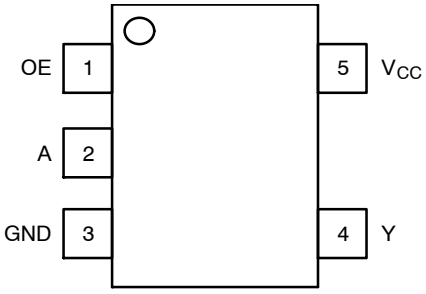
X = Don't Care

### Pin Assignments




**Pinout (125)**

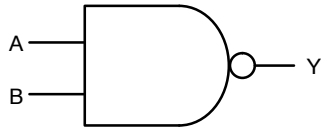
| Pin | Name | Description |
|---|---|---|
| 1 | $\overline{OE}$ | Enable (Active−Low) |
| 2 | A | Input |
| 3 | GND | Ground |
| 4 | Y | Output |
| 5 | $V_{CC}$ | Supply |




**Pinout (126)**

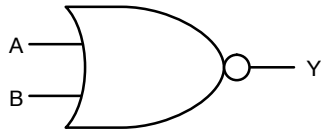
| Pin | Name | Description |
|---|---|---|
| 1 | OE | Enable (Active−High) |
| 2 | A | Input |
| 3 | GND | Ground |
| 4 | Y | Output |
| 5 | $V_{CC}$ | Supply |

## FUNCTIONS AND FUNCTION TABLES – GATES



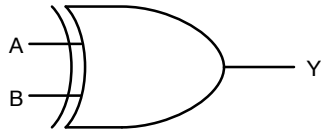

**00 – NAND**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



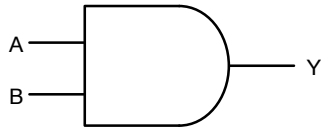

**02 – NOR**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



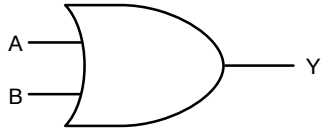

**86 – XOR**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



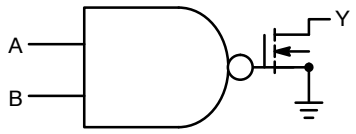

**08 – AND**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



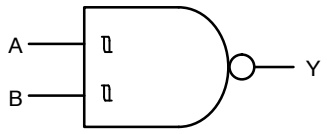

**32 – OR**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |




**09 – AND with Open–Drain Output**

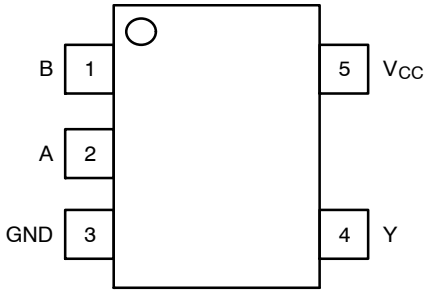
| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | Hi–Z |




**132 – NAND, Schmitt–Trigger**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Pin Assignment**




**Pinout (Gates)**

| Pin | Name | Description |
|---|---|---|
| 1 | B | Input |
| 2 | A | Input |
| 3 | GND | Ground |
| 4 | Y | Output |
| 5 | $V_{CC}$ | Supply |

**Table 1. MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +6.5 | V |
| $V_{OUT}$ | DC Output Voltage (U04) | | −0.5 to $V_{CC}$+0.5 | V |
| | DC Output Voltage (Other functions) | Active−Mode (High or Low State) | −0.5 to $V_{CC}$+0.5 | |
| | | Tri−State Mode (Note 1) | −0.5 to +6.5 | |
| | | Power−Down Mode (Vcc = 0 V) | −0.5 to +6.5 | |
| $I_{IK}$ | DC Input Diode Current | | −20 | mA |
| $I_{OK}$ | DC Output Diode Current (U04) | | ±20 | mA |
| | DC Output Diode Current (Other functions) | | −20 | |
| $I_{OUT}$ | DC Output Source/Sink Current | | ±25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC Supply Current Per Supply Pin or Ground Pin | | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | | 659 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C | | 190 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage (Note 3) | Human Body Model | 2000 | V |
| | | Charged Device Model | 1000 | |
| $I_{LATCHUP}$ | Latchup Performance (Note 4) | | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

**Table 2. RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | NLV18VHC1Gxx | 2.0 | 5.5 | V |
| | | NLV18VHC1GTxx | 4.5 | 5.5 | |
| $V_{IN}$ | Digital Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage (U04) | | 0 | $V_{CC}$ | V |
| | DC Output Voltage (Other functions) | Active−Mode (High or Low State) | 0 | $V_{CC}$ | |
| | | Tri−State Mode (Note 1) | 0 | 5.5 | |
| | | Power−Down Mode (Vcc = 0 V) | 0 | 5.5 | |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Transition Rise or Fall Rate | | | | ns/V |
| | Functions 14 and 17 | | 0 | No Limit | |
| | All Other Functions | $V_{CC}$ = 2.0 V | 0 | 20 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 20 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0 | 10 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0 | 5 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 3. DC ELECTRICAL CHARACTERISTICS (NLV18VHC1Gxx)**

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A$ = −40°C to 85°C | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **NLV18VHC1G14, NLV18VHC1G17 and NLV18VHC1G132** | | | | | | | | | | | |
| $V_{T+}$ | Positive−Going Threshold | | 2.0 | − | 1.3 | 1.5 | − | 1.5 | − | 1.5 | V |
| | | | 3.0 | − | 2.0 | 2.20 | − | 2.20 | − | 2.20 | |
| | | | 4.5 | − | 3.0 | 3.15 | − | 3.15 | − | 3.15 | |
| | | | 5.5 | − | 3.6 | 3.85 | − | 3.85 | − | 3.85 | |
| $V_{T-}$ | Negative−Going Threshold | | 2.0 | 0.5 | 0.75 | − | 0.5 | − | 0.5 | − | V |
| | | | 3.0 | 0.9 | 1.5 | − | 0.9 | − | 0.9 | − | |
| | | | 4.5 | 1.35 | 2.3 | − | 1.35 | − | 1.35 | − | |
| | | | 5.5 | 1.65 | 2.9 | − | 1.65 | − | 1.65 | − | |
| $V_H$ | Hysteresis Voltage | | 2.0 | 0.2 | 0.56 | 1.0 | 0.2 | 1.0 | 0.2 | 1.0 | V |
| | | | 3.0 | 0.3 | 0.57 | 1.2 | 0.3 | 1.2 | 0.3 | 1.2 | |
| | | | 4.5 | 0.4 | 0.67 | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | |
| | | | 5.5 | 0.5 | 0.74 | 1.6 | 0.5 | 1.6 | 0.5 | 1.6 | |
| **NLV18VHC1GU04 (Under Development)** | | | | | | | | | | | |
| $V_{IH}$ | High− Level Input Voltage | | 2.0 | 1.7 | − | − | 1.7 | − | 1.7 | − | V |
| | | | 3.0 | 2.4 | − | − | 2.4 | − | 2.4 | − | |
| | | | 4.5 | 3.6 | − | − | 3.6 | − | 3.6 | − | |
| | | | 5.5 | 4.4 | − | − | 4.4 | − | 4.4 | − | |
| $V_{IL}$ | Low− Level Input Voltage | | 2.0 | − | − | 0.3 | − | 0.3 | − | 0.3 | V |
| | | | 3.0 | − | − | 0.6 | − | 0.6 | − | 0.6 | |
| | | | 4.5 | − | − | 0.9 | − | 0.9 | − | 0.9 | |
| | | | 5.5 | − | − | 1.1 | − | 1.1 | − | 1.1 | |
| **ALL OTHER PARTS** | | | | | | | | | | | |
| $V_{IH}$ | High− Level Input Voltage | | 2.0 | 1.5 | − | − | 1.5 | − | 1.5 | − | V |
| | | | 3.0 | 2.1 | − | − | 2.1 | − | 2.1 | − | |
| | | | 4.5 | 3.15 | − | − | 3.15 | − | 3.15 | − | |
| | | | 5.5 | 3.85 | − | − | 3.85 | − | 3.85 | − | |
| $V_{IL}$ | Low− Level Input Voltage | | 2.0 | − | − | 0.5 | − | 0.5 | − | 0.5 | V |
| | | | 3.0 | − | − | 0.9 | − | 0.9 | − | 0.9 | |
| | | | 4.5 | − | − | 1.35 | − | 1.35 | − | 1.35 | |
| | | | 5.5 | − | − | 1.65 | − | 1.65 | − | 1.65 | |
| **ALL PARTS** | | | | | | | | | | | |
| $V_{OH}$ (Note 5) | High− Level Output Voltage | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T-}$) $I_{OH}$ = −50 μA | 2.0 | 1.9 | 2.0 | − | 1.9 | − | 1.9 | − | V |
| | | | 3.0 | 2.9 | 3.0 | − | 2.9 | − | 2.9 | − | |
| | | | 4.5 | 4.4 | 4.5 | − | 4.4 | − | 4.4 | − | |
| | | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T-}$) | | | | | | | | | |
| | | $I_{OH}$ = −4 mA | 3.0 | 2.58 | − | − | 2.48 | − | 2.34 | − | |
| | | $I_{OH}$ = −8 mA | 4.5 | 3.94 | − | − | 3.8 | − | 3.66 | − | |

**Table 3. DC ELECTRICAL CHARACTERISTICS (NLV18VHC1Gxx)**

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A$ = −40°C to 85°C | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **ALL PARTS** | | | | | | | | | | | |
| $V_{OL}$ | Low− Level Output Voltage | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T−}$) $I_{OL}$ = 50 μA | 2.0 | − | 0.0 | 0.1 | − | 0.1 | − | 0.1 | V |
| | | | 3.0 | − | 0.0 | 0.1 | − | 0.1 | − | 0.1 | |
| | | | 4.5 | − | 0.0 | 0.1 | − | 0.1 | − | 0.1 | |
| | | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T−}$) $I_{OL}$ = 4 mA $I_{OL}$ = 8 mA | | | | | | | | | |
| | | | 3.0 | − | − | 0.36 | − | 0.44 | − | 0.52 | |
| | | | 4.5 | − | − | 0.36 | − | 0.44 | − | 0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 5.5 | − | − | ±0.1 | − | ±1.0 | − | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | − | − | 1.0 | − | 20 | − | 40 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The $V_{OH}$ parameter does not apply to devices with open−drain output, NLV18VHC1G05, NLV18VHC1G07, NLV18VHC1GT05 and NLV18VHC1GT07.

**Table 4. DC ELECTRICAL CHARACTERISTICS (NLV18VHC1GTxx)**

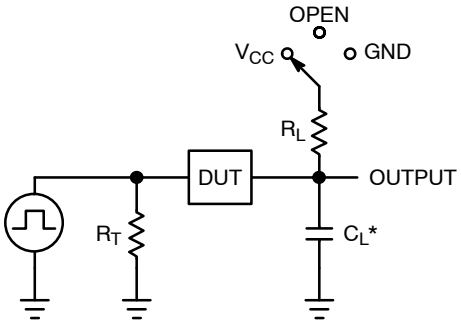
| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25 °C | | | $T_A$ = −40°C to 85°C | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **NLV18VHC1GT14 and NLV18VHC1GT17** | | | | | | | | | | | |
| $V_{T+}$ | Positive−Going Threshold | | 4.5 | − | 1.74 | 2.0 | − | 2.0 | − | 2.0 | V |
| | | | 5.5 | − | 1.94 | 2.1 | − | 2.1 | − | 2.1 | |
| $V_{T−}$ | Negative−Going Threshold | | 4.5 | 0.5 | 1.01 | − | 0.5 | − | 0.5 | − | V |
| | | | 5.5 | 0.6 | 1.13 | − | 0.6 | − | 0.6 | − | |
| $V_H$ | Hysteresis Voltage | | 4.5 | 0.4 | 0.73 | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | V |
| | | | 5.5 | 0.5 | 0.81 | 1.6 | 0.5 | 1.6 | 0.5 | 1.6 | |
| **ALL OTHER PARTS** | | | | | | | | | | | |
| $V_{IH}$ | High− Level Input Voltage | | 4.5 − 5.5 | 2.0 | − | − | 2.0 | − | 2.0 | − | V |
| $V_{IL}$ | Low− Level Input Voltage | | 4.5 − 5.5 | − | − | 0.8 | − | 0.8 | − | 0.8 | V |
| **ALL PARTS** | | | | | | | | | | | |
| $V_{OH}$ (Note 4) | High− Level Output Voltage | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T−}$) | | | | | | | | | V |
| | | $I_{OH}$ = −50 μA | 4.5 | 4.4 | 4.5 | − | 4.4 | − | 4.4 | − | |
| | | $I_{OH}$ = −8 mA | 4.5 | 3.94 | − | − | 3.80 | − | 3.66 | − | |
| $V_{OL}$ | Low− Level Output Voltage | $V_{IN}$ = $V_{IH}$ ($V_{T+}$) or $V_{IL}$ ($V_{T−}$) | | | | | | | | | V |
| | | $I_{OL}$ = 50 μA | 4.5 | − | 0.0 | 0.1 | − | 0.1 | − | 0.1 | |
| | | $I_{OL}$ = 8 mA | 4.5 | − | − | 0.36 | − | 0.44 | − | 0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | − | − | ±0.1 | − | ±1.0 | − | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND; $I_O$ = 0 A | 5.5 | − | − | 1.0 | − | 20 | − | 40 | μA |
| $\Delta I_{CC}$ | Additional Supply Current per Input | $V_{IN}$ = 3.4 V; $I_O$ = 0 A; Other input at $V_{CC}$ or GND | 5.5 | − | − | 1.35 | − | 1.5 | − | 1.65 | mA |

**Table 5. AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ | | | $-40°C \le T_A \le 85°C$ | | $-55°C \le T_A \le 125°C$ | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, A to Y (Figures 1 and 2) | $C_L$ = 15 pF | 3.0 to 3.6 | – | 7.0 | 12.8 | – | 15.0 | – | 17.0 | ns |
| | | $C_L$ = 50 pF | | – | 8.5 | 16.3 | – | 18.5 | – | 20.5 | |
| | | $C_L$ = 15 pF | 4.5 to 5.5 | – | 4.0 | 8.6 | – | 10.0 | – | 11.5 | |
| | | $C_L$ = 50 pF | | – | 5.5 | 10.6 | – | 12.0 | – | 13.5 | |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time, (A or $\overline{OE}$ or OE) to Y (Figures 1 and 2) | $C_L$ = 15 pF | 3.0 to 3.6 | – | 4.5 | 8.0 | – | 9.5 | – | 11.5 | ns |
| | | $C_L$ = 50 pF | | – | 6.4 | 11.5 | – | 13.0 | – | 15.0 | |
| | | $C_L$ = 15 pF | 4.5 to 5.5 | – | 3.5 | 5.1 | – | 6.0 | – | 8.5 | |
| | | $C_L$ = 50 pF | | – | 4.5 | 7.1 | – | 8.0 | – | 10.5 | |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time, (A or $\overline{OE}$ or OE) to Y (Figures 1 and 2) | $C_L$ = 15 pF | 3.0 to 3.6 | – | 6.5 | 9.7 | – | 11.5 | – | 14.5 | ns |
| | | $C_L$ = 50 pF | | – | 8.0 | 13.2 | – | 15.0 | – | 18.0 | |
| | | $C_L$ = 15 pF | 4.5 to 5.5 | – | 4.8 | 6.8 | – | 8.0 | – | 10.0 | |
| | | $C_L$ = 50 pF | | – | 7.0 | 8.8 | – | 10.0 | – | 12.0 | |
| $C_{IN}$ | Input Capacitance | | | – | 4.0 | 10 | – | 10 | – | 10 | pF |
| $C_{OUT}$ | Output Capacitance | Output in High Impedance State | | – | 6.0 | – | – | – | – | – | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | 8.0 | pF |

6. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.




$C_L$ includes probe and jig capacitance
$R_T$ is $Z_{OUT}$ of pulse generator (typically 50 Ω)
f = 1 MHz

| Test | Switch Position | $C_L$, pF | $R_L$, Ω |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Characteristics Table | X |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | 1 k |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | 1 k |

X = Don't Care

**Figure 1. Test Circuit**

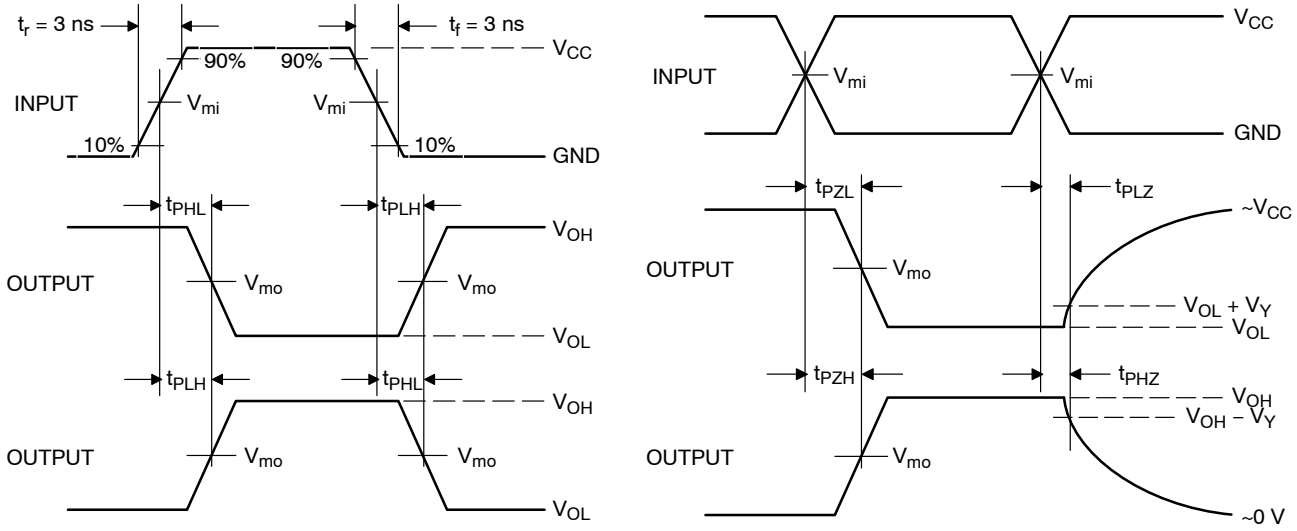



**Figure 2. Switching Waveforms**

| $V_{CC}$, V | $V_{mi}$, V | $V_{mo}$, V | | $V_Y$, V |
|---|---|---|---|---|
| | | $t_{PLH}$, $t_{PHL}$ | $t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$ | |
| 3.0 to 3.6 | $V_{CC}/2$ | $(V_{OH} - V_{OL})/2$ | $V_{CC}/2$ | 0.3 |
| 4.5 to 5.5 | $V_{CC}/2$ | $(V_{OH} - V_{OL})/2$ | $V_{CC}/2$ | 0.3 |

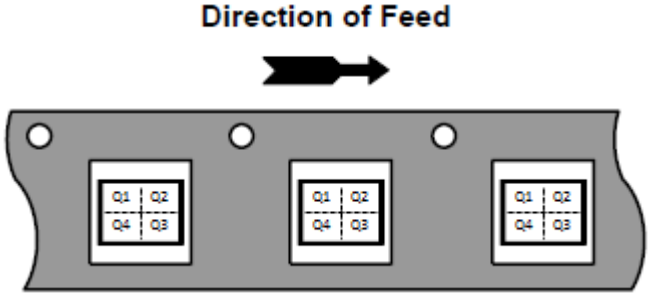
## ORDERING INFORMATION

| Device | Package | Marking | Pin 1 Orientation (See below) | Shipping† |
|---|---|---|---|---|
| NLV18VHC1G00DFT2G | SC−88A | V1 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G02DFT2G | SC−88A | V3 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G04DFT2G | SC−88A | V5 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G05DFT2G (in development) | SC−88A | VF | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G07DFT2G (in development) | SC−88A | V7 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G08DFT2G | SC−88A | V2 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G09DFT2G | SC−88A | VX | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G14DFT2G | SC−88A | VA | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G17DFT2G (in development) | SC−88A | TBD | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G32DFT2G | SC−88A | V4 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G32DFT1G | SC−88A | V4 | Q2 | 3000 / Tape & Reel |
| NLV18VHC1G50DFT2G (in development) | SC−88A | VR | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G86DFT2G (in development) | SC−88A | V8 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G125DFT2G | SC−88A | W0 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G126DFT2G (in development) | SC−88A | W2 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1G132DFT2G | SC−88A | VD | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GU04DFT2G (in development) | SC−88A | V6 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT00DFT2G (in development) | SC−88A | VH | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT02DFT2G (in development) | SC−88A | VJ | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT04DFT2G | SC−88A | VK | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT05DFT2G (in development) | SC−88A | TBD | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT07DFT2G (in development) | SC−88A | TBD | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT08DFT2G | SC−88A | VT | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT14DFT2G (in development) | SC−88A | VC | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT17DFT2G (in development) | SC−88A | TBD | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT32DFT2G (in development) | SC−88A | VN | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT50DFT2G (in development) | SC−88A | VL | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT86DFT2G (in development) | SC−88A | VM | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT125DFT2G | SC−88A | W1 | Q4 | 3000 / Tape & Reel |
| NLV18VHC1GT126DFT2G (in development) | SC−88A | W3 | Q4 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

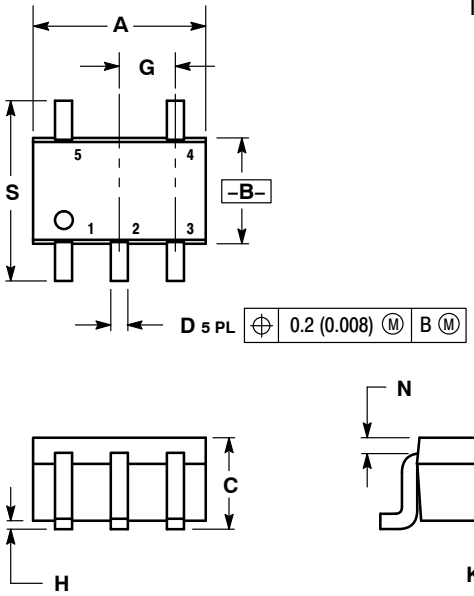
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel



## PACKAGE DIMENSIONS

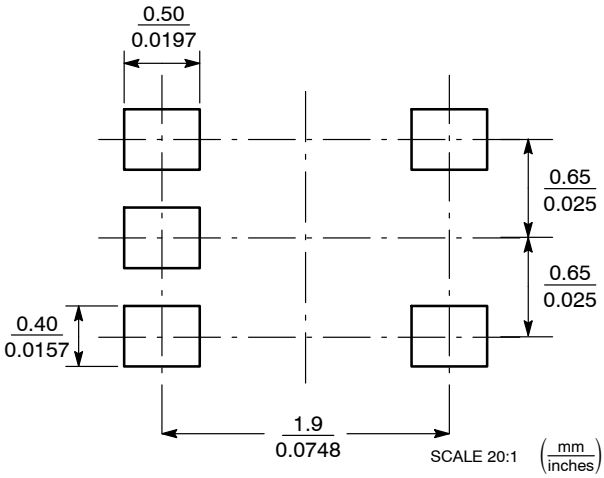
**SC−88A (SC−70−5/SOT−353)**
CASE 419A−02
ISSUE L




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

## SOLDER FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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