MC74HC14A

Hex Schmitt-Trigger Inverter

High–Performance Silicon–Gate CMOS

The MC74HC14A is identical in pinout to the LS14, LS04 and the HC04. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC14A is useful to "square up" slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 60 FETs or 15 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
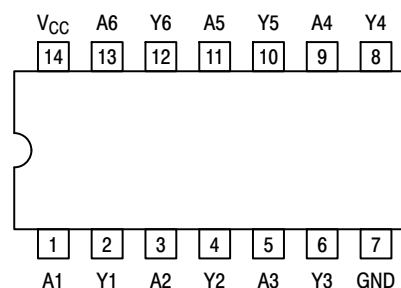- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

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http://onsemi.com
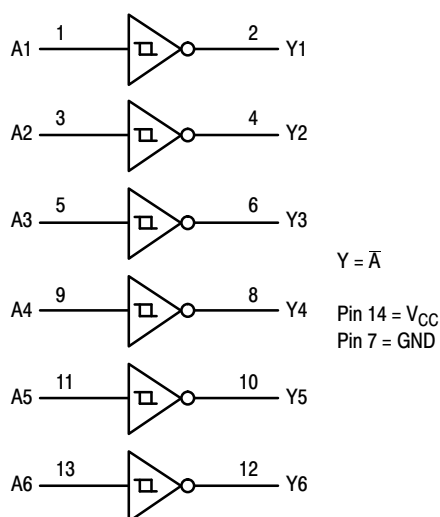
SOIC–14 NB
D SUFFIX
CASE 751A

TSSOP–14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

14–Lead (Top View)

LOGIC DIAGRAM

$Y = \overline{A}$

Pin 14 = V_{CC}
Pin 7 = GND

MARKING DIAGRAMS
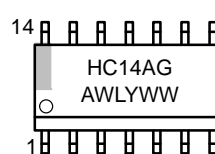
SOIC–14 NB
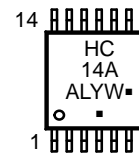
TSSOP–14

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb–Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
A	**Y**
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74HC14A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: −7 mW/°C from 65° to 125°C
           TSSOP Package: −6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		−55	+125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	No Limit* No Limit* No Limit*	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*When V_{in} = 50% V_{CC}, I_{CC} > 1mA

MC74HC14A

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V$_{CC}$ V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V$_{T+}$ max	Maximum Positive–Going Input Threshold Voltage (Figure 3)	V$_{out}$ = 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V$_{T+}$ min	Minimum Positive–Going Input Threshold Voltage (Figure 3)	V$_{out}$ = 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V$_{T-}$ max	Maximum Negative–Going Input Threshold Voltage (Figure 3)	V$_{out}$ = V$_{CC}$ − 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V$_{T-}$ min	Minimum Negative–Going Input Threshold Voltage (Figure 3)	V$_{out}$ = V$_{CC}$ − 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
V$_H$max (Note 1)	Maximum Hysteresis Voltage (Figure 3)	V$_{out}$ = 0.1V or V$_{CC}$ − 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
V$_H$min (Note 1)	Minimum Hysteresis Voltage (Figure 3)	V$_{out}$ = 0.1V or V$_{CC}$ − 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V$_{OH}$	Minimum High–Level Output Voltage	V$_{in} \leq$ V$_{T-}$ min $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V$_{in} \leq$ V$_{T-}$ min $\qquad \|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V$_{OL}$	Maximum Low–Level Output Voltage	V$_{in} \geq$ V$_{T+}$ max $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V$_{in} \geq$ V$_{T+}$ max $\qquad \|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I$_{in}$	Maximum Input Leakage Current	V$_{in}$ = V$_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I$_{CC}$	Maximum Quiescent Supply Current (per Package)	V$_{in}$ = V$_{CC}$ or GND I$_{out}$ = 0μA	6.0	1.0	10	40	μA

1. V$_H$min > (V$_{T+}$ min) − (V$_{T-}$ max); V$_H$max = (V$_{T+}$ max) − (V$_{T-}$ min).

AC CHARACTERISTICS (C$_L$ = 50pF, Input t$_r$ = t$_f$ = 6ns)

Symbol	Parameter	V$_{CC}$ V	Guaranteed Limit −55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t$_{TLH}$, t$_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C$_{in}$	Maximum Input Capacitance		10	10	10	pF
C$_{PD}$	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, V$_{CC}$ = 5.0 V 22			pF

* Used to determine the no–load dynamic power consumption: P$_D$ = C$_{PD}$ V$_{CC}^2$f + I$_{CC}$ V$_{CC}$.
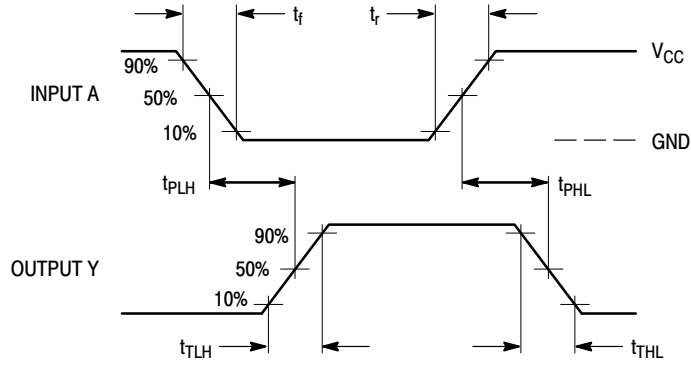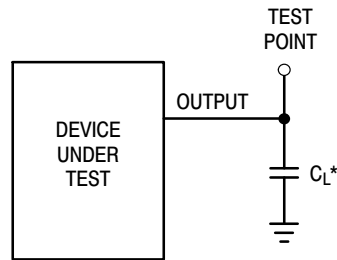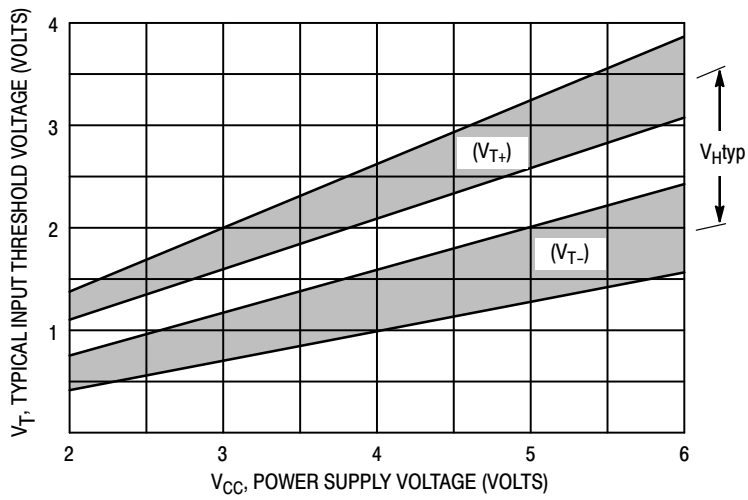
MC74HC14A

Figure 1. Switching Waveforms

*Includes all probe and jig capacitance
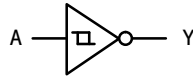
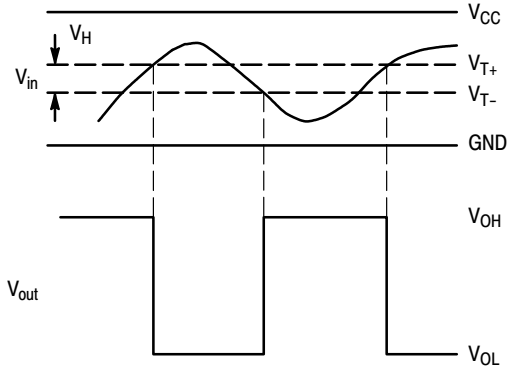**Figure 2. Test Circuit**

$V_H typ = (V_{T+} typ) - (V_{T-} typ)$

Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

MC74HC14A

(a) A Schmitt−Trigger Squares Up Inputs With Slow Rise and Fall Times

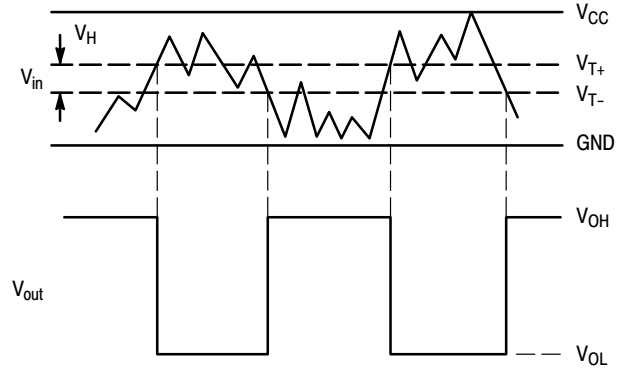(b) A Schmitt−Trigger Offers Maximum Noise Immunity

Figure 4. Typical Schmitt−Trigger Applications

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74HC14ADG	SOIC−14 NB (Pb−Free)	55 Units / Rail
MC74HC14ADR2G	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
MC74HC14ADTG	TSSOP−14 (Pb−Free)	96 Units / Rail
MC74HC14ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLV74HC14ADG*	SOIC−14 NB (Pb−Free)	55 Units / Rail
NLV74HC14ADR2G*	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
NLV74HC14ADTG*	TSSOP−14 (Pb−Free)	96 Units / Rail
NLV74HC14ADTR2G*	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14

1

SCALE 1:1

DETAIL A

A3

L

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

D

A
B

14

8

H

E

1

7

⊕ 0.25 Ⓜ B Ⓜ

13X b

⊕ 0.25 Ⓜ C A Ⓢ B Ⓢ

A

⬠ 0.10

A1

e

C SEATING PLANE

h
X 45°

DETAIL A

M

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*

6.50

14X
1.18

1

1.27
PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

STYLE 1:
PIN 1. COMMON CATHODE
  2. ANODE/CATHODE
  3. ANODE/CATHODE
  4. NO CONNECTION
  5. ANODE/CATHODE
  6. NO CONNECTION
  7. ANODE/CATHODE
  8. ANODE/CATHODE
  9. ANODE/CATHODE
  10. NO CONNECTION
  11. ANODE/CATHODE
  12. ANODE/CATHODE
  13. NO CONNECTION
  14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
  2. ANODE
  3. ANODE
  4. NO CONNECTION
  5. ANODE
  6. NO CONNECTION
  7. ANODE
  8. ANODE
  9. ANODE
  10. NO CONNECTION
  11. ANODE
  12. ANODE
  13. NO CONNECTION
  14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
  2. CATHODE
  3. CATHODE
  4. NO CONNECTION
  5. CATHODE
  6. NO CONNECTION
  7. CATHODE
  8. CATHODE
  9. CATHODE
  10. NO CONNECTION
  11. CATHODE
  12. CATHODE
  13. NO CONNECTION
  14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
  2. ANODE/CATHODE
  3. ANODE/CATHODE
  4. ANODE/CATHODE
  5. ANODE/CATHODE
  6. NO CONNECTION
  7. COMMON ANODE
  8. COMMON CATHODE
  9. ANODE/CATHODE
  10. ANODE/CATHODE
  11. ANODE/CATHODE
  12. ANODE/CATHODE
  13. NO CONNECTION
  14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
  2. CATHODE
  3. CATHODE
  4. CATHODE
  5. CATHODE
  6. CATHODE
  7. CATHODE
  8. ANODE
  9. ANODE
  10. ANODE
  11. ANODE
  12. ANODE
  13. ANODE
  14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
  2. COMMON ANODE
  3. COMMON CATHODE
  4. ANODE/CATHODE
  5. ANODE/CATHODE
  6. ANODE/CATHODE
  7. ANODE/CATHODE
  8. ANODE/CATHODE
  9. ANODE/CATHODE
  10. ANODE/CATHODE
  11. COMMON CATHODE
  12. COMMON ANODE
  13. ANODE/CATHODE
  14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
  2. ANODE/CATHODE
  3. ANODE/CATHODE
  4. NO CONNECTION
  5. ANODE/CATHODE
  6. ANODE/CATHODE
  7. COMMON ANODE
  8. COMMON ANODE
  9. ANODE/CATHODE
  10. ANODE/CATHODE
  11. NO CONNECTION
  12. ANODE/CATHODE
  13. ANODE/CATHODE
  14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

◢ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

PIN 1 IDENT.

14   8

1   7

B
−U−

◢ | 0.15 (0.006) | T | U Ⓢ

A
−V−

N

0.25 (0.010)

M

N

F

DETAIL E

K
K1

J J1

SECTION N−N

C

◢ | 0.10 (0.004)
−T− SEATING PLANE

D   **G**   **H**

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**GENERIC
MARKING DIAGRAM***

14

XXXX
XXXX
ALYW■

1

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**TSSOP−14 WB**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊

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74HC85N NLU1G32AMUTCG NLV7SZ58DFT2G CD4068BE NL17SG32P5T5G NL17SG86DFT2G NLV14001UBDR2G NLX1G11AMUTCG NLX1G97MUTCG 74LS38 74LVC32ADTR2G MC74HCT20ADTR2G NLV17SZ00DFT2G NLV17SZ02DFT2G NLV74HC02ADR2G 74HC32S14-13 74LS133 74LVC1G32Z-7 M38510/30402BDA 74LVC1G86Z-7 74LVC2G08RA3-7 NLV74HC08ADTR2G NLV74HC14ADR2G NLV74HC20ADR2G NLX2G86MUTCG 5962-8973601DA 74LVC2G02HD4-7 NLU1G00AMUTCG 74LVC2G32RA3-7 74LVC2G00HD4-7 NL17SG02P5T5G 74LVC2G00HK3-7 74LVC2G86HK3-7 NLX1G99DMUTWG NLVVHC1G00DFT2G NLVHC1G08DFT2G NLV7SZ57DFT2G NLV74VHC04DTR2G NLV27WZ86USG NLV27WZ00USG NLU1G86CMUTCG NLU1G08CMUTCG NL17SZ32P5T5G NL17SZ00P5T5G NL17SH02P5T5G 74AUP2G00RA3-7 NLV74HC02ADTR2G NLX1G332CMUTCG NL17SG86P5T5G NL17SZ05P5T5G