# MC74HCT366A

## Hex 3-State Inverting Buffer with Common Enables and LSTTL Compatible Inputs

### High−Performance Silicon−Gate CMOS

The MC74HCT366A is identical in pinout to the LS366. The device inputs are compatible with standard CMOS or LSTTL outputs.

This device is a high−speed hex buffer with 3−state outputs and two common active−low Output Enables. When either of the enables is high, the buffer outputs are placed into high−impedance states. The HCT366A has inverting outputs.

### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
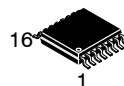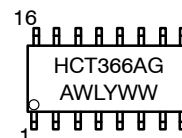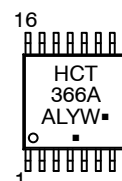- These are Pb−Free Devices*

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**MARKING DIAGRAMS**
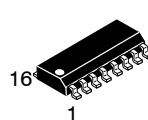


SOIC−16
D SUFFIX
CASE 751B

```
HCT366AG
AWLYWW
```



TSSOP−16
DT SUFFIX
CASE 948F

```
HCT
366A
ALYW■
```

A       = Assembly Location
WL, L   = Wafer Lot
Y       = Year
WW, W   = Work Week
G or ■  = Pb−Free Package
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
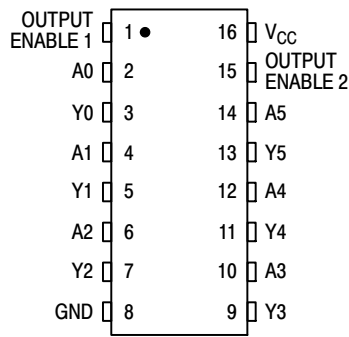
# MC74HCT366A



**Figure 1. Pin Assignment**

## FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Enable 1 | Enable 2 | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

X = don't care
Z = high impedance
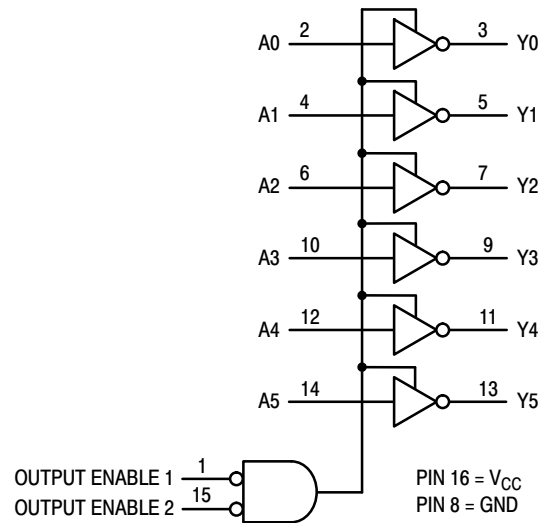


**Figure 2. Logic Diagram**

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| MC74HCT366ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HCT366ADR2G | | 2500 Units / Reel |
| MC74HCT366ADTR2G | TSSOP−16 (Pb−Free) | 2500 Units / Reel |
| NLVHCT366ADTRG* | | 2500 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MC74HCT366A

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | − 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air,     SOIC Package† <br> TSSOP Package† | 500 <br> 450 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: − 7 mW/°C from 65° to 125°C
                TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|--------|-----------|--|-----|-----|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time <br> (Figure 1) | $V_{CC}$ = 2.0 V <br> $V_{CC}$ = 3.0 V <br> $V_{CC}$ = 4.5 V <br> $V_{CC}$ = 6.0 V | 0 <br> 0 <br> 0 <br> 0 | 1000 <br> 600 <br> 500 <br> 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|--------|-----------|-----------------|--|-----------|------------------|--|--|------|
| | | | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = $V_{CC}$ − 0.1 V <br> $|I_{out}|$ ≤ 20 µA | | 4.5 to 5.5 | 2.0 | 2.0 | 2.0 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1 V <br> $|I_{out}|$ ≤ 20 µA | | 4.5 to 5.5 | 0.80 | 0.80 | 0.80 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ <br> $|I_{out}|$ ≤ 20 µA | | 2.0 <br> 4.5 <br> 6.0 | 1.9 <br> 4.4 <br> 5.9 | 1.9 <br> 4.4 <br> 5.9 | 1.9 <br> 4.4 <br> 5.9 | V |
| | | $V_{in}$ = $V_{IH}$ | $|I_{out}|$ ≤ 3.6 mA <br> $|I_{out}|$ ≤ 6.0 mA <br> $|I_{out}|$ ≤ 7.8 mA | 3.0 <br> 4.5 <br> 6.0 | 2.48 <br> 3.98 <br> 5.48 | 2.34 <br> 3.84 <br> 5.34 | 2.20 <br> 3.70 <br> 5.20 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IL}$ <br> $|I_{out}|$ ≤ 20 µA | | 2.0 <br> 4.5 <br> 6.0 | 0.1 <br> 0.1 <br> 0.1 | 0.1 <br> 0.1 <br> 0.1 | 0.1 <br> 0.1 <br> 0.1 | V |
| | | $V_{in}$ = $V_{IL}$ | $|I_{out}|$ ≤ 3.6 mA <br> $|I_{out}|$ ≤ 6.0 mA <br> $|I_{out}|$ ≤ 7.8 mA | 3.0 <br> 4.5 <br> 6.0 | 0.26 <br> 0.26 <br> 0.26 | 0.33 <br> 0.33 <br> 0.33 | 0.40 <br> 0.40 <br> 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | µA |

# MC74HCT366A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|--------|-----------|-----------------|---------|--------------------|--------------|---------------|------|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $I_{OZ}$ | Maximum Three–State Leakage Current | Output in High–Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND | 6.0 | ± 0.5 | ± 5.0 | ± 10 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND $I_{out} = 0$ µA | 6.0 | 4 | 40 | 160 | µA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|--------|-----------|---------|------------------|--------|---------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3) | 2.0 3.0 4.5 6.0 | 120 60 24 20 | 150 75 30 26 | 180 90 36 31 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 220 110 44 37 | 275 140 55 47 | 330 170 66 56 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 220 110 44 37 | 275 140 55 47 | 330 170 66 56 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 3.0 4.5 6.0 | 60 22 12 10 | 75 28 15 13 | 90 34 18 15 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three–State Output Capacitance (Output in High–Impedance State) | — | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|--------|-----------|-----------------------------------|------|
| $C_{PD}$ | Power Dissipation Capacitance (Per Buffer)* | 60 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

# MC74HCT366A
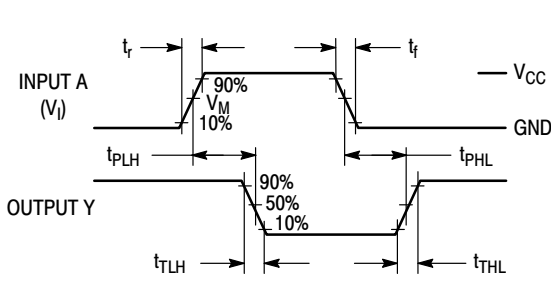
## SWITCHING WAVEFORMS
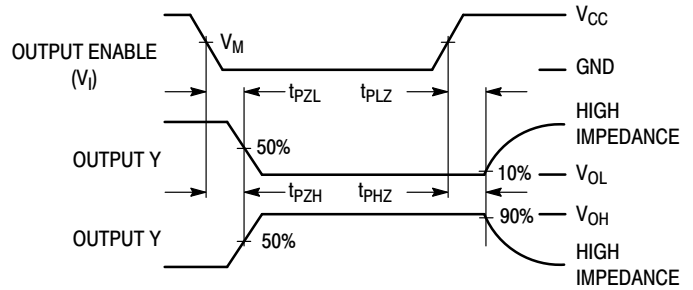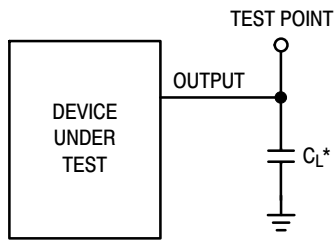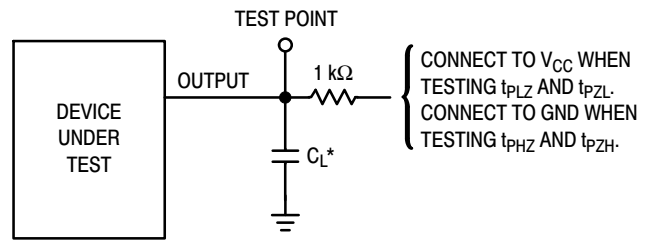
($V_I$ = 0 to 3 V, $V_M$ = 1.3 V)



**Figure 1.**



**Figure 2.**
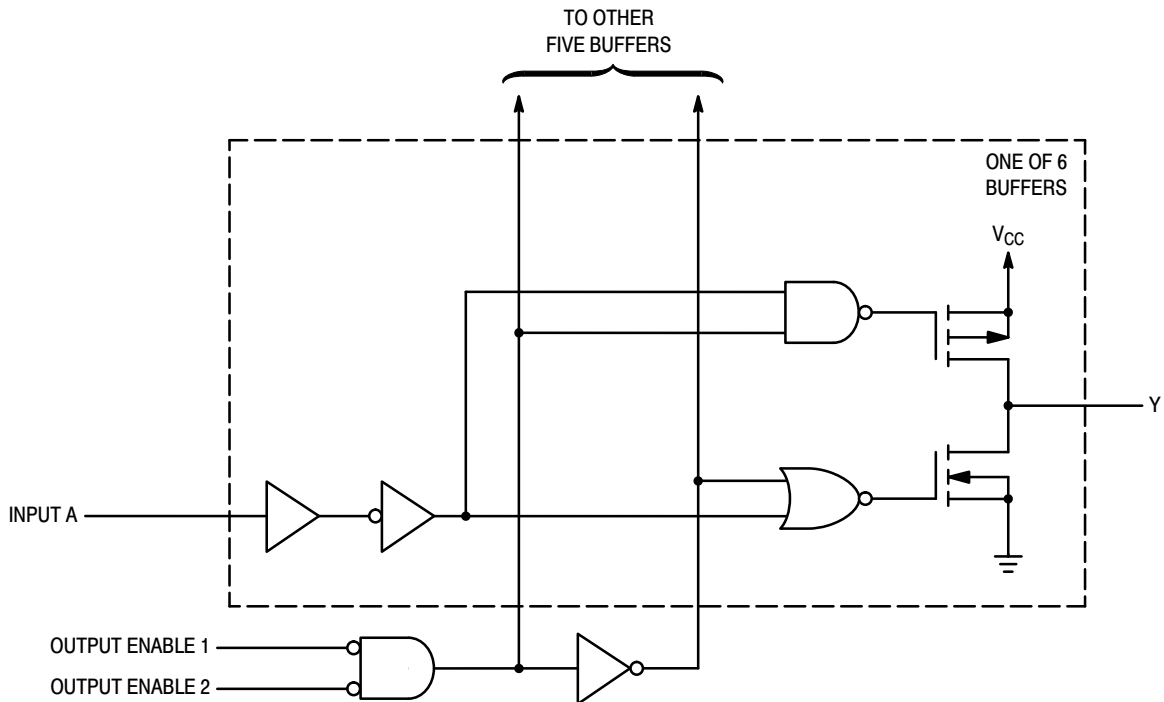
## TEST CIRCUITS



*Includes all probe and jig capacitance

**Figure 3.**



CONNECT TO $V_{CC}$ WHEN TESTING $t_{PLZ}$ AND $t_{PZL}$.
CONNECT TO GND WHEN TESTING $t_{PHZ}$ AND $t_{PZH}$.

*Includes all probe and jig capacitance

**Figure 4.**

## LOGIC DETAIL

**ON Semiconductor®**

**SCALE 1:1**

**SOIC−16**
CASE 751B−05
ISSUE K

DATE 29 DEC 2006

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ 0.25 (0.010) Ⓜ B Ⓢ

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH

DIMENSIONS: MILLIMETERS

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | SOIC−16 | | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**ON Semiconductor®**

**TSSOP−16**
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

16

1

**SCALE 2:1**

**16X K** REF

$\oplus$ | 0.10 (0.004) (M) | T | U (S) | V (S)

0.15 (0.006) | T | U (S)

**2X L/2**

**L**

PIN 1
IDENT.

16          9

16          9

1          8

0.15 (0.006) | T | U (S)

**A**

**−V−**

**B**

**−U−**

**K**

**K1**

**J1**

**J**

**SECTION N−N**

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

**C**

0.10 (0.004)

**−T−** SEATING
PLANE

**D**

**G**

**H**

**DETAIL E**

**−W−**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**SOLDERING FOOTPRINT**

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM\***

16

XXXX
XXXX
ALYW

1

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪",
may or may not be present.

| DOCUMENT NUMBER: | 98ASH70247A | |
|---|---|---|
| DESCRIPTION: | TSSOP−16 | **PAGE 1 OF 1** |

## PUBLICATION ORDERING INFORMATION

◊

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