MC74VHC74

Dual D-Type Flip-Flop with Set and Reset

The MC74VHC74 is an advanced high speed CMOS D−type flip−flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset ($\overline{RD}$) and Set ($\overline{SD}$) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
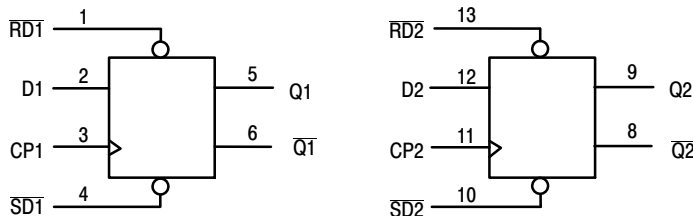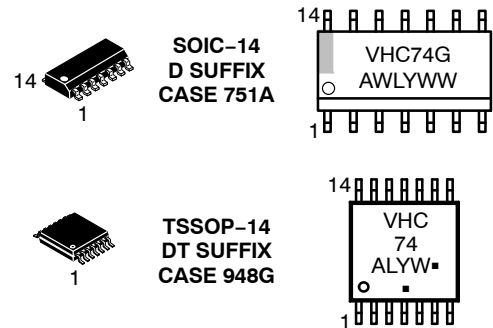- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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FUNCTION TABLE

Inputs				Outputs	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	⌐	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ORDERING INFORMATION

Figure 1. LOGIC DIAGRAM

MC74VHC74
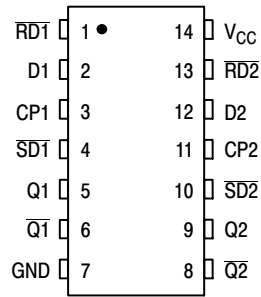
Figure 2. PIN ASSIGNMENT

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage	-0.5 to $+7.0$	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC}+0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating   SOIC Packages: -7 mW/°C from 65° to 125°C
         TSSOP Package: -6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

MC74VHC74

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	TA = 25°C			TA = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions		TA = 25°C			TA = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q or $\overline{Q}$	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		6.7 9.2	11.9 15.4	1.0 1.0	14.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		4.6 6.1	7.3 9.3	1.0 1.0	8.5 10.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{SD}$ or $\overline{RD}$ to Q or $\overline{Q}$	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$		7.6 10.1	12.3 15.8	1.0 1.0	14.5 18.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		4.8 6.3	7.7 9.7	1.0 1.0	9.0 11.0	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$ $C_L = 50pF$	80 50	125 75		70 45		MHz
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$	130 90	170 115		110 75		
C_{in}	Maximum Input Capacitance				4	10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1)	25	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit		Unit
			$T_A = 25°C$	$T_A = −55°C$ to $+125°C$	
t_w	Minimum Pulse Width, CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_w	Minimum Pulse Width, $\overline{RD}$ or $\overline{SD}$	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_{su}	Minimum Setup Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_h	Minimum Hold Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	ns
t_{rec}	Minimum Recovery Time, $\overline{SD}$ or $\overline{RD}$ to CP	3.3 ± 0.3 5.0 ± 0.5	5.0 3.0	5.0 3.0	ns

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74VHC74DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74VHC74DTG	TSSOP−14 (Pb−Free)	96 Units / Rail
MC74VHC74DTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLV74VHC74DTR2G*	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
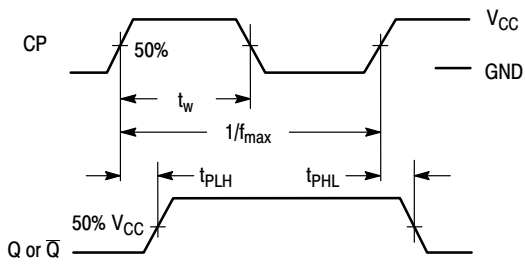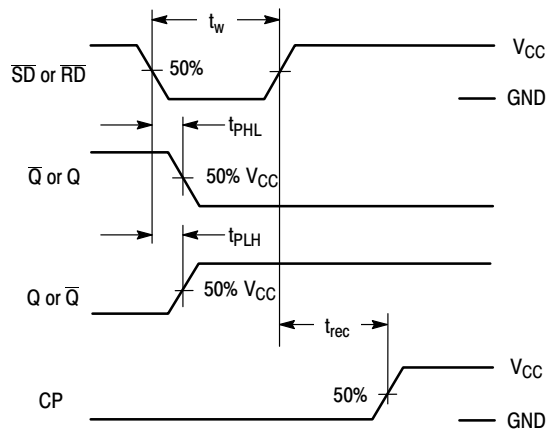
Figure 3.

Figure 4.

Switching Waveforms
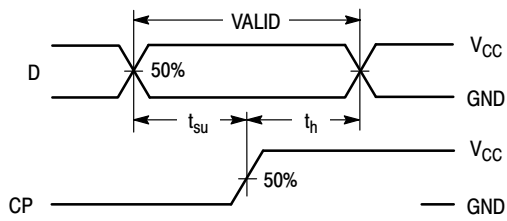
Figure 5.
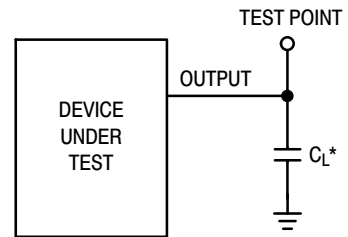
Figure 6.

*Includes all probe and jig capacitance
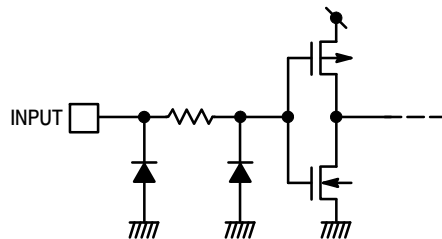
Figure 7. Input Equivalent Circuit

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14

1

SCALE 1:1

DETAIL A

DETAIL A

X 45°

SEATING PLANE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*

6.50

14X 1.18

1.27 PITCH

14X 0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
Y   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
   2. ANODE/CATHODE
   3. ANODE/CATHODE
   4. NO CONNECTION
   5. ANODE/CATHODE
   6. NO CONNECTION
   7. ANODE/CATHODE
   8. ANODE/CATHODE
   9. ANODE/CATHODE
   10. NO CONNECTION
   11. ANODE/CATHODE
   12. ANODE/CATHODE
   13. NO CONNECTION
   14. COMMON ANODE

STYLE 2:
         CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
   2. ANODE
   3. ANODE
   4. NO CONNECTION
   5. ANODE
   6. NO CONNECTION
   7. ANODE
   8. ANODE
   9. ANODE
   10. NO CONNECTION
   11. ANODE
   12. ANODE
   13. NO CONNECTION
   14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
   2. CATHODE
   3. CATHODE
   4. NO CONNECTION
   5. CATHODE
   6. NO CONNECTION
   7. CATHODE
   8. CATHODE
   9. CATHODE
   10. NO CONNECTION
   11. CATHODE
   12. CATHODE
   13. NO CONNECTION
   14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
   2. ANODE/CATHODE
   3. ANODE/CATHODE
   4. ANODE/CATHODE
   5. ANODE/CATHODE
   6. NO CONNECTION
   7. COMMON ANODE
   8. COMMON CATHODE
   9. ANODE/CATHODE
   10. ANODE/CATHODE
   11. ANODE/CATHODE
   12. ANODE/CATHODE
   13. NO CONNECTION
   14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
   2. CATHODE
   3. CATHODE
   4. CATHODE
   5. CATHODE
   6. CATHODE
   7. CATHODE
   8. ANODE
   9. ANODE
   10. ANODE
   11. ANODE
   12. ANODE
   13. ANODE
   14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
   2. COMMON ANODE
   3. COMMON CATHODE
   4. ANODE/CATHODE
   5. ANODE/CATHODE
   6. ANODE/CATHODE
   7. ANODE/CATHODE
   8. ANODE/CATHODE
   9. ANODE/CATHODE
   10. ANODE/CATHODE
   11. COMMON CATHODE
   12. COMMON ANODE
   13. ANODE/CATHODE
   14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
   2. ANODE/CATHODE
   3. ANODE/CATHODE
   4. NO CONNECTION
   5. ANODE/CATHODE
   6. ANODE/CATHODE
   7. COMMON ANODE
   8. COMMON ANODE
   9. ANODE/CATHODE
   10. ANODE/CATHODE
   11. NO CONNECTION
   12. ANODE/CATHODE
   13. ANODE/CATHODE
   14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

◁ | 0.15 (0.006) | T U Ⓢ

2X **L/2**

L

PIN 1
IDENT.

14   8

1   7

◁ | 0.15 (0.006) | T U Ⓢ

A

−V−

B
−U−

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1

SECTION N−N

C

◁ | 0.10 (0.004)

−T− SEATING
PLANE

D   **G**   **H**

DETAIL E

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

GENERIC
MARKING DIAGRAM*

14

XXXX
XXXX
ALYW▪

1

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**TSSOP−14 WB**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊

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