MC74HCT132A

Quad 2-Input NAND Gate with Schmitt-Trigger Inputs with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

The MC74HCT132A can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

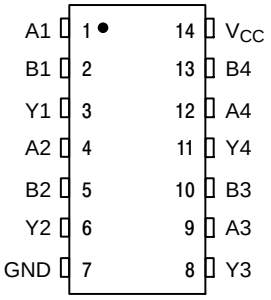

Figure 1. Pin Assignment

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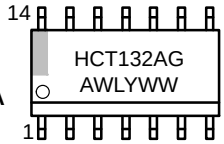
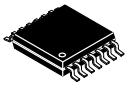
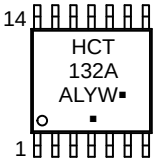
MARKING DIAGRAMS

SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

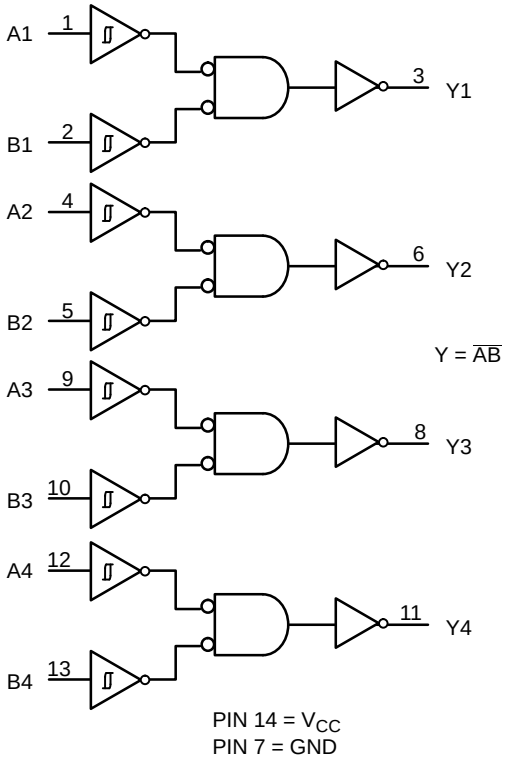


Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT132ADG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74HCT132ADR2G		2500 / Tape & Reel
NLV74HCT132ADR2G*		2500 / Tape & Reel
MC74HCT132ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLVHCT132ADTR2G*		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	−0.5 to +7.0 −0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{GND}	DC Ground Current per Ground Pin		±75	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	14−SOIC 14−TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >100 >500	V
$I_{Latch-Up}$	Latch−Up Performance	Above V_{CC} and Below GND at 85°C (Note 4)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	−	No Limit (Note 5)	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. When $V_{IN} \sim 0.5\ V_{CC}$, I_{CC} >> quiescent current.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55°C to 25°C	≤85°C	≤125°C	
V_{T+}max	Maximum Positive−Going Input Threshold Voltage	V_{OUT} = 0.1 V $\|I_{OUT}\| \le 20$ μA	4.5 5.5	1.9 2.1	1.9 2.1	1.9 2.1	V
V_{T+}min	Minimum Positive−Going Input Threshold Voltage	V_{OUT} = 0.1 V $\|I_{OUT}\| \le 20$ μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}max	Maximum Negative−Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $\|I_{OUT}\| \le 20$ μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}min	Minimum Negative−Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $\|I_{OUT}\| \le 20$ μA	4.5 5.5	0.5 0.6	0.5 0.6	0.5 0.6	V
$V_H$min (Note 7)	Minimum Hysteresis Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\| \le 20$ μA	4.5 5.5	0.4 0.4	0.4 0.4	0.4 0.4	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} \le$ V_{T-}min or V_{T+}max $\|I_{OUT}\| \le 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{IN} \le$ $-V_{T-}$min or V_{T+}max $\|I_{OUT}\| \le 4.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} \ge V_{T+}$max $\|I_{OUT}\| \le 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{IN} \ge V_{T+}$max $\|I_{OUT}\| \le 4.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0 μA	5.5	1.0	10	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

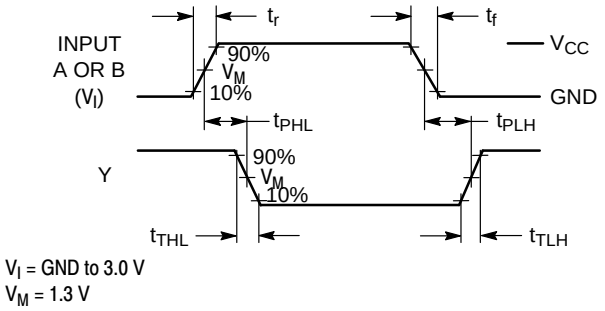
7. $V_H$min > (V_{T+}min) − (V_{T-}max); $V_H$max = (V_{T+}max) + (V_{T-}min).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns, V_{CC} = 5.0 V ± 10%)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55°C to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	5.0	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	5.0	15	19	22	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

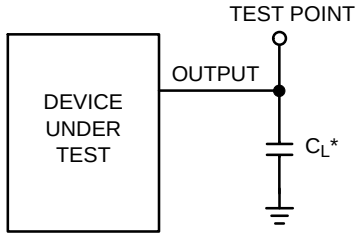
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Gate) (Note 8)	24	pF

8. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.



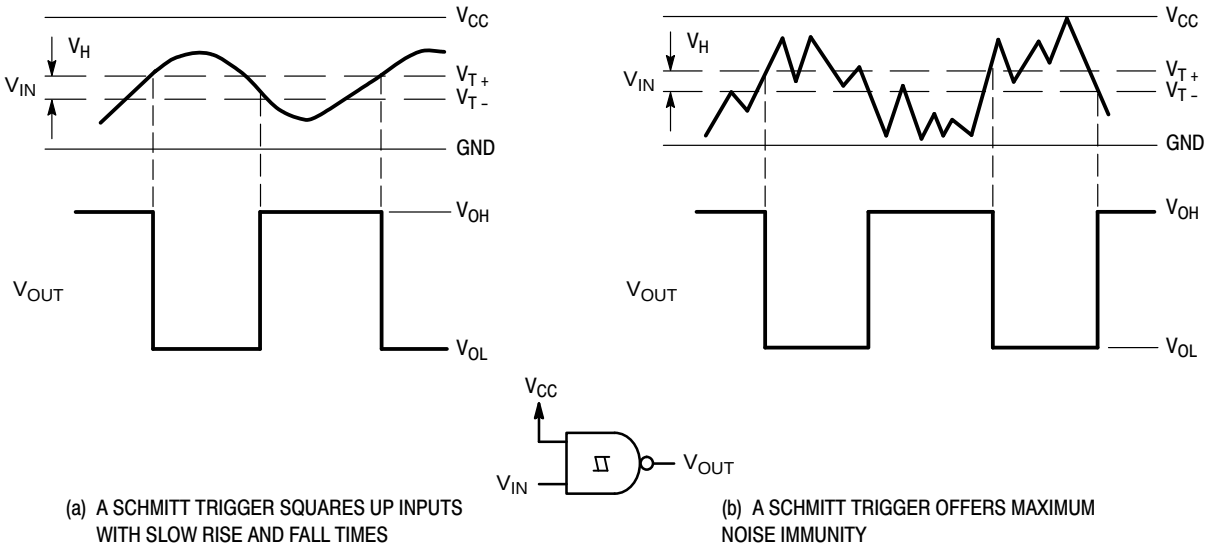
V_I = GND to 3.0 V
V_M = 1.3 V

Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit



(a) A SCHMITT TRIGGER SQUARES UP INPUTS WITH SLOW RISE AND FALL TIMES

(b) A SCHMITT TRIGGER OFFERS MAXIMUM NOISE IMMUNITY

Figure 5. Typical Schmitt−Trigger Applications

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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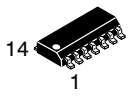

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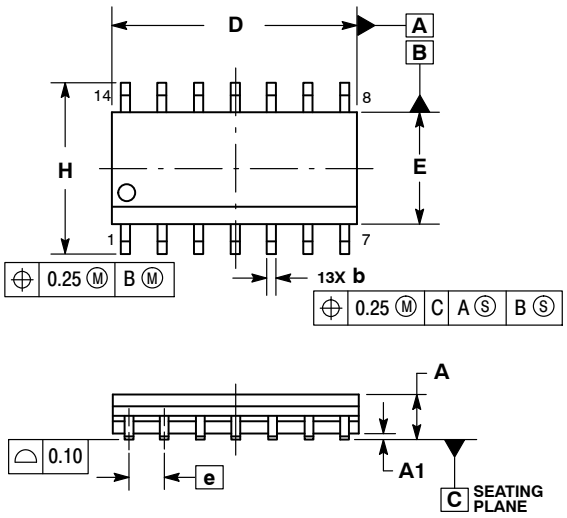
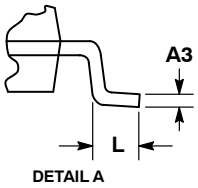
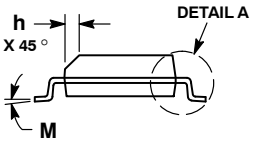
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



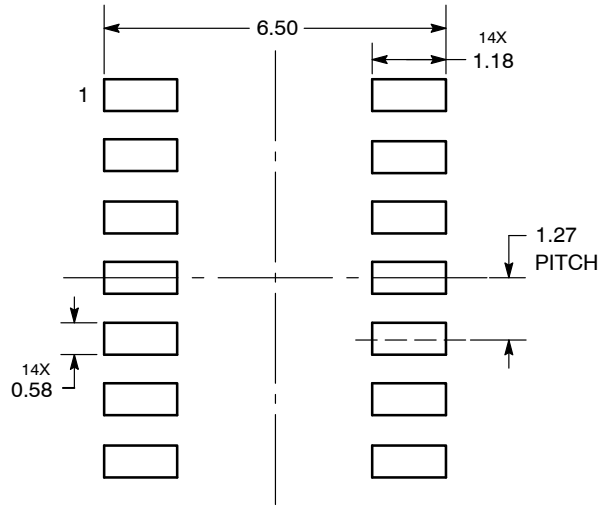




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

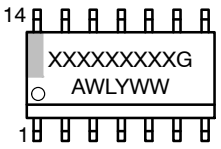
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

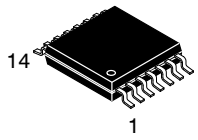
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



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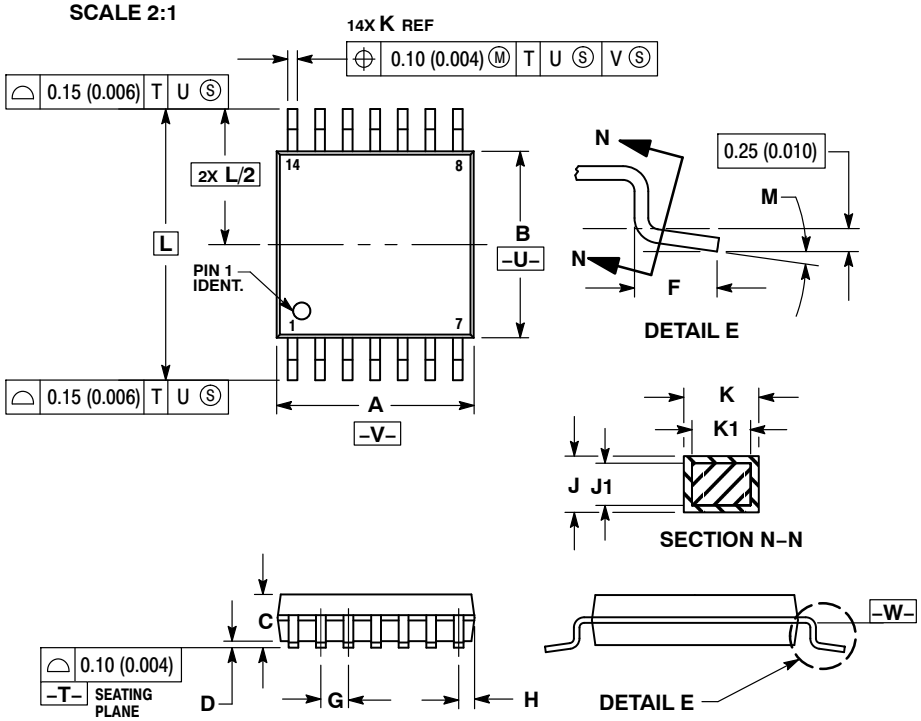
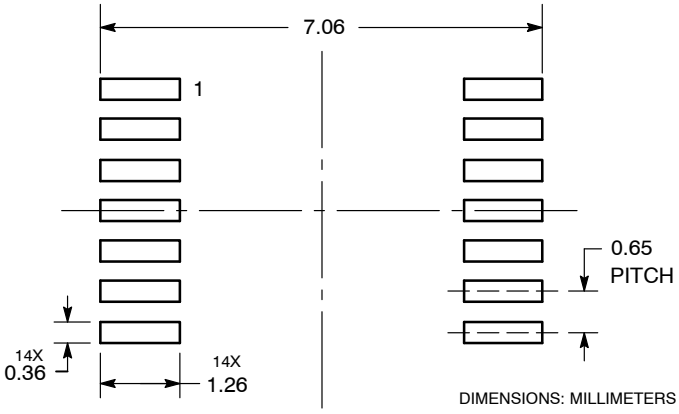


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

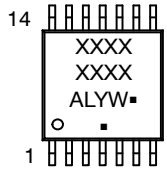
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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