NLX1G74

Single D Flip-Flop

The NLX1G74 is a high performance, full function edge−triggered D Flip−Flop in ultra−small footprint. The NLX1G74 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- Extremely High Speed: t_{PD} = 2.6 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- 24 mA Balanced Output Sink and Source Capability at V_{CC} = 3.0 V
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra Small Package
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

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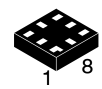
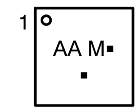
http://onsemi.com



UQFN8
MU SUFFIX
CASE 523AN

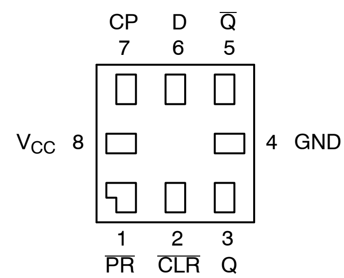
MARKING DIAGRAM



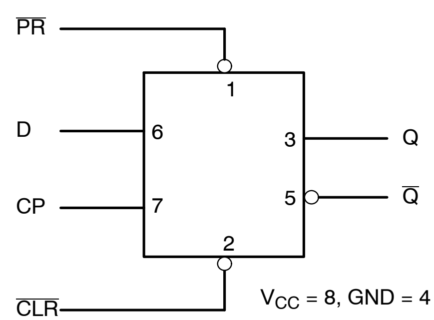
AA = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

Inputs				Outputs		
$\overline{PR}$	$\overline{CLR}$	CP	D	Q	$\overline{Q}$	Operating Mode
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	↑̸	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low−to−High Transition
↑̸ = Not a Low−to−High Transition
For I_{CC} reasons, DO NOT FLOAT Inputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage − Output in High or Low State (Note 1)		−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current Per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		250	°C/W
P_D	Power Dissipation in Still Air at 85°C		250	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm X 1 inch, 2 ounce copper trace with no air flow.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage	(Note 6)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	V_{CC}	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5.0	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

ORDERING INFORMATION

Device	Package	Shipping†
NLX1G74MUTCG	UQFN8 (Pb−Free)	3000 / Tape & Reel
NLVX1G74MUTCG*	UQFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$-40°C \le T_A \le 85°C$ Min	$-40°C \le T_A \le 85°C$ Max	Unit
V_{IH}	High−Level Input Voltage		1.65	0.75 V_{CC}			0.75 V_{CC}		V
			2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65			0.25 V_{CC}		0.25 V_{CC}	V
			2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	
V_{OH}	High−Level Output Voltage $V_{IN} = V_{IL}$ or V_{IL}	I_{OH} = 100 μA	1.65 to 5.5	V_{CC} − 0.1	V_{CC}		V_{CC} − 0.1		V
		I_{OH} = −3 mA	1.65	1.29	1.52		1.29		
		I_{OH} = −8 mA	2.3	1.9	2.1		1.9		
		I_{OH} = −12 mA	2.7	2.2	2.4		2.2		
		I_{OH} = −16 mA	3.0	2.4	2.7		2.4		
		I_{OH} = −24 mA	3.0	2.3	2.5		2.3		
		I_{OH} = −32 mA	4.5	3.8	4.0		3.8		
V_{OL}	Low−Level Output Voltage $V_{IN} = V_{IH}$	I_{OL} = 100 μA	1.65 to 5.5		0.008	0.1		0.1	V
		I_{OL} = 3 mA	1.65		0.10	0.24		0.24	
		I_{OL} = 8 mA	2.3		0.12	0.3		0.3	
		I_{OL} = 12 mA	2.7		0.15	0.4		0.4	
		I_{OL} = 16 mA	3.0		0.19	0.4		0.4	
		I_{OL} = 24 mA	3.0		0.30	0.55		0.55	
		I_{OL} = 32 mA	4.5		0.30	0.55		0.55	
I_{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5			±0.1		±1.0	μA
I_{OFF}	Power off Input Leakage Current	5.5V or V_{IN} = GND	0			1.0		10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

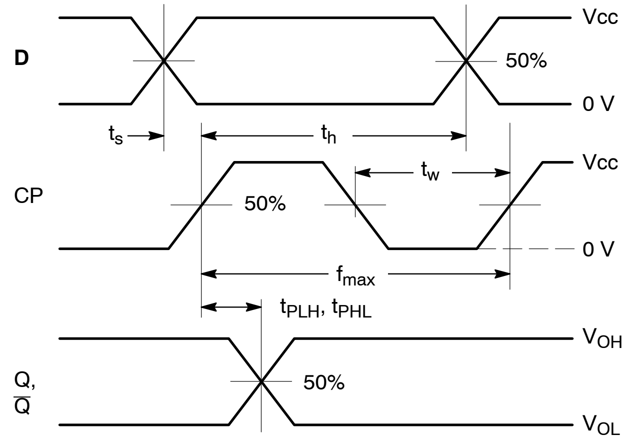
Symbol	Parameter	V_{CC} (V)	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	Unit
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	75			75		MHz
		2.5 ± 0.2		150			150		
		3.3 ± 0.3		200			200		
		5.0 ± 0.5		250			250		
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	175			175		
		5.0 ± 0.5		200			200		
t_{PLH}, t_{PHL}	Propagation Delay, CP to Q or $\overline{Q}$ (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	2.5	6.5	12.5	2.5	13	ns
		2.5 ± 0.2		1.5	3.8	7.5	1.5	8.0	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	4.5	0.8	5.0	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$ (Waveform 2)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	2.5	6.5	14	2.5	14.5	ns
		2.5 ± 0.2		1.5	3.8	9.0	1.5	9.5	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	5.0	0.8	5.5	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t_S	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	6.5			6.5		ns
		2.5 ± 0.2		3.5			3.5		
		3.3 ± 0.3		2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
t_H	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	0.5			0.5		ns
		2.5 ± 0.2		0.5			0.5		
		3.3 ± 0.3		0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
t_W	Pulse Width, CP, $\overline{CLR}$, $\overline{PR}$ (Waveform 3)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	6.0			6.0		ns
		2.5 ± 0.2		4.0			4.0		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
t_{REC}	Recover Time $\overline{PR}$; $\overline{CLR}$ to CP (Waveform 3)	1.8 ± 0.15	$C_L = 15$ pF, $R_D = 1$ MΩ, S_1 = Open	8.0			8.0		MHz
		2.5 ± 0.2		4.5			4.5		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		3.0			3.0		
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω, S_1 = Open	3.0			3.0		
		5.0 ± 0.5		3.0			3.0		

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

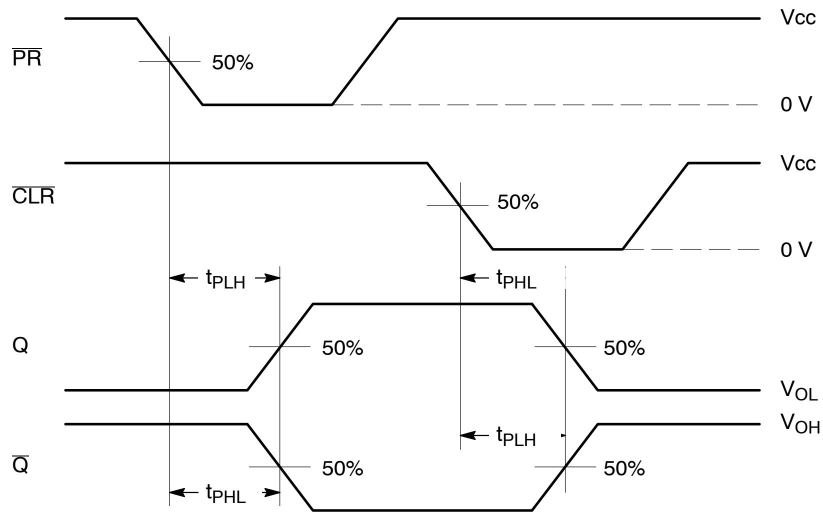
CAPACITANCE (Note 8)

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5$ V	7.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5$ V	7.0	pF
C_{PD}	Power Dissipation Capacitance (Note 9) Frequency = 10 MHz	$V_{CC} = 3.3$ V $V_{CC} = 5.0$ V	16 21	pF

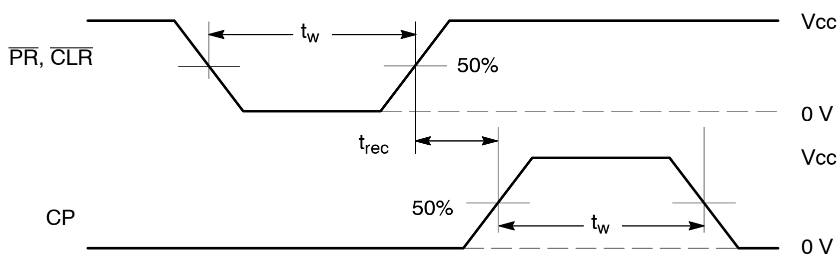
8. $T_A = +25°C$, f = 1 MHz
9. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 1) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC(static)}$.



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 3.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns



WAVEFORM 2 – PROPAGATION DELAYS
$t_R = t_F = 3.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns



WAVEFORM 3 – RECOVERY TIME
$t_R = t_F = 3.0$ ns from 10% to 90%; f = 1 MHz; $t_w = 500$ ns
Output Reg: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

Figure 1. AC Waveforms

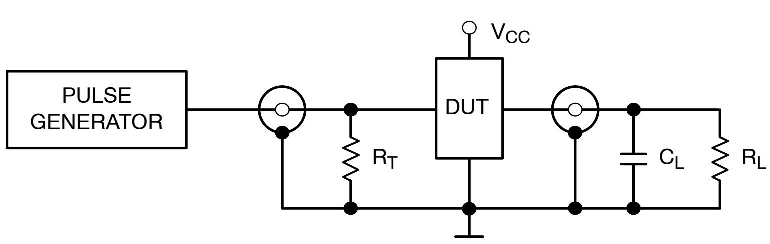
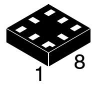


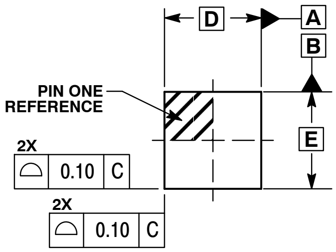
Figure 2. Test Circuit

UQFN8, 1.6x1.6, 0.5P
CASE 523AN−01
ISSUE O

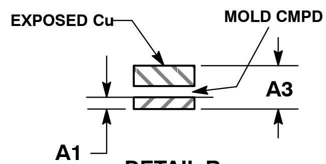
DATE 26 NOV 2008



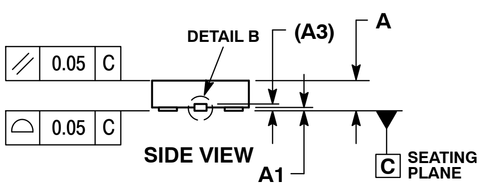
SCALE 4:1



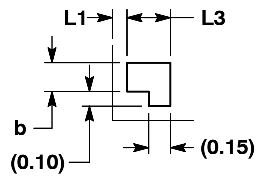
TOP VIEW



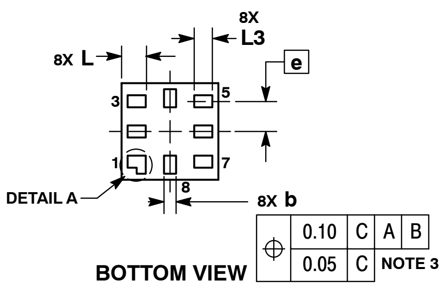
DETAIL B
OPTIONAL CONSTRUCTION



SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTION

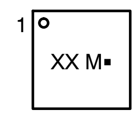


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	−−−	0.15
L3	0.25	0.35

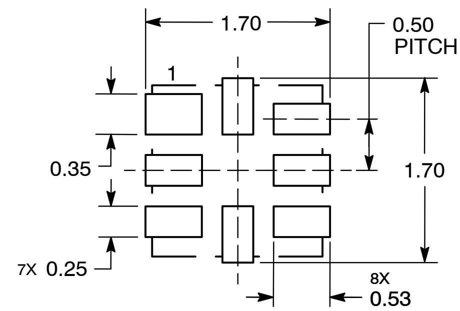
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON36348E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**8 PIN UQFN, 1.6X1.6, 0.5P**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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