NLX2G86

Dual 2-Input Exclusive-OR Gate

The NLX2G86 is a high performance dual 2–input Exclusive–OR Gate operating from a 1.65 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.4 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with V_{CC} = 3.0 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ86
- This is a Pb–Free Device

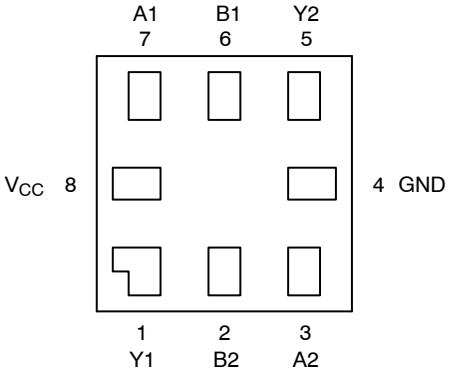

Figure 1. Pinout (Top View)

PIN ASSIGNMENT

Pin	Function
1	Y1
2	B2
3	A2
4	GND
5	Y2
6	B1
7	A1
8	V_{CC}

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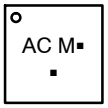
UQFN8
MU SUFFIX
CASE 523AN

MARKING DIAGRAM



AC = Device Code
M = Date Code*
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

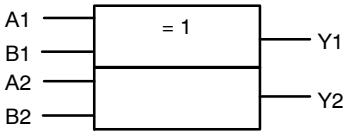


Figure 2. Logic Symbol

FUNCTION TABLE

Input		Output Y = A + B
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		−0.5 to +7.0	V
V_O	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	(Note 1)	TBD	°C/W
P_D	Power Dissipation in Still Air at 85°C		TBD	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage	(Note 5)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	5.5	V
T_A	Operating Free−Air Temperature		−40	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 1.8 V ±0.15 V V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0 0 0	20 20 10 5	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit	Condition
			Min	Typ	Max	Min	Max		
V_{IH}	High−Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V	
V_{IL}	Low−Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V	
V_{OH}	High−Level Output Voltage V_{IN} = V_{IH}	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5		1.55 1.7 2.2 2.9 4.4		V	I_{OH} = −100 μA
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20		1.29 1.9 2.4 2.3 3.8		V	I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IL}	1.65 1.8 2.3 3.0 4.5		0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1 0.1	V	I_{OL} = 100 μA
		1.65 2.3 3.0 3.0 4.5		0.08 0.10 0.15 0.22 0.22	0.24 0.30 0.40 0.55 0.55		0.24 0.30 0.40 0.55 0.55	V	I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±1.0		±1.0	μA	0 V ≤ V_{IN} ≤ 5.5 V
I_{OFF}	Power Off Leakage Current	0.0			1.0		10	μA	V_{IN} or V_{OUT} = 5.5 V
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μA	V_{IN} = 5.5 V, GND

AC ELECTRICAL CHARACTERISTICS $t_R = t_F$ = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	1.8 ± 0.15	2.0	7.9	9.0	2.0	10.5	ns
		R_L = 1 MΩ, C_L = 15 pF	2.5 ± 0.2	1.2	4.1	7.0	1.2	7.5	
		R_L = 1 MΩ, C_L = 15 pF	3.3 ± 0.3	0.8	3.0	4.8	0.8	5.2	
		R_L = 500 Ω, C_L = 50 pF		1.2	3.8	5.4	1.2	5.9	
		R_L = 1 MΩ, C_L = 15 pF	5.0 ± 0.5	0.5	2.2	3.5	0.5	3.8	
		R_L = 500 Ω, C_L = 50 pF		0.8	2.9	4.2	1.0	4.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	9	pF
		10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	11	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

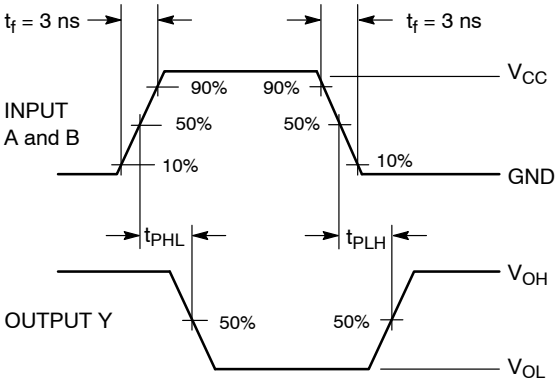
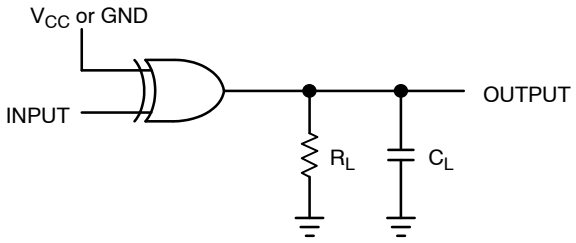


Figure 3. Switching Waveform



A 1−MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size†
NLX2G86MUTCG	UQFN8 (Pb−Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

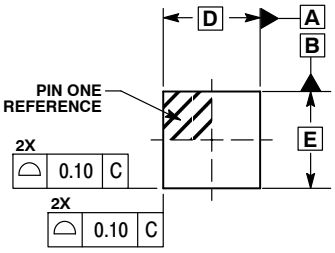
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

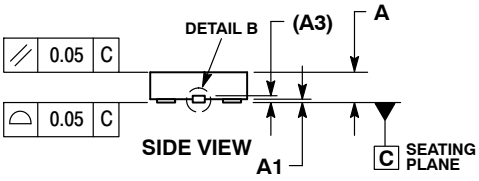
UQFN8, 1.6x1.6, 0.5P
CASE 523AN−01
ISSUE O

DATE 26 NOV 2008

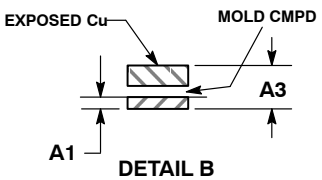
SCALE 4:1



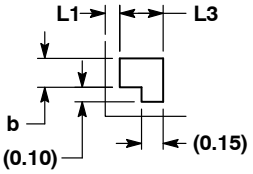
TOP VIEW



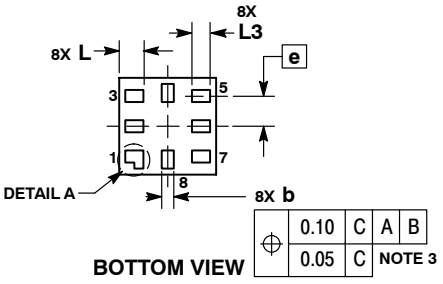
SIDE VIEW



DETAIL B
OPTIONAL
CONSTRUCTION



DETAIL A
OPTIONAL
CONSTRUCTION

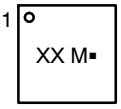


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	−−−	0.15
L3	0.25	0.35

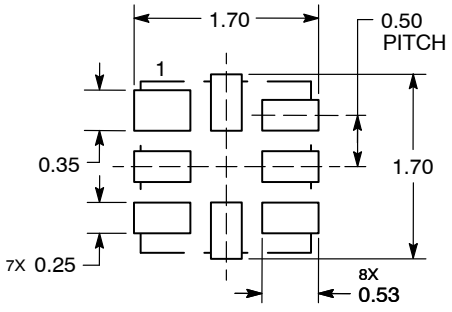
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**8 PIN UQFN, 1.6X1.6, 0.5P**	**PAGE 1 OF 1**

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