

# EMD4DXV6

## Dual Bias Resistor Transistors

### NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMD4DXV6T1 series, two complementary BRT devices are housed in the SOT-563 package which is ideal for low power surface mount applications where board space is at a premium.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for  $Q_1$  and  $Q_2$ , - minus sign for  $Q_1$  (PNP) omitted)

| Rating                    | Symbol    | Value | Unit |
|---------------------------|-----------|-------|------|
| Collector-Base Voltage    | $V_{CBO}$ | 50    | Vdc  |
| Collector-Emitter Voltage | $V_{CEO}$ | 50    | Vdc  |
| Collector Current         | $I_C$     | 100   | mAdc |

#### THERMAL CHARACTERISTICS

| Characteristic (One Junction Heated)  | Symbol          | Max         | Unit                       |
|---|-----------------|-------------|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$ (Note 1)<br>Derate above $25^\circ\text{C}$ (Note 1) | $P_D$           | 357<br>2.9  | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction-to-Ambient (Note 1)   | $R_{\theta JA}$ | 350         | $^\circ\text{C}/\text{W}$  |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$ (Note 1)<br>Derate above $25^\circ\text{C}$          | $P_D$           | 500<br>4.0  | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction-to-Ambient (Note 1)   | $R_{\theta JA}$ | 250         | $^\circ\text{C}/\text{W}$  |
| Junction and Storage Temperature  | $T_J, T_{stg}$  | -55 to +150 | $^\circ\text{C}$           |

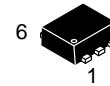
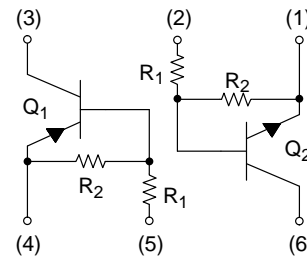
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 board with minimum mounting pad.



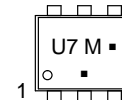
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SOT-563  
CASE 463A  
STYLE 1

#### MARKING DIAGRAM



U7 = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

| Device         | Package           | Shipping†          |
|----------------|-------------------|--------------------|
| EMD4DXV6T1G    | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| EMD4DXV6T5G    | SOT-563 (Pb-Free) | 8000 / Tape & Reel |
| NSVEMD4DXV6T5G | SOT-563 (Pb-Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# EMD4DXV6

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

### Q1 TRANSISTOR: PNP

#### OFF CHARACTERISTICS

|   |           |   |   |     |      |
|---|-----------|---|---|-----|------|
| Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )    | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_B = 0$ ) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ( $V_{EB} = 6.0$ , $I_C = 5.0\text{ mA}$ )  | $I_{EBO}$ | – | – | 0.2 | mAdc |

#### ON CHARACTERISTICS

|  |               |      |      |      |                  |
|--|---------------|------|------|------|------------------|
| Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )                             | $V_{(BR)CBO}$ | 50   | –    | –    | Vdc              |
| Collector-Emitter Breakdown Voltage ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )                            | $V_{(BR)CEO}$ | 50   | –    | –    | Vdc              |
| DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )                                   | $h_{FE}$      | 80   | 140  | –    |                  |
| Collector-Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )                | $V_{CE(SAT)}$ | –    | –    | 0.25 | Vdc              |
| Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  | $V_{OL}$      | –    | –    | 0.2  | Vdc              |
| Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) | $V_{OH}$      | 4.9  | –    | –    | Vdc              |
| Input Resistor   | R1            | 7.0  | 10   | 13   | $\text{k}\Omega$ |
| Resistor Ratio   | R1/R2         | 0.17 | 0.21 | 0.25 |                  |

### Q2 TRANSISTOR: NPN

#### OFF CHARACTERISTICS

|   |           |   |   |     |      |
|---|-----------|---|---|-----|------|
| Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )    | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_B = 0$ ) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ( $V_{EB} = 6.0$ , $I_C = 0\text{ mA}$ )    | $I_{EBO}$ | – | – | 0.1 | mAdc |

#### ON CHARACTERISTICS

|  |               |      |     |      |                  |
|--|---------------|------|-----|------|------------------|
| Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )                             | $V_{(BR)CBO}$ | 50   | –   | –    | Vdc              |
| Collector-Emitter Breakdown Voltage ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )                            | $V_{(BR)CEO}$ | 50   | –   | –    | Vdc              |
| DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )                                   | $h_{FE}$      | 80   | 140 | –    |                  |
| Collector-Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )                | $V_{CE(SAT)}$ | –    | –   | 0.25 | Vdc              |
| Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 3.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  | $V_{OL}$      | –    | –   | 0.2  | Vdc              |
| Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) | $V_{OH}$      | 4.9  | –   | –    | Vdc              |
| Input Resistor   | R1            | 32.9 | 47  | 61.1 | $\text{k}\Omega$ |
| Resistor Ratio   | R1/R2         | 0.8  | 1.0 | 1.2  |                  |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

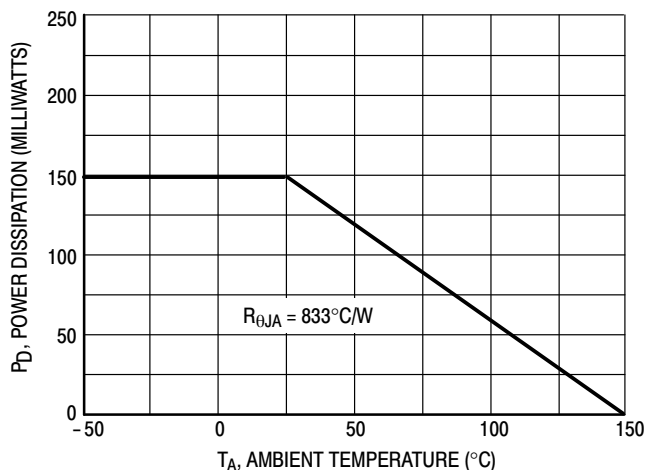


Figure 1. Derating Curve

# EMD4DXV6

## TYPICAL ELECTRICAL CHARACTERISTICS — EMD4DXV6 PNP TRANSISTOR

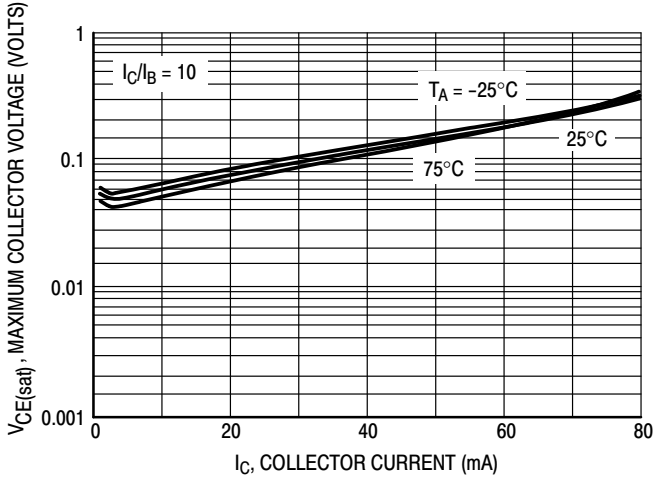


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

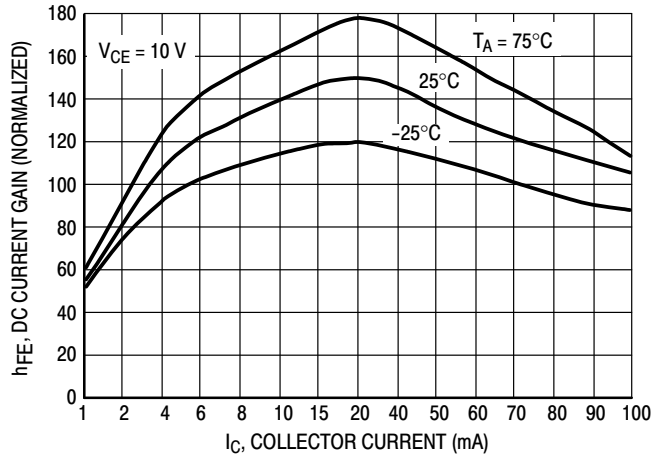


Figure 3. DC Current Gain

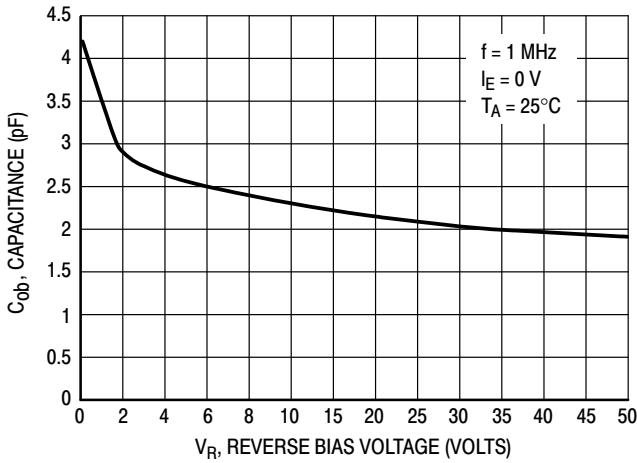


Figure 4. Output Capacitance

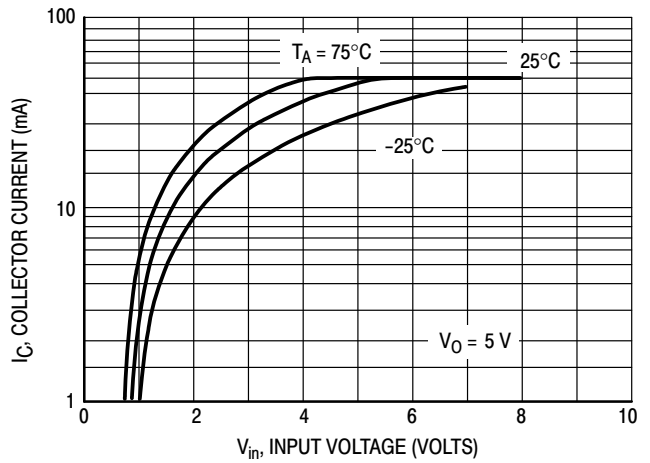


Figure 5. Output Current versus Input Voltage

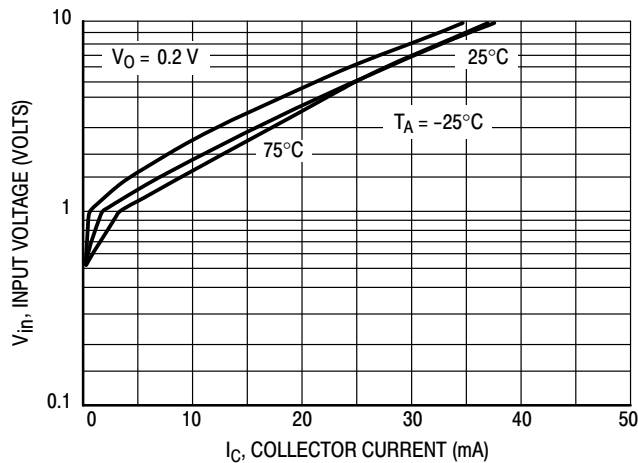


Figure 6. Input Voltage versus Output Current

# EMD4DXV6

## TYPICAL ELECTRICAL CHARACTERISTICS — EMD4DXV6 NPN TRANSISTOR

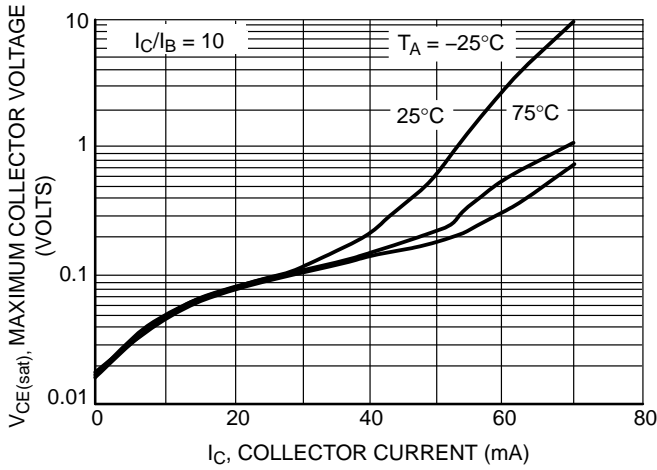


Figure 7.  $V_{CE(sat)}$  vs.  $I_C$

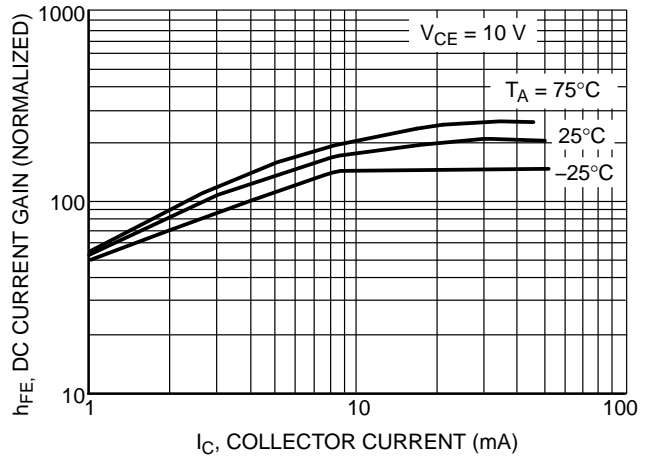


Figure 8. DC Current Gain

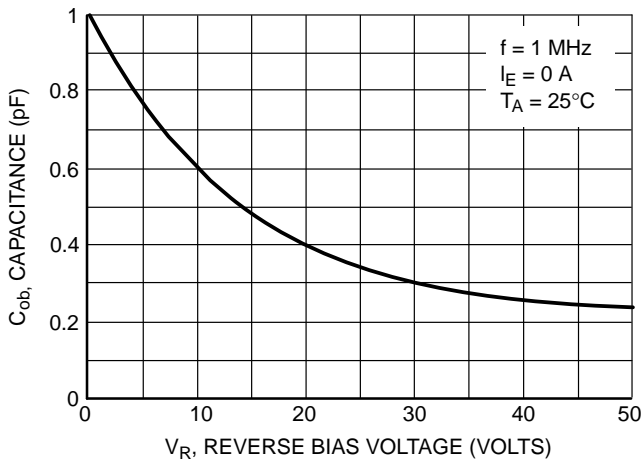


Figure 9. Output Capacitance

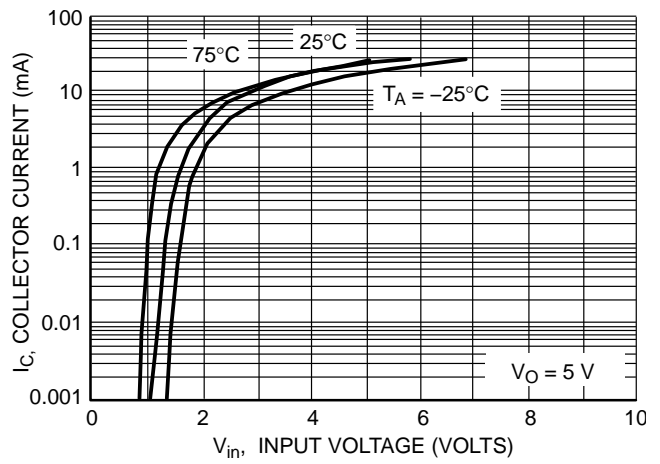


Figure 10. Output Current vs. Input Voltage

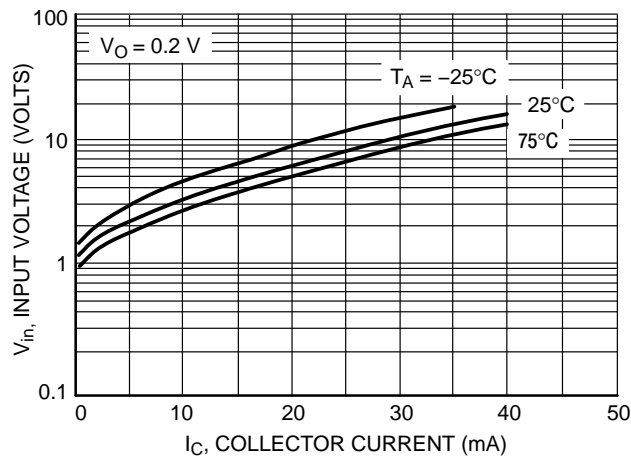
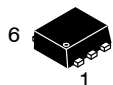


Figure 11. Input Voltage vs. Output Current

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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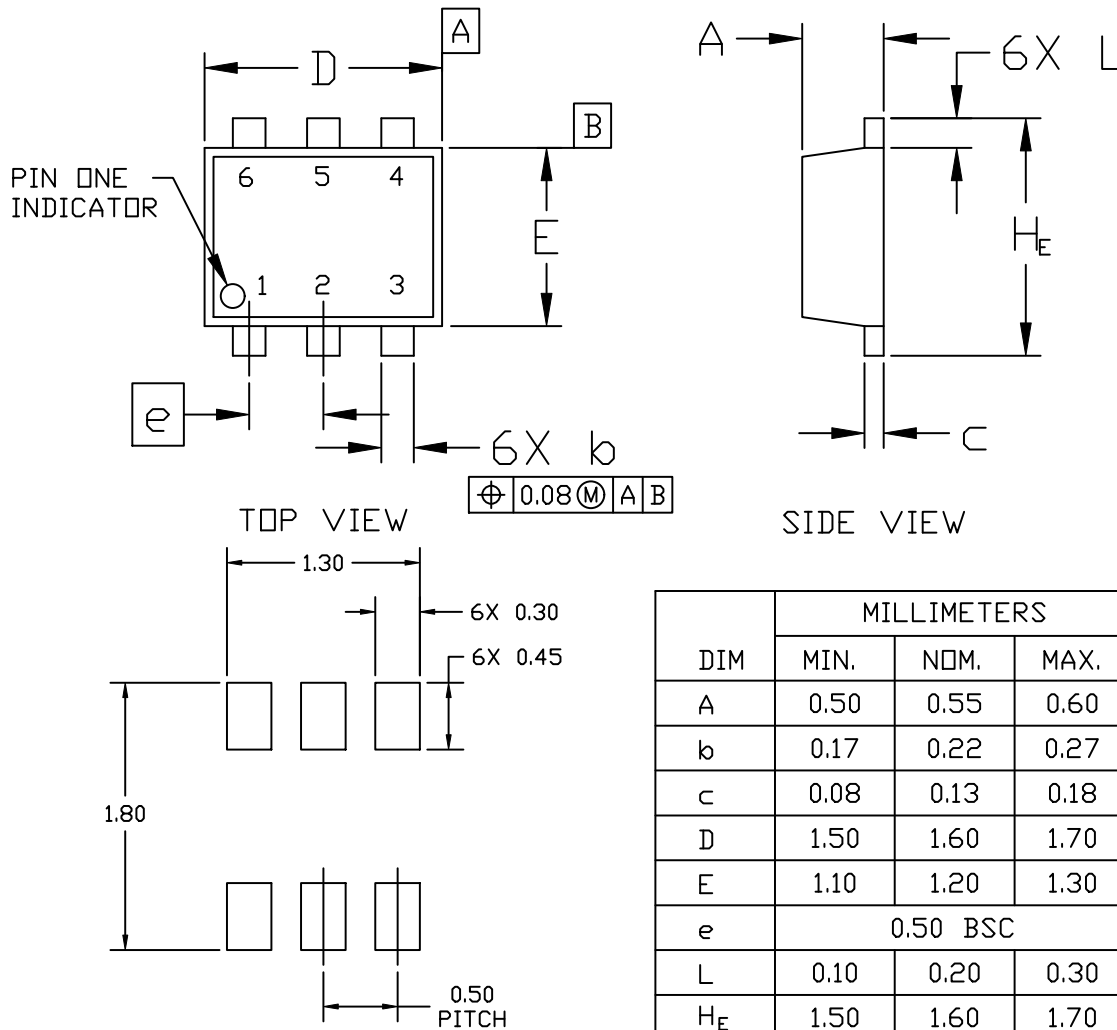
SCALE 4:1

**SOT-563, 6 LEAD**  
CASE 463A  
ISSUE H

DATE 26 JAN 2021

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



| DIM            | MILLIMETERS |      |      |
|----------------|-------------|------|------|
|                | MIN.        | NOM. | MAX. |
| A              | 0.50        | 0.55 | 0.60 |
| b              | 0.17        | 0.22 | 0.27 |
| c              | 0.08        | 0.13 | 0.18 |
| D              | 1.50        | 1.60 | 1.70 |
| E              | 1.10        | 1.20 | 1.30 |
| e              | 0.50 BSC    |      |      |
| L              | 0.10        | 0.20 | 0.30 |
| H <sub>E</sub> | 1.50        | 1.60 | 1.70 |

**RECOMMENDED MOUNTING FOOTPRINT\***

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                        |  |
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**SOT-563, 6 LEAD**  
CASE 463A  
ISSUE H

DATE 26 JAN 2021

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

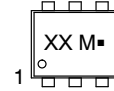
STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

STYLE 11:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

**GENERIC  
MARKING DIAGRAM\***



XX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                        |   |
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