N-Channel JFET, -15 V, 10 to 32 mA, 35 ms, Dual

Automotive JFET designed for compact and efficient designs and including high gain performance. AEC-Q101 qualified JFET and PPAP capable suitable for automotive applications.

Features

- Large | yfs |
- Small Ciss
- This Small Package Enables Sets to be Smaller and Thinner
- Ultralow Noise Figure
- MCPH5 Package is Pin-compatible with SC-88AFL
- Composite Type with 2 JFET Contained in a MCPH5 Package Currently in Use, Improving the Mounting Efficiency Greatly
- The NSVJ5908DSG5 is Formed with Two Chips, Being Equivalent to the NSVJ3557SA3, Placed in One Package
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- AM Tuner RF Amplification
- Low Noise Amplifier

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSX}	15	V
Gate-to-Drain Voltage	V _{GDS}	-15	V
Gate Current	I _G	10	mA
Drain Current	I _D	50	mA
Allowable Power Dissipation – 1 unit	P_{D}	200	mW
Total Power Dissipation	P _T	300	mW
Operating Junction and Storage Temperature	$T_{J_{I}}T_{Stg}$	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

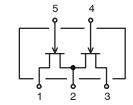


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ELECTRICAL CONNECTION

N-Channel

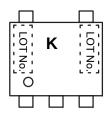


- 2: Source1/Source2
- 3: Drain 2
- 4: Gate2
- 5: Gate1



SC-88AFL/MCPH5 CASE 419AP

MARKING DIAGRAM



= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Table 1. ELECTRICAL CHARACTERISTICS $(T_A = 25^{\circ}C)$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Gate-to-Drain Breakdown Voltage	V _{(BR)GDS}	$I_G = -10 \mu A, V_{DS} = 0 V$	-15	-	-	V
Gate-to-Source Leakage Current	I _{GSS}	$V_{GS} = -10 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	-1.0	nA
Cutoff Voltage	V _{GS(off)}	V _{DS} = 5 V, I _D = 100 μA	-0.3	-0.7	-1.5	V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} = 5 V, V _{GS} = 0 V	10	-	32	mA
Forward Transfer Admittance	yfs	V _{DS} = 5 V, V _{GS} = 0 V, f = 1 kHz	24	35	-	mS
Input Capacitance	Ciss	V _{DS} = 5 V, V _{GS} = 0 V, f = 1 MHz	-	10.5	-	pF
Reverse Transfer Capacitance	Crss		-	3.5	-	pF
Noise Figure	NF	$V_{DS} = 5 \text{ V}, \text{ Rg} = 1 \text{ k}\Omega, \text{ I}_D = 1 \text{ mA}, \text{ f} = 1 \text{ kHz}$	-	1.0	-	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: The specifications shown above are for each individual JFET.

ORDERING INFORMATION

Device	Marking	Package Type	Shipping [†]
NSVJ5908DSG5T1G	К	SC-88AFL / MCPH5 (Pb-Free / Halogen Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

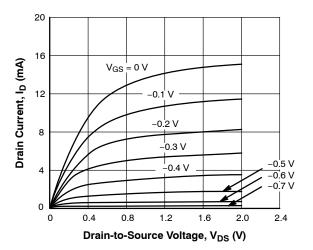


Figure 1. I_D vs. V_{DS}

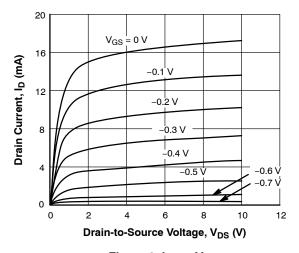


Figure 2. I_D vs. V_{DS}

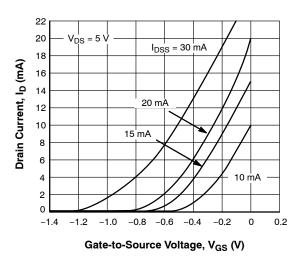


Figure 3. I_D vs. V_{GS}

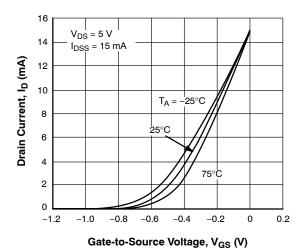


Figure 4. ID vs. VGS

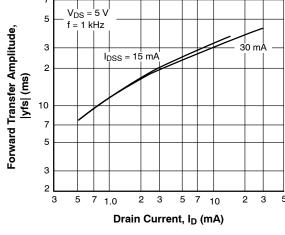


Figure 5. |yfs| vs. I_D

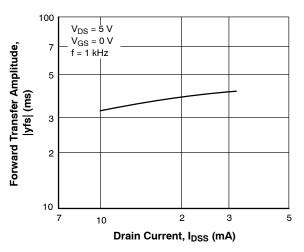


Figure 6. |yfs| vs. I_{DSS}

TYPICAL CHARACTERISTICS

3

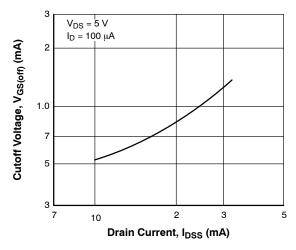


Figure 7. V_{GS(Off)} vs. I_{DSS}

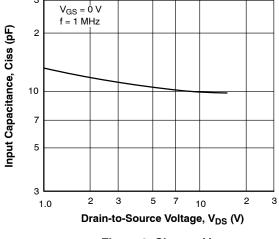


Figure 8. Ciss vs. V_{DS}

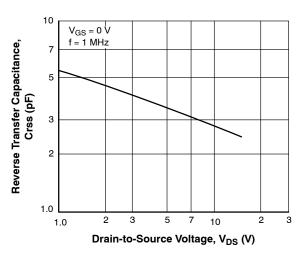


Figure 9. Crss vs. V_{DS}

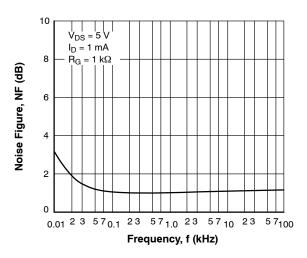


Figure 10. NF vs. f

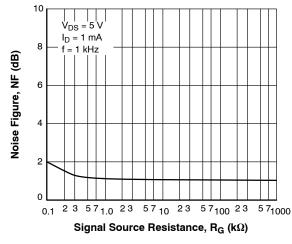


Figure 11. NF vs. R_G

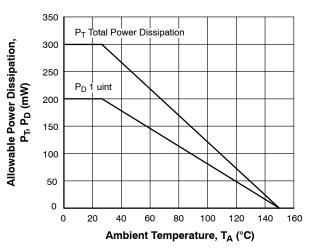


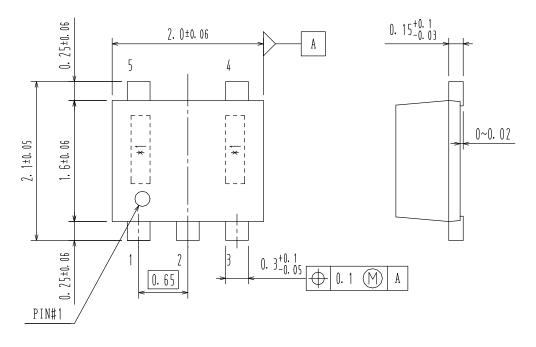
Figure 12. P_T, P_D vs. T_A

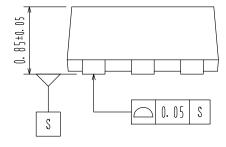


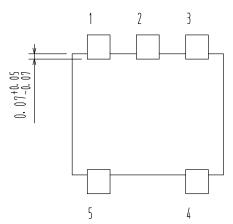
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