MMBT5087L

Low Noise Transistor

PNP Silicon

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	−50	Vdc
Collector – Base Voltage	V_{CBO}	−50	Vdc
Emitter – Base Voltage	V_{EBO}	−3.0	Vdc
Collector Current – Continuous	I_C	−50	mAdc

THERMAL CHARACTERISTICS

| Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) $T_A = 25°C$ Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25°C$ Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.062 in.
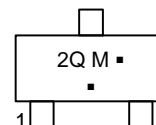2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

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COLLECTOR
3

1
BASE

2
EMITTER
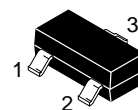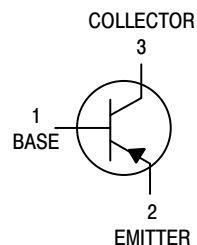
SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM

2Q M ▪

1

2Q = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping[†]
MMBT5087LT1G, NSVMMBT5087LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBT5087LT3G, NSVMMBT5087LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMBT5087L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−50	−	Vdc
Collector–Base Breakdown Voltage (I_C = −100 µAdc, I_E = 0)	$V_{(BR)CBO}$	−50	−	Vdc
Collector Cutoff Current (V_{CB} = −10 Vdc, I_E = 0) (V_{CB} = −35 Vdc, I_E = 0)	I_{CBO}	− −	−10 −50	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −100 µAdc, V_{CE} = −5.0 Vdc) (I_C = −1.0 mAdc, V_{CE} = −5.0 Vdc) (I_C = −10 mAdc, V_{CE} = −5.0 Vdc)	h_{FE}	250 250 250	800 − −	−
Collector–Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc)	$V_{CE(sat)}$	−	−0.3	Vdc
Base–Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc)	$V_{BE(sat)}$	−	0.85	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = −500 µAdc, V_{CE} = −5.0 Vdc, f = 20 MHz)	f_T	40	−	MHz
Output Capacitance (V_{CB} = −5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	−	4.0	pF
Small–Signal Current Gain (I_C = −1.0 mAdc, V_{CE} = −5.0 Vdc, f = 1.0 kHz)	h_{fe}	250	900	−
Noise Figure (I_C = −20 mAdc, V_{CE} = −5.0 Vdc, R_S = 10 kΩ, f = 1.0 kHz) (I_C = −100 µAdc, V_{CE} = −5.0 Vdc, R_S = 3.0 kΩ, f = 1.0 kHz)	NF	− −	2.0 2.0	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

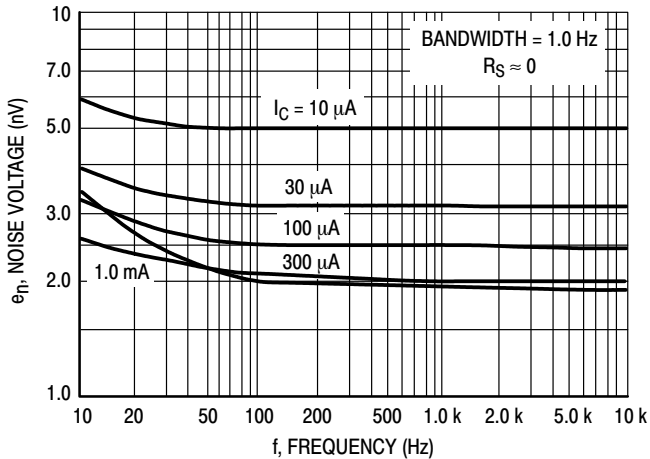## TYPICAL NOISE CHARACTERISTICS
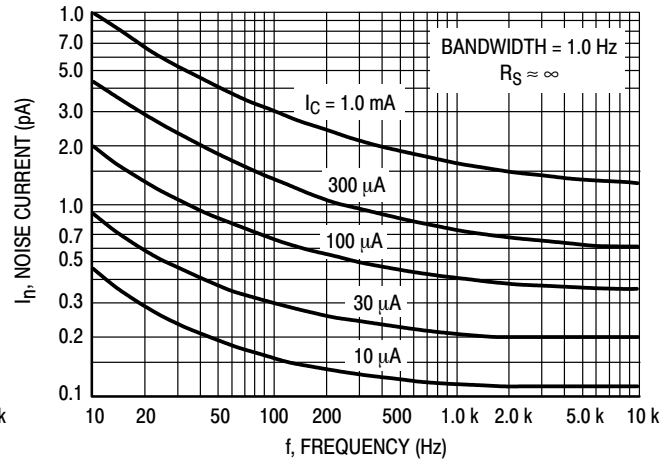(V_{CE} = −5.0 Vdc, T_A = 25°C)

Figure 1. Noise Voltage

Figure 2. Noise Current

NOISE FIGURE CONTOURS

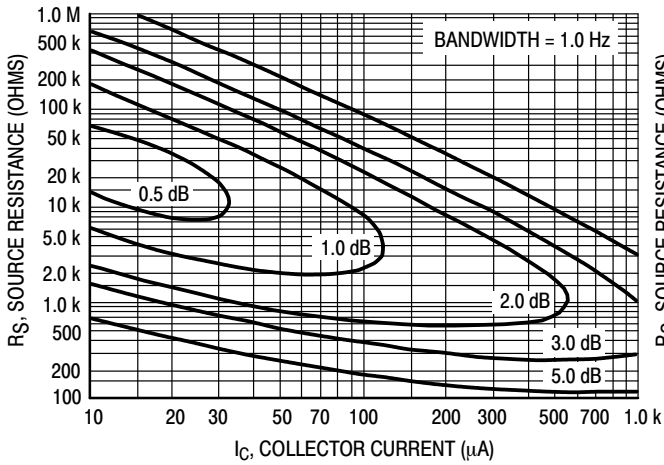$(V_{CE} = -5.0 \text{ Vdc}, T_A = 25°C)$
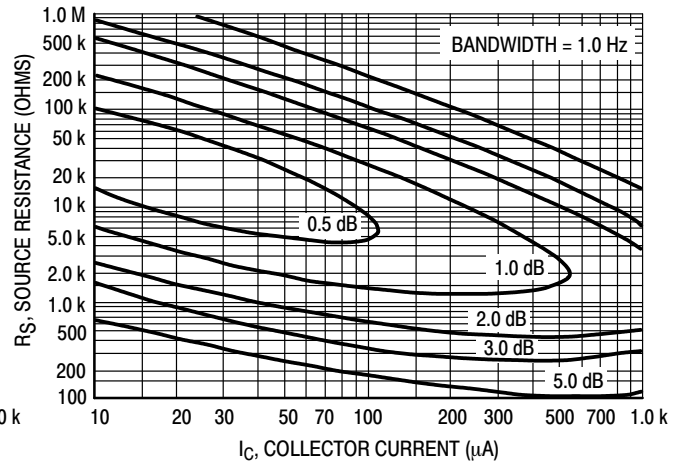
Figure 3. Narrow Band, 100 Hz
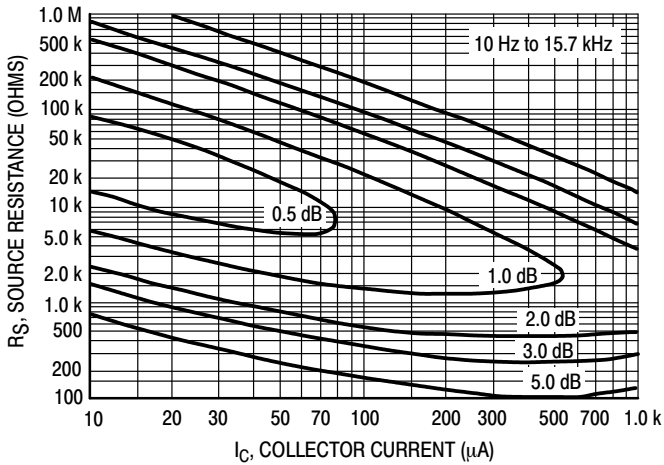
Figure 4. Narrow Band, 1.0 kHz

Figure 5. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10} \left[\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS
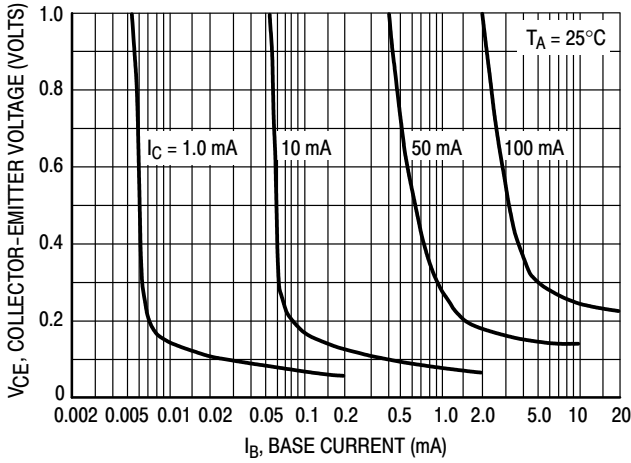
Figure 6. Collector Saturation Region
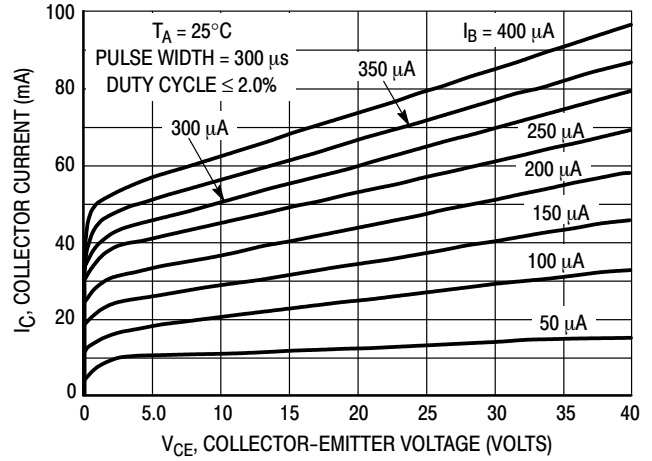
Figure 7. Collector Characteristics
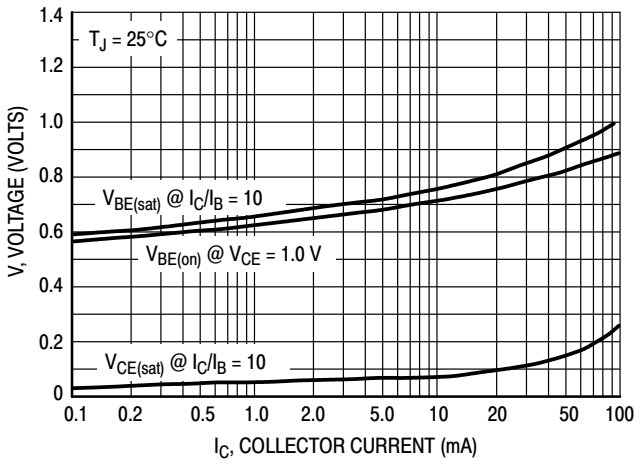
Figure 8. "On" Voltages
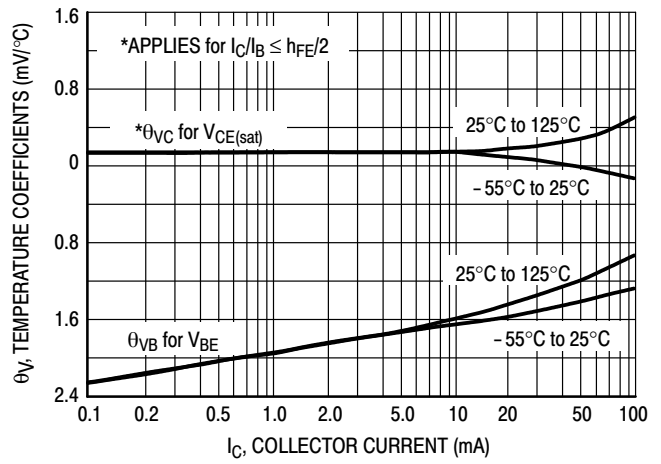
Figure 9. Temperature Coefficients

MMBT5087L

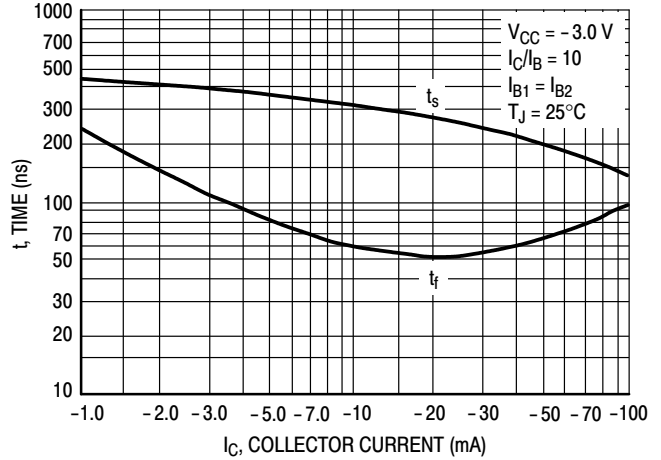## TYPICAL DYNAMIC CHARACTERISTICS
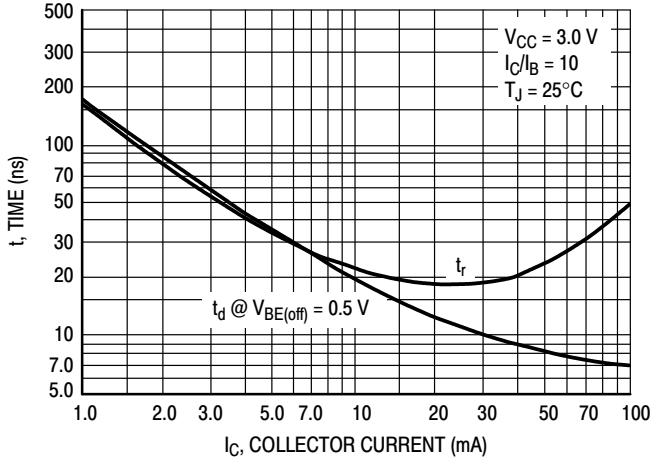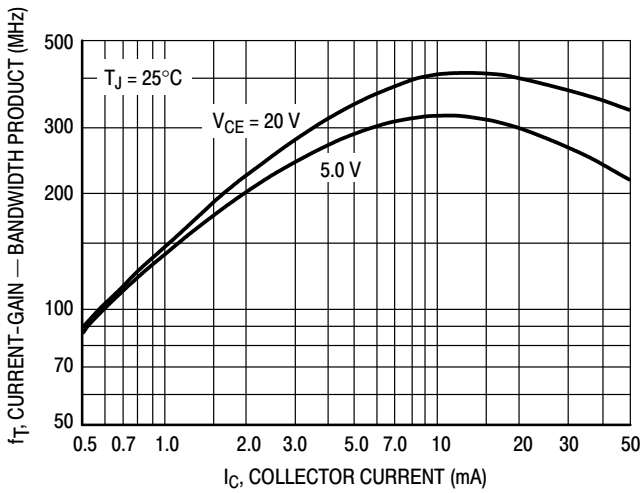

Figure 10. Turn−On Time

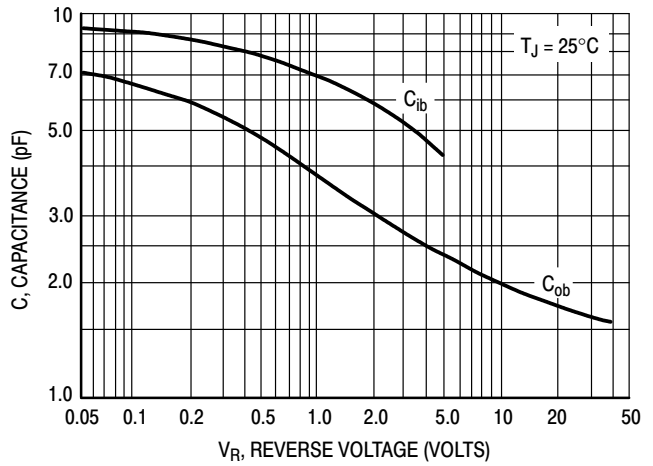Figure 11. Turn−Off Time

Figure 12. Current−Gain — Bandwidth Product

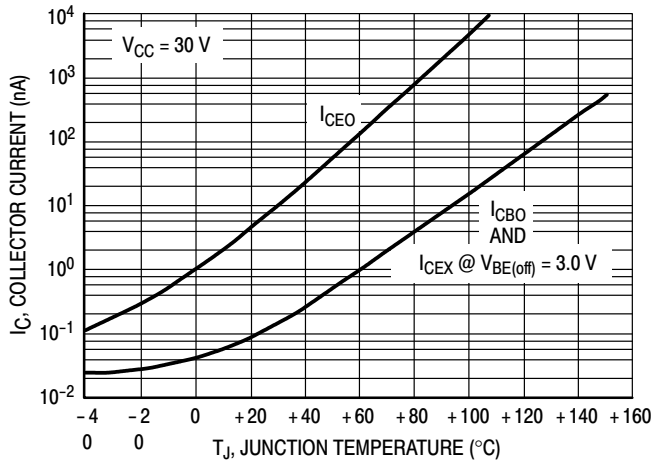Figure 13. Capacitance
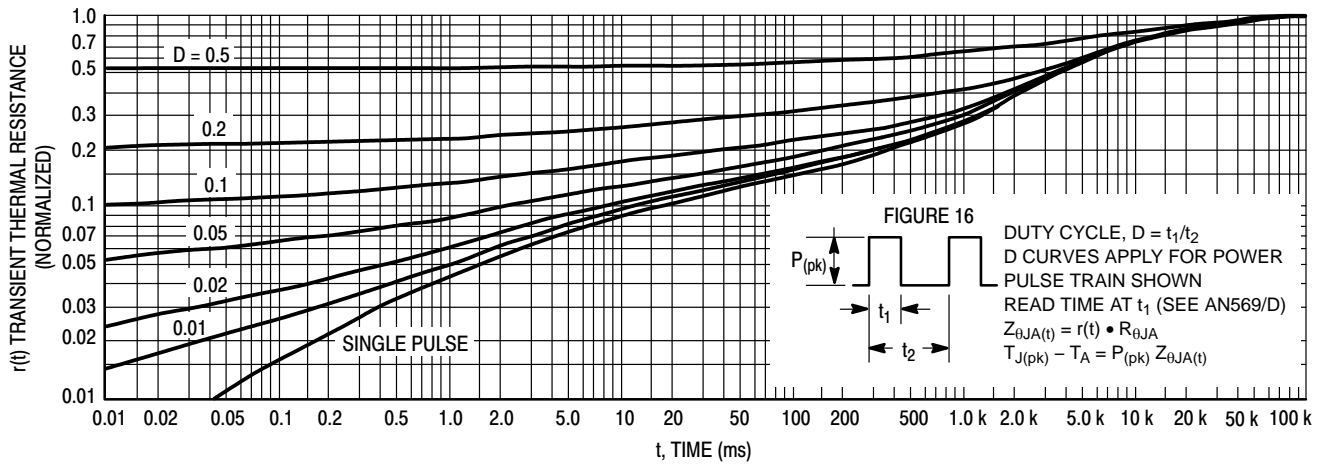
Figure 14. Thermal Response

Figure 15. Typical Collector Leakage Current

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 16. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 14 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 14 by the steady state value $R_{\theta JA}$.

Example:
Dissipating 2.0 watts peak under the following conditions:
  $t_1 = 1.0$ ms, $t_2 = 5.0$ ms (D = 0.2)
Using Figure 14 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore
  $\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at **www.onsemi.com**.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SOT−23 (TO−236)
CASE 318−08
ISSUE AS

DATE 30 JAN 2018

SCALE 4:1

TOP VIEW

VIEW C

SIDE VIEW

END VIEW

SEE VIEW C

**RECOMMENDED
SOLDERING FOOTPRINT**

2.90

3X 0.90

3X 0.80

0.95
PITCH

DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH.
   MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF
   THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
   PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H$_E$	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	———	10°	0°	———	10°

**GENERIC
MARKING DIAGRAM***

XXXM▪

1

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪",
may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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PUBLICATION ORDERING INFORMATION

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