# **MOSFET** - Single N-Channel

# 100 V, 9.0 m $\Omega$ , 60 A

# NTBS9D0N10MC

#### **Features**

- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Typical Applications**

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

## **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	100	٧
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	Steady T 05°C		I <sub>D</sub>	60	Α
Power Dissipation $R_{\theta JC}$ (Note 2)	State			68	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State T <sub>A</sub> = 25°C		I <sub>D</sub>	14	Α
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	Oldic		P <sub>D</sub>	3.8	W
Pulsed Drain Current	T <sub>C</sub> = 25°	°C, t <sub>p</sub> = 100 μs	I <sub>DM</sub>	239	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			Is	57	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L</sub> = 11 A <sub>pk</sub> , L = 3 mH)			E <sub>AS</sub>	181.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

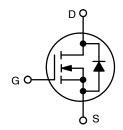
- 1. Surface–mounted on FR4 board using a 1 in<sup>2</sup>, 2 oz. Cu pad.
- 2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



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V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
100 V	9.0 mΩ @ 10 V	60 A



**N-CHANNEL MOSFET** 



CASE 418AJ

**MARKING DIAGRAM** 

AYWW77 NTBS9D0 N10MC

= Assembly Location

= Year WW = Work Week = Lot Traceability

NTBS9D0N10MC = Specific Device Code

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTBS9D0N10MC	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{ hetaJC}$	2.2	°C/W
Junction-to-Ambient - Steady State (Notes 1, 2)	$R_{ hetaJA}$	40	

### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u>.                                      </u>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, referenced to 25°C			56		mV/°C
Zero Gate Voltage Drain Current	Gate Voltage Drain Current $I_{DSS}$ $V_{GS} = 0 \text{ V},$ $T_{J} = 25^{\circ}\text{C}$		T <sub>J</sub> = 25°C			1	μΑ
		$V_{DS} = 80 \text{ V}$	T <sub>J</sub> = 150°C			100	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V}, V_{I}$	<sub>DS</sub> = 0 V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	: 131 μA	2.0	3.0	4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 131 μA, referen	iced to 25°C		-9.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub>	= 23 A		7.8	9.0	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub>	= 12 A		12	22.2	
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub>	= 23 A		59		S
Gate-Resistance	R <sub>G</sub>	T <sub>A</sub> = 25°0			0.6		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 50 V			1695		pF
Output Capacitance	Coss				935		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				13		
Total Gate Charge	Q <sub>G(TOT)</sub>				23		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 50 \text{ V},$ $I_{D} = 23 \text{ A}$ $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$			5		
Gate-to-Source Charge	Q <sub>GS</sub>				8		
Gate-to-Drain Charge	Q <sub>GD</sub>				5		
Output Charge	Q <sub>OSS</sub>				59		1
SWITCHING CHARACTERISTICS, V <sub>GS</sub>	= <b>10 V</b> (Note 3)						
Turn-On Delay Time	t <sub>d(ON)</sub>				15		ns
Rise Time	t <sub>r</sub>	VG9 = 10 V. VD9	= 50 V.		6		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$V_{GS}$ = 10 V, $V_{DS}$ = 50 V, $I_{D}$ = 23 A, $R_{G}$ = 6 $\Omega$			21		
Fall Time	t <sub>f</sub>				7		
DRAIN-SOURCE DIODE CHARACTERI	STICS						
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 23 A, T <sub>J</sub> = 25°C V <sub>GS</sub> = 0 V, I <sub>S</sub> = 23 A, T <sub>J</sub> = 150°C			0.87	1.2	V
					0.72		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dI}_{S}/\text{dt} = 300 \text{ A}/\mu\text{s,}$ $I_{S} = 12 \text{ A}$			29		ns
Reverse Recovery Charge	Q <sub>RR</sub>				61		nC
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dI}_{S}/\text{dt} = 1000 \text{ A/}\mu\text{s,}$ $I_{S} = 12 \text{ A}$			23		ns
Reverse Recovery Charge	Q <sub>RR</sub>				147		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperature

#### **TYPICAL CHARACTERISTICS**

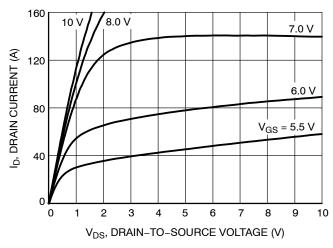


Figure 1. On-Region Characteristics

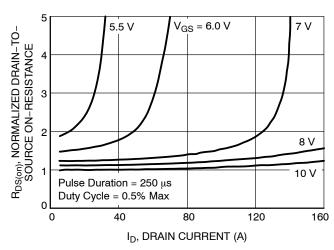


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

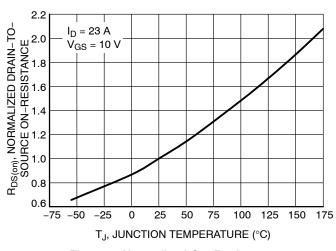


Figure 3. Normalized On–Resistance vs. Junction Temperature

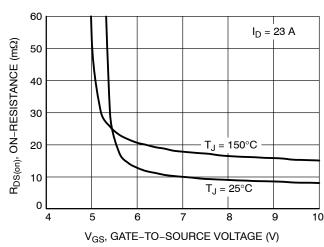


Figure 4. On-Resistance vs. Gate-to-Source Voltage

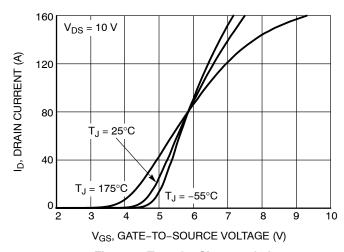


Figure 5. Transfer Characteristics

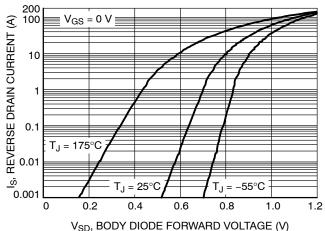


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

#### **TYPICAL CHARACTERISTICS**

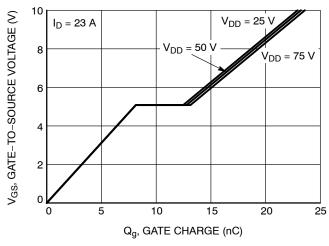


Figure 7. Gate Charge Characteristics

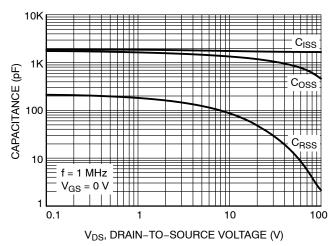


Figure 8. Capacitance vs. Drain-to-Source Voltage

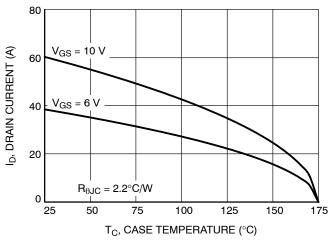


Figure 9. Drain Current vs. Case Temperature

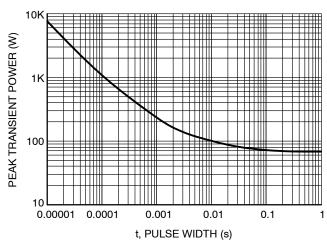


Figure 10. Peak Power

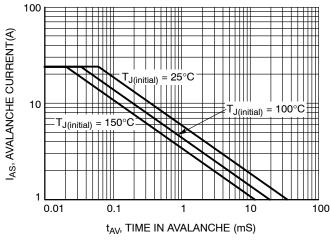


Figure 11. Unclamped Inductive Switching Capability

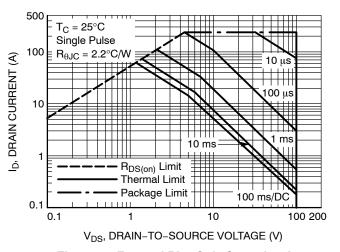


Figure 12. Forward Bias Safe Operating Area

### **TYPICAL CHARACTERISTICS**

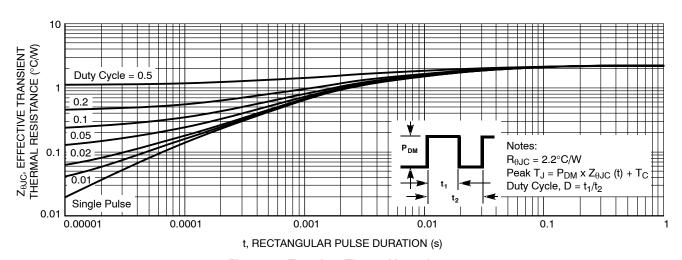
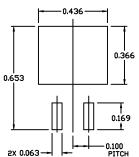


Figure 13. Transient Thermal Impedance



#### D<sup>2</sup>PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE F

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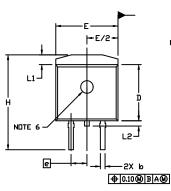
RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Table Semiconductor Manual Table 17 PROBLED

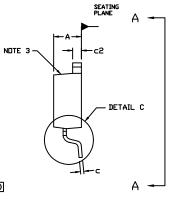
#### NOTES

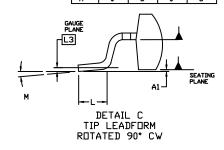
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: INCHES
- 3. CHAMFER OPTIONAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- 6. OPTIONAL MOLD FEATURE.
- 7. ①,② ... DPTIONAL CONSTRUCTION FEATURE CALL DUTS.

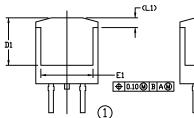
T						
	INCHES		MILLIMETERS			
DIM	MIN.	MAX.	MIN.	MAX.		
A	0.160	0.190	4.06	4.83		
A1	0.000	0.010	0.00	0.25		
b	0.020	0.039	0.51	0.99		
С	0.012	0.029	0.30	0.74		
c2	0.045	0.065	1.14	1.65		
D	0.330	0.380	8.38	9.65		
D1	0.260		6.60			
E	0.380	0.420	9.65	10.67		
E1	0.245		6.22			
e	0.100	0.100 BSC		4 BSC		
Н	0.575	0.625	14.60	15.88		
L	0.070	0.110	1.78	2.79		
L1		0.066		1.68		
L2		0.070		1.78		
L3	0.010 BSC		0.25	BSC		
м	n•	8.	n•	8.		

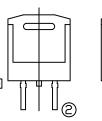


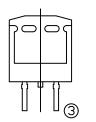
VIEW A-A

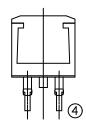








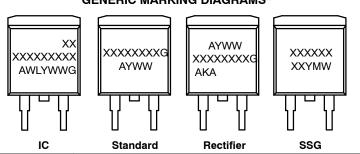




VIEW A-A

OPTIONAL CONSTRUCTIONS

## **GENERIC MARKING DIAGRAMS\***



XXXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •", may or may not be present. Some products may not follow the Generic Marking.

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D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)

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