ON Semiconductor

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Onsemi

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MOSFET - Power, N-Channel, SUPERFET[®] III, FAST

650 V, 360 mΩ, 10 A

NTD360N65S3H

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

Features

- 700 V @ $T_J = 150^{\circ}C$
- Typ. $R_{DS(on)} = 296 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 17.5 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 180 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

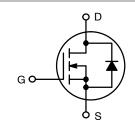
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



ON Semiconductor®

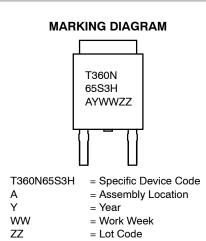
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V _{DSS}	R _{DS(ON)} MAX	I _D MAX		
650 V	360 m Ω @ 10 V	10 A		





D-PAK CASE 369AS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Parameter	Value	Unit V		
V _{DSS}	Drain to Source Voltage			650	
V _{GSS}	Gate to Source Voltage	DC	±30	V	
		AC (f > 1 Hz)	±30	V	
Ι _D	Drain Current	Continuous (T _C = 25°C)	10	А	
		Continuous (T _C = 100°C)	6		
I _{DM}	Drain Current	Pulsed (Note 1)	28	А	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		75	mJ	
I _{AS}	Avalanche Current (Note 2)		1.9	А	
E _{AR}	Repetitive Avalanche Energy (Note 1)		0.83	mJ	
dv/dt	MOSFET dv/dt		120	V/ns	
	Peak Diode Recovery dv/dt (Note 3)		20		
P _D	Power Dissipation	(T _C = 25°C)	83	W	
		Derate Above 25°C	0.66	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		260	°C	

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 1.9 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^{\circ}C$. 3. $I_{SD} \leq 5.0 \text{ A}$, di/dt $\leq 200 \text{ A}/\mu s$, $V_{DD} \leq 400 \text{ V}$, starting $T_J = 25^{\circ}C$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.51	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. Device on 1 in² pad 2 oz copper pad on 1.5×1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping [†]
NTD360N65S3H	T360N65S3H	D-PAK	330 mm	16 mm	2500 / Tape & Reel

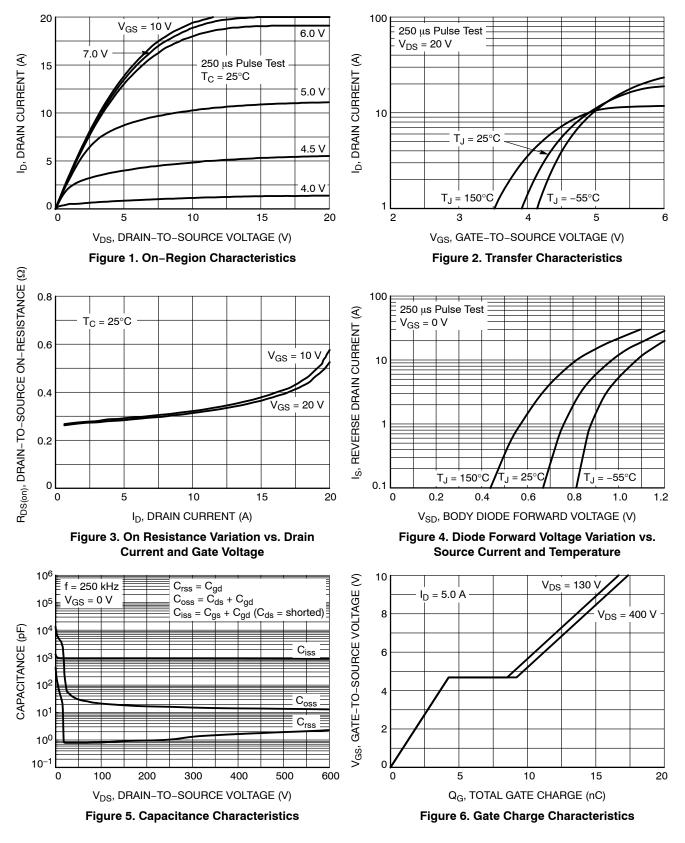
+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

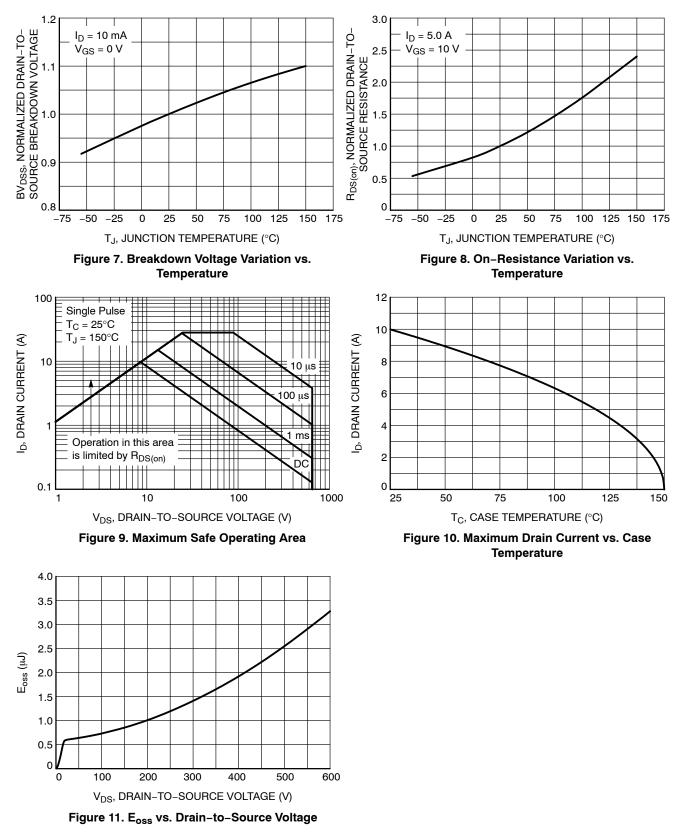
Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS	•	•			
BV _{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_{D} = 1 mA, T_{J} = 25°C	650	-	-	V
		$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 1 \text{ mA}, \text{ T}_{J} = 150^{\circ}\text{C}$	700	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.63	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	3	μA
		$V_{DS} = 520 \text{ V}, \text{ T}_{C} = 125^{\circ}\text{C}$	-	2.6	-	1
I _{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
ON CHARACTE	ERISTICS	•	-			
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 0.7$ mA	2.4	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 5.0 A	-	296	360	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 5.0 A	-	11.2	-	S
OYNAMIC CHA	RACTERISTICS	·		•		
C _{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz	-	916	-	pF
C _{oss}	Output Capacitance		-	15	-	pF
Coss(eff.)	Effective Output Capacitance	$V_{DS} = 0 V$ to 400 V, $V_{GS} = 0 V$	-	180	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	24	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V_{DS} = 400 V, I _D = 5.0 A, V _{GS} = 10 V (Note 5)	-	17.5	-	nC
Q _{gs}	Gate to Source Gate Charge		-	4.3	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	5	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.9	-	Ω
WITCHING CH	IARACTERISTICS	•	-			
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 5.0 \text{ A},$	-	15	-	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \text{ R}_{g} = 12 \Omega$ (Note 5)	-	6.7	-	ns
t _{d(off)}	Turn-Off Delay Time		-	45	-	ns
t _f	Turn-Off Fall Time		-	7	-	ns
SOURCE-DRAI	N DIODE CHARACTERISTICS	•		•	•	
۱ _S	Maximum Continuous Source to Drain Diode Forward Current		-	-	10	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		-	-	28	А
V _{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I _{SD} = 5.0 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400 \text{ V}, \text{ I}_{SD} = 5.0 \text{ A},$	-	204	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$		1.8	1	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

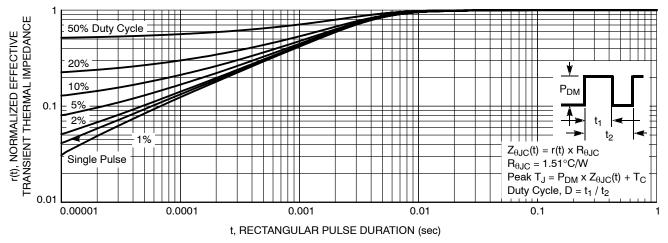


Figure 12. Transient Thermal Response Curve

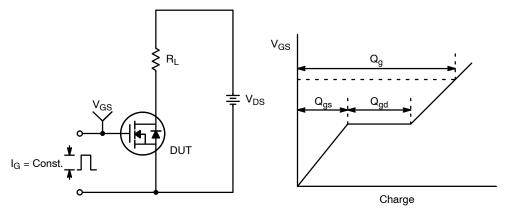


Figure 13. Gate Charge Test Circuit & Waveform

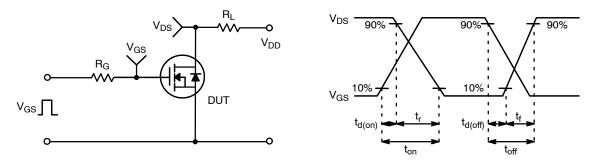


Figure 14. Resistive Switching Test Circuit & Waveforms

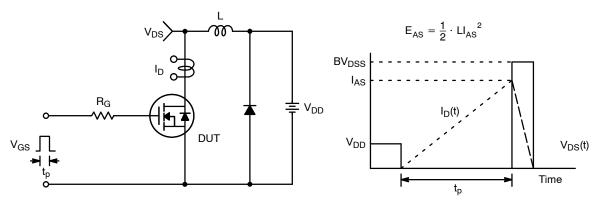


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

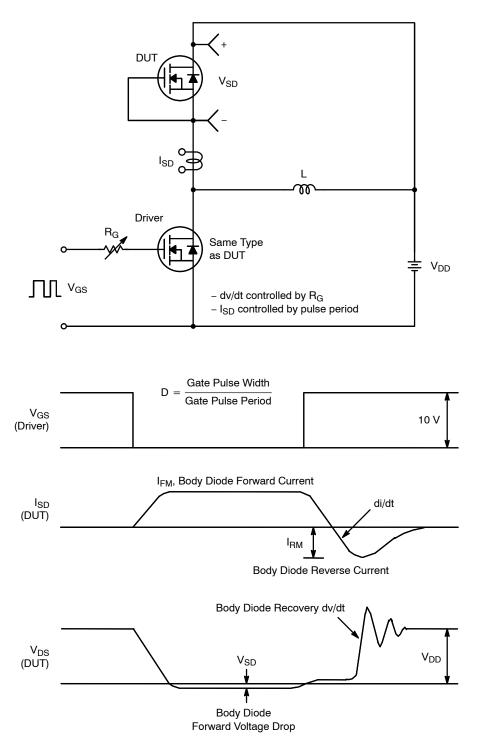
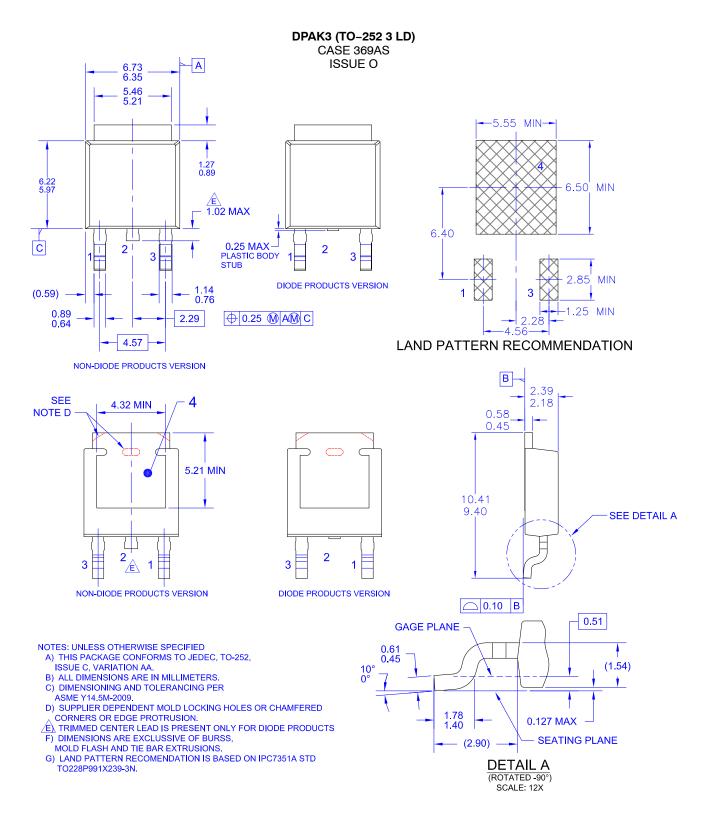


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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PACKAGE DIMENSIONS



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PUBLICATION ORDERING INFORMATION

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