Power MOSFET

30 V, 41 A, Single N-Channel, DPAK/IPAK

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Three Package Variations for Design Flexibility
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Pa	Symbol	Value	Unit		
Drain-to-Source Vo	V _{DSS}	30	V		
Gate-to-Source Vo	Gate-to-Source Voltage				V
Continuous Drain		T _A = 25°C	Ι _D	12.7	Α
Current R _{θJA} (Note 1)		T _A = 100°C		9.0	
Power Dissipation R _{θJA} (Note 1)		T _A = 25°C	P_{D}	2.56	W
Continuous Drain		T _A = 25°C	Ι _D	9.4	Α
Current R _{0JA} (Note 2)	Steady State	T _A = 100°C		6.6	
Power Dissipation R _{θJA} (Note 2)	State	T _A = 25°C	P_{D}	1.38	W
Continuous Drain		$T_C = 25^{\circ}C$	Ι _D	41	Α
Current R _{θJC} (Note 1)		T _C = 100°C		29	
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P_{D}	26.3	W
Pulsed Drain Current	t _p =10μs	T _A = 25°C	I _{DM}	150	Α
Current Limited by F	Package	T _A = 25°C	I _{DmaxPkg}	40	Α
Operating Junction Temperature	Operating Junction and Storage Temperature				
Source Current (Bo	Source Current (Body Diode)				
Drain to Source dV/	dV/dt	6.0	V/ns		
Single Pulse Drain-to-Source Avalanche Energy (T_J = 25°C, V_{DD} = 24 V, V_{GS} = 10 V, I_L = 19 A_{pk} , L = 0.1 mH, R_G = 25 Ω)			EAS	18	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

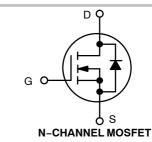
- 1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.



ON Semiconductor®

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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX	
30 V	9.0 mΩ @ 10 V	41 A	
	19 mΩ @ 4.5 V	41 A	







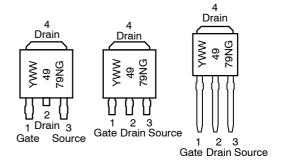


CASE 369AA **DPAK** (Bent Lead) STYLE 2

CASE 369AC 3 IPAK (Straight Lead) (Straight Lead

CASE 369D **IPAK** DPAK)

MARKING DIAGRAMS & PIN ASSIGNMENTS



= Year WW = Work Week 4979N = Device Code = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	5.7	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	4.3	
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	58.6	
Junction-to-Ambient - Steady State (Note 4)	$R_{ heta JA}$	108.6	

Drain-to-Source Breakdown Voltage V(BR)DSS VGS = 0 V, ID = 250 μA 30 V VGS = 0 V, ID = 250 μA 30 V VGS = 0 V, ID = 250 μA 30 V VGS = 0 V, ID = 250 μA 30 V VGS = 0 V, ID = 250 μA 30 V VGS = 0 V, ID = 250 μA 17 VGS = 0 V, ID = 250 μA 17 VGS = 0 V, ID = 250 μA 17 VGS = 0 V, ID = 250 μA 1.0 LO = 10 VGS = 24 V VGS	Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
Drain-to-Source Breakdown Voltage Temperature Coefficient	OFF CHARACTERISTICS							
Temperature Coefficient Temperature Coeffici	Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Sate - to - Source Leakage Current I _{GSS} V _{DS} = 0 V, V _{GS} = ±20 V ±100 nA	Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				17		mV/°C
Sate - to - Source Leakage Current I _{GSS} V _{DS} = 0 V, V _{GS} = ±20 V ±100 nA	Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1.0	
ON CHARACTERISTICS (Note 5)			V _{DS} = 24 V	T _J = 125°C			10	μΑ
Negative Threshold Voltage V _{GS(TH)} V _{GS} = V _{DS} , I _D = 250 μA 1.5 1.8 2.5 V	Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS}	_S = ±20 V			±100	nA
Negative Threshold Temperature VGS(TH)/TJ	ON CHARACTERISTICS (Note 5)							
Coefficient Mode Invited By Section By Se	Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D}$	= 250 μΑ	1.5	1.8	2.5	٧
ID = 15 A 6.9 MS VGS = 4.5 V ID = 30 A 13.6 19 MS ID = 15 A 13.2 MS ID = 15 A 13.6 19 MS ID = 15 A ID =	Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				4.5		mV/°C
VGS = 4.5 V ID = 30 A 13.6 19 ID = 15 A 13.2	Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A		6.9	9.0	
VGS = 4.5 V ID = 30 A 13.6 19				I _D = 15 A		6.9		
Forward Transconductance g_{FS} $V_{DS} = 1.5 \text{ V}, I_D = 30 \text{ A}$ 36 S $CHARGES, CAPACITANCES AND GATE RESISTANCE$ Input Capacitance C_{ISS} Output Capacitance C_{OSS} Reverse Transfer Capacitance C_{RSS} Total Gate Charge $Q_{G(TOT)}$ Threshold Gate Charge Q_{GS} Gate-to-Drain Charge Q_{GD} Total Gate Charge Q_{GTOT} Total Gate Charge Q_{GTOT} Total Gate Charge Q_{GS} Q_{GS} Q_{GTOT} Q_{GS}			V _{GS} = 4.5 V	I _D = 30 A		13.6	19	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE Input Capacitance C _{ISS} Output Capacitance C _{OSS} Reverse Transfer Capacitance C _{RSS} Total Gate Charge Q _{G(TOT)} Threshold Gate Charge Q _{G(TH)} Gate-to-Source Charge Q _{GS} Gate-to-Drain Charge Q _{GD} Total Gate Charge Q _G Gate-to-Drain Charge Q _G Total Gate Charge Q _{G(TOT)} V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A 16.5 NC SWITCHING CHARACTERISTICS (Note 6) Turn-On Delay Time t _r Rise Time t _r V _{GS} = 4.5 V, V _{DS} = 15 V, V _{DS}				I _D = 15 A		13.2		1
Input Capacitance	Forward Transconductance	9FS	V _{DS} = 1.5 V, I	_D = 30 A		36		S
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	CHARGES, CAPACITANCES AND GATE	RESISTANCE						
Reverse Transfer Capacitance C_{RSS} 180 Total Gate Charge $Q_{G(TOT)}$ Threshold Gate Charge $Q_{G(TH)}$ Gate—to—Source Charge Q_{GS} Gate—to—Drain Charge Q_{GD} Total Gate Charge Q_{GD} Total Gate Charge Q_{GTOT} Turn—On Delay Time Q_{GTOT} Rise Time Q_{GS} Turn—On Delay Time Q_{GTOT} Tur	Input Capacitance	C _{ISS}				837		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = 1.0 M	Hz, V _{DS} = 15 V		347		pF
Threshold Gate Charge $Q_{G(TH)}$ Gate—to—Source Charge Q_{GS} Gate—to—Drain Charge Q_{GD} Total Gate Charge $Q_{G(TOT)}$ $Q_{G(TOT)}$ $Q_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}, I_{D} = 30 \text{ A}$ 1.42 1.42 1.42 1.42 1.42 1.42 1.48 Total Gate Charge $Q_{G(TOT)}$ SWITCHING CHARACTERISTICS (Note 6) Turn—On Delay Time $t_{d(ON)}$ Rise Time t_{r} $V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}, V_{DS} $	Reverse Transfer Capacitance	C _{RSS}				180		1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Total Gate Charge	Q _{G(TOT)}				9.0		
Gate-to-Source Charge Q _{GS} 2.8 Gate-to-Drain Charge Q _{GD} 4.8 Total Gate Charge Q _G (TOT) V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A 16.5 nC SWITCHING CHARACTERISTICS (Note 6) Turn-On Delay Time t _d (ON) 10 10 Rise Time t _r V _{GS} = 4.5 V, V _{DS} = 15 V,	Threshold Gate Charge	Q _{G(TH)}	V 45.V.V	45.77.1 00.4		1.42		nC
Total Gate Charge $Q_{G(TOT)}$ $V_{GS} = 10 \text{ V}, V_{DS} = 15 \text{ V}, I_D = 30 \text{ A}$ 16.5 nC SWITCHING CHARACTERISTICS (Note 6) Turn-On Delay Time $t_{d(ON)}$ 10 Rise Time t_r $V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}, 27$ ns	Gate-to-Source Charge	Q _{GS}	$V_{GS} = 4.5 \text{ V}, V_{DS} =$	15 V, I _D = 30 A		2.8		
SWITCHING CHARACTERISTICS (Note 6) Turn-On Delay Time t _{d(ON)} 10 Rise Time t _r V _{GS} = 4.5 V, V _{DS} = 15 V, 27	Gate-to-Drain Charge	Q_{GD}				4.8		1
Turn–On Delay Time $ \begin{matrix} t_{d(ON)} \\ \hline \\ Rise Time \end{matrix} $	Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A			16.5		nC
Rise Time t _r V _{GS} = 4.5 V, V _{DS} = 15 V,	SWITCHING CHARACTERISTICS (Note	6)						
V _{GS} = 4.5 V, V _{DS} = 15 V,	Turn-On Delay Time	t _{d(ON)}				10		
Turn–Off Delay Time $t_{d(OFF)}$ $I_D = 15 \text{ A}, R_G = 3.0 \Omega$ 13.3	Rise Time	t _r	$V_{GS} = 4.5 \text{ V, V}_{I}$	_{os} = 15 V,		27		1
	Turn-Off Delay Time	t _{d(OFF)}	$I_D = 15 \text{ A}, R_G = 3.0 \Omega$			13.3		d ns

^{5.} Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%.

Fall Time

Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
 Surface-mounted on FR4 board using the minimum recommended pad size.

^{6.} Switching characteristics are independent of operating junction temperatures.
7. Assume terminal length of 110 mils.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (Note	e 6)						
Turn-On Delay Time	t _{d(ON)}				6.5		
Rise Time	t _r	V _{GS} = 10 V, V _{DS}	V_{GS} = 10 V, V_{DS} = 15 V, I_{D} = 15 A, R_{G} = 3.0 Ω		20.2		
Turn-Off Delay Time	t _{d(OFF)}	I _D = 15 A, R _G =	= 3.0 Ω		17.2		ns
Fall Time	t _f				4.2		
DRAIN-SOURCE DIODE CHARACTER	ISTICS						
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 \text{ V}.$ $T_J = 25^{\circ}\text{C}$			0.91	1.1	.,
		$V_{GS} = 0 \text{ V},$ $I_S = 30 \text{ A}$ $I_J = 25^{\circ}\text{C}$ $T_J = 125^{\circ}\text{C}$	T _J = 125°C		0.82		V
Reverse Recovery Time	t _{RR}	<u> </u>			20.8		
Charge Time	t _a	V _{GS} = 0 V, dIS/dt =	= 100 A/μs,		9.8		ns
Discharge Time	t _b	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 30 \text{ A}$			11		
Reverse Recovery Charge	Q _{RR}				8.0		nC
PACKAGE PARASITIC VALUES							
Source Inductance (Note 7)	L _S				2.85		nΗ
Drain Inductance, DPAK	L _D	T _A = 25°C			0.0164		
Drain Inductance, IPAK (Note 7)	L _D				1.88		
Gate Inductance (Note 7)	L _G				4.9		
Gate Resistance	R_{G}				1.0	2.2	Ω

- 5. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.
 6. Switching characteristics are independent of operating junction temperatures.
 7. Assume terminal length of 110 mils.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD4979NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4979N-1G	IPAK (Pb-Free)	75 Units / Rail
NTD4979N-35G	IPAK Trimmed Lead (Pb-Free)	75 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL PERFORMANCE CURVES

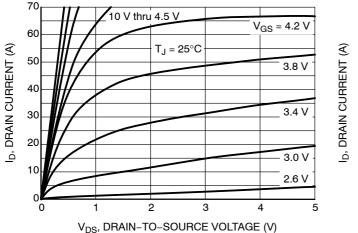
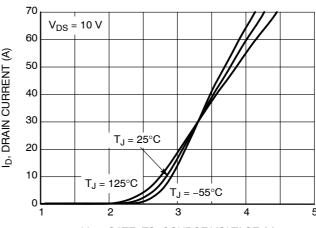


Figure 1. On-Region Characteristics



V_{GS}, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics

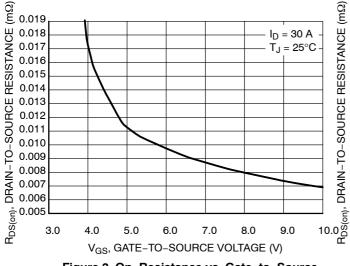


Figure 3. On-Resistance vs. Gate-to-Source Voltage

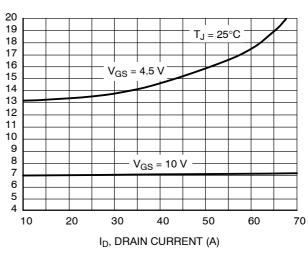


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

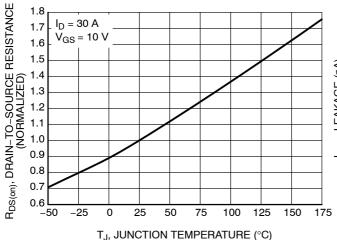


Figure 5. On–Resistance Variation with Temperature

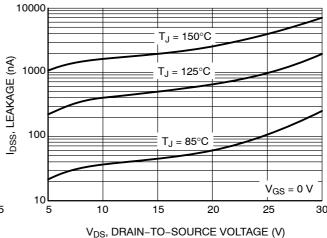
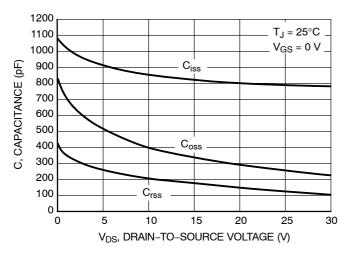


Figure 6. Drain-to-Source Leakage Current vs. Voltage

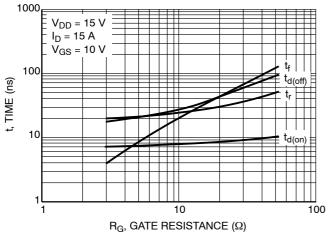
TYPICAL PERFORMANCE CURVES



V_{GS}, GATE-TO-SOURCE VOLTAGE (V) Q_T 9 8 7 6 5 \overline{Q}_{gr} Q_{gs} 4 3 $I_D = 30 A$ $T_J = 25^{\circ}C$ 2 $V_{DD} = 15 V$ $V_{GS} = 10 A$ 0 0 2 3 8 9 10 11 12 13 14 15 16 17 18 Q_G, TOTAL GATE CHARGE (nC)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge



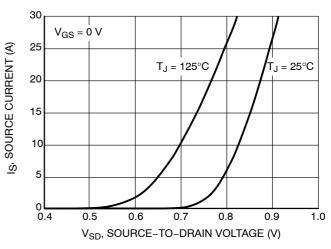
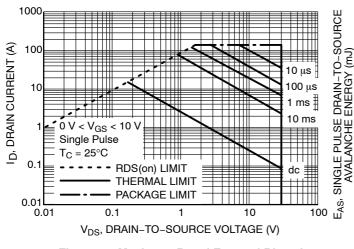


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current



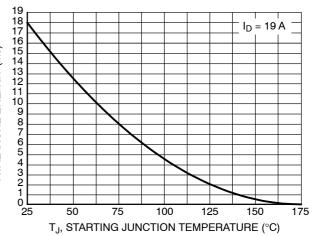


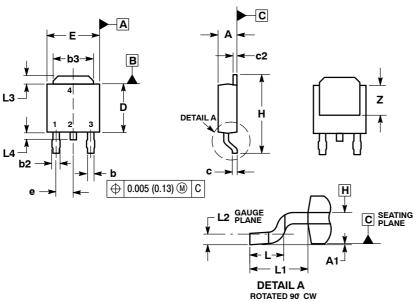
Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)

CASE 369AA **ISSUE B**



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: INCHES.

 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

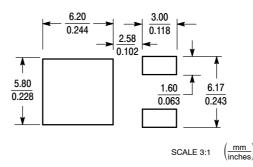
 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.030	0.045	0.76	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
Е	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29	BSC	
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.108	REF	2.74 REF		
L2	0.020	BSC	0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
7	0 155		3.93		

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE

- 4. DRAIN

SOLDERING FOOTPRINT*

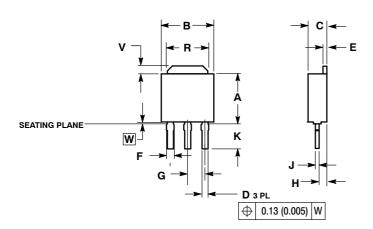


^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD

CASE 369AC ISSUE O

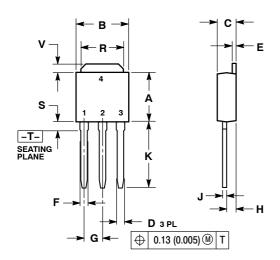


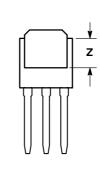
NOTES

- 1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- SEATING PLANE IS ON TOP OF DAMBAR POSITION.
- DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INC	HES	MILLIN	ETERS
DIM	MIN MAX		MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090	BSC	2.29 BSC	
Н	0.034	0.040	0.87	1.01
7	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
٧	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

IPAK CASE 369D **ISSUE C**





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090	BSC	2.29 BSC		
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
K	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

STYLE 2:

PIN 1. GATE 2. DRAIN

- SOURCE DRAIN

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