

# NTGD3148N

## MOSFET – Power, Dual, N-Channel, TSOP-6

**20 V, 3.5 A**

### Features

- Low Threshold Levels,  $V_{GS(th)} < 1.5\text{ V}$
- Low Gate Charge (3.8 nC)
- Leading Edge Trench Technology of Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- This is a Pb-Free Device

### Applications

- DC-DC Converters (Buck and Boost Circuits)
- Low Side Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment Like Cell Phones, DSCs, Media Player, Etc
- Battery Charging and Protection Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	20	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 12$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	3.0	A
			$T_A = 85^\circ\text{C}$	2.2	
Continuous Drain Current (Note 1)	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	$I_D$	3.5	A
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	0.9	W
	$t \leq 5\text{ s}$			1.1	
Pulsed Drain Current		$t_p = 10\ \mu\text{s}$	$I_{DM}$	10	A
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-50 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	0.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	140	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	110	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

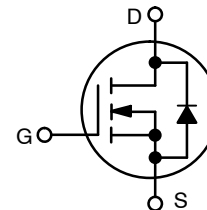


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### N-CHANNEL MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ Max
20 V	70 m $\Omega$ @ 4.5 V	3.5 A
	100 m $\Omega$ @ 2.5 V	

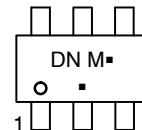


N-CHANNEL MOSFET



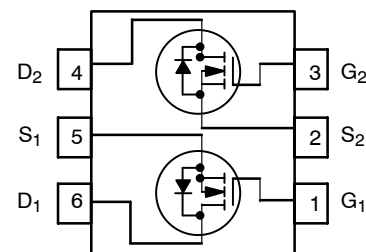
TSOP-6  
CASE 318G  
STYLE 13

### MARKING DIAGRAM



DN = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN CONNECTION



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NTGD3148N

## MOSFET ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, Ref to 25°C		12.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 16 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			100	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	0.5		1.5	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.28		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.5 A		41.7	70	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2.8 A		58	100	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 3.5 A		6.2		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 10 V		300		pF
Output Capacitance	C <sub>OSS</sub>			73		
Reverse Transfer Capacitance	C <sub>RSS</sub>			44		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A		3.8		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.3		
Gate-to-Source Charge	Q <sub>GS</sub>			0.7		
Gate-to-Drain Charge	Q <sub>GD</sub>			1.1		
Gate Resistance	R <sub>G</sub>			2.8		Ω

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A, R <sub>G</sub> = 3.0 Ω		7.4		ns
Rise Time	t <sub>r</sub>			11.2		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			12.8		
Fall Time	t <sub>f</sub>			1.6		

### DRAIN-TO-SOURCE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 0.8 A	T <sub>J</sub> = 25°C		0.71	V
			T <sub>J</sub> = 125°C		0.57	
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, d <sub>I</sub> S/d <sub>t</sub> = 100 A/μs, I <sub>S</sub> = 0.8 A		9.0		ns
Charge Time	T <sub>a</sub>			5.0		
Discharge Time	T <sub>b</sub>			4.0		
Reverse Recovery Time	Q <sub>RR</sub>				2.5	

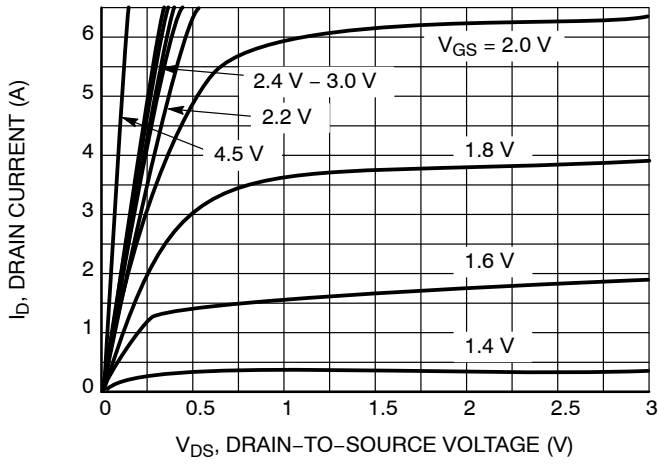
- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

### ORDERING INFORMATION

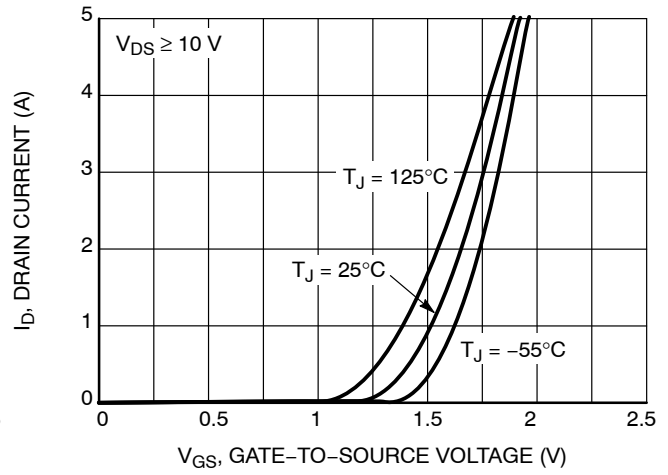
Device	Package	Shipping <sup>†</sup>
NTGD3148NT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

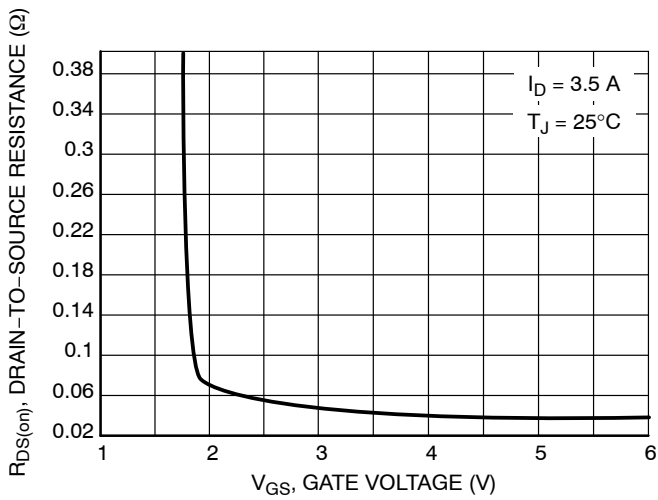
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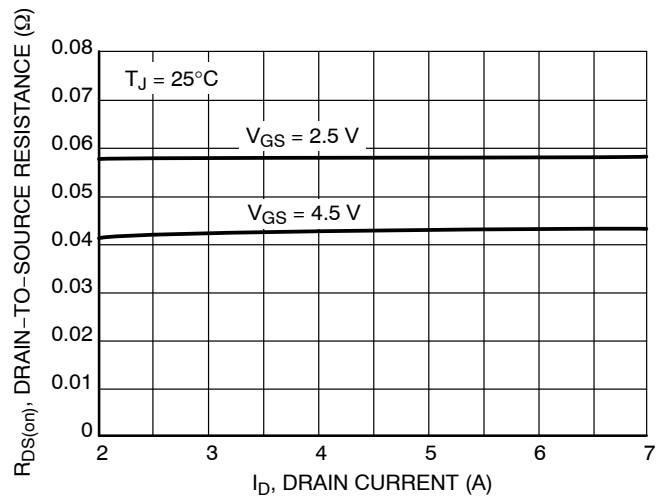
**Figure 1. On-Region Characteristics**



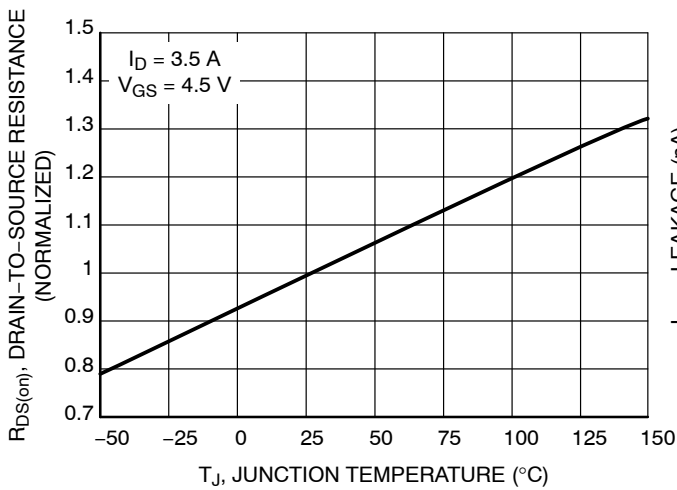
**Figure 2. Transfer Characteristics**



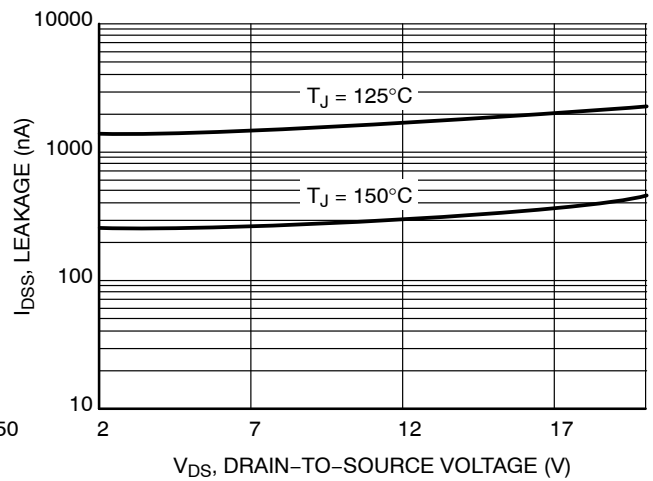
**Figure 3. On-Resistance vs. Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

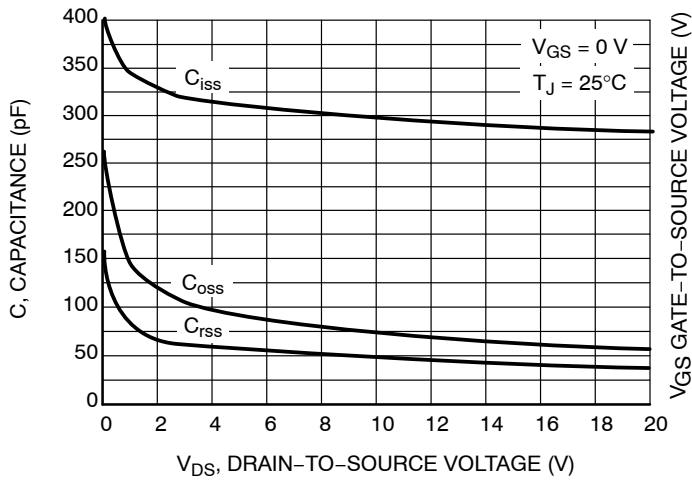


**Figure 5. On-Resistance Variation vs. Temperature**

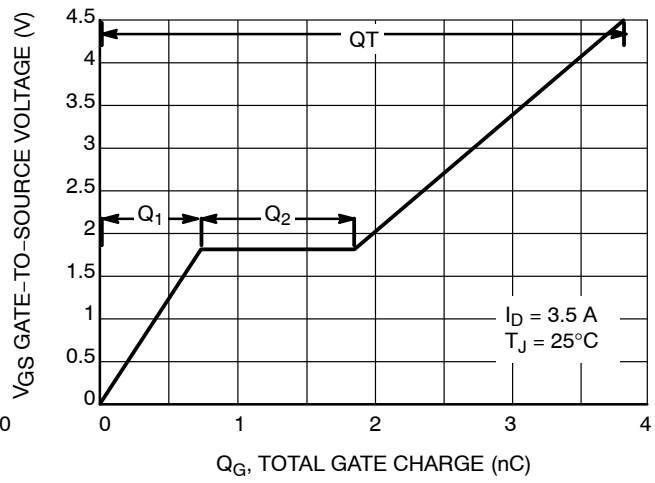


**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

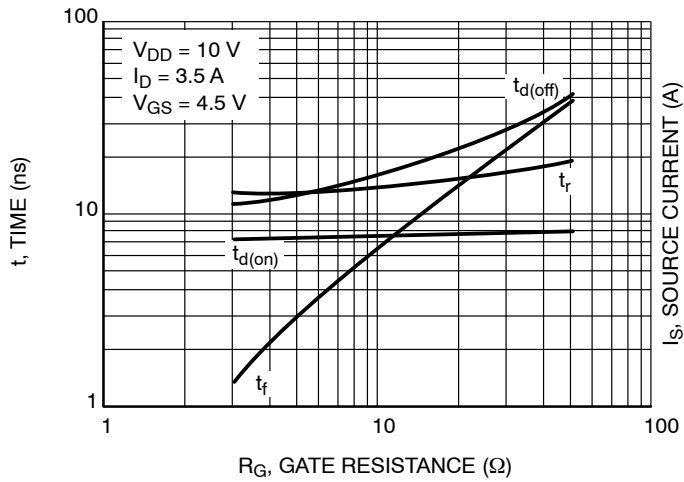
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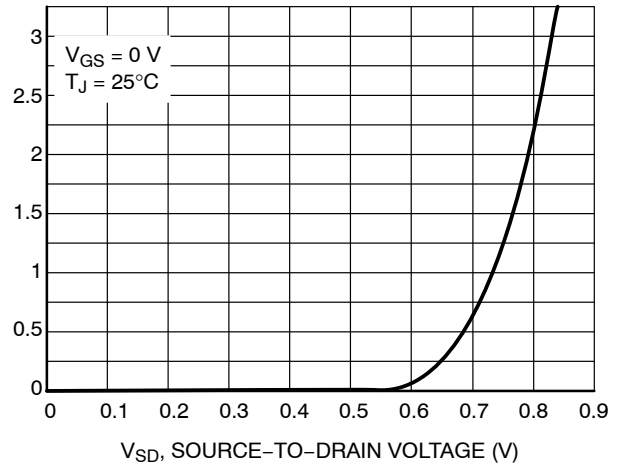
**Figure 7. Capacitance Variation**



**Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge**



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

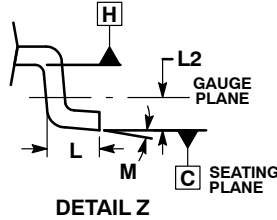
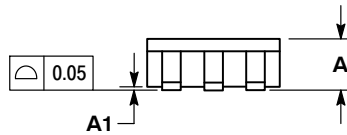
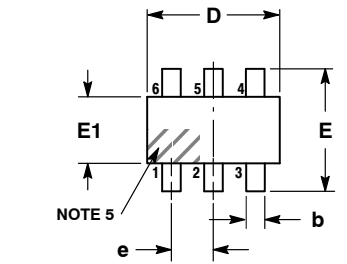
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SCALE 2:1

### TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



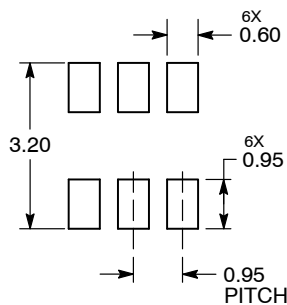
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- |  |  |   |   |   |  |
|--|--|---|---|---|--|
| <p>STYLE 1:<br/>PIN 1. DRAIN<br/>2. DRAIN<br/>3. GATE<br/>4. SOURCE<br/>5. DRAIN<br/>6. DRAIN</p>              | <p>STYLE 2:<br/>PIN 1. EMITTER 2<br/>2. BASE 1<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 2<br/>6. COLLECTOR 2</p>    | <p>STYLE 3:<br/>PIN 1. ENABLE<br/>2. N/C<br/>3. R BOOST<br/>4. Vz<br/>5. V in<br/>6. V out</p>                            | <p>STYLE 4:<br/>PIN 1. N/C<br/>2. V in<br/>3. NOT USED<br/>4. GROUND<br/>5. ENABLE<br/>6. LOAD</p>                | <p>STYLE 5:<br/>PIN 1. EMITTER 2<br/>2. BASE 2<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 1<br/>6. COLLECTOR 2</p> | <p>STYLE 6:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. EMITTER<br/>5. COLLECTOR<br/>6. COLLECTOR</p> |
| <p>STYLE 7:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. N/C<br/>5. COLLECTOR<br/>6. EMITTER</p>   | <p>STYLE 8:<br/>PIN 1. Vbus<br/>2. D(in)<br/>3. D(in)+<br/>4. D(out)+<br/>5. D(out)<br/>6. GND</p>                         | <p>STYLE 9:<br/>PIN 1. LOW VOLTAGE GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN<br/>5. DRAIN<br/>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:<br/>PIN 1. D(OUT)+<br/>2. GND<br/>3. D(OUT)-<br/>4. D(IN)-<br/>5. VBUS<br/>6. D(IN)+</p>             | <p>STYLE 11:<br/>PIN 1. SOURCE 1<br/>2. DRAIN 2<br/>3. DRAIN 2<br/>4. SOURCE 2<br/>5. GATE 1<br/>6. DRAIN 1/GATE 2</p>  | <p>STYLE 12:<br/>PIN 1. I/O<br/>2. GROUND<br/>3. I/O<br/>4. I/O<br/>5. VCC<br/>6. I/O</p>                          |
| <p>STYLE 13:<br/>PIN 1. GATE 1<br/>2. SOURCE 2<br/>3. GATE 2<br/>4. DRAIN 2<br/>5. SOURCE 1<br/>6. DRAIN 1</p> | <p>STYLE 14:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. CATHODE/DRAIN<br/>5. CATHODE/DRAIN<br/>6. CATHODE/DRAIN</p> | <p>STYLE 15:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. DRAIN<br/>5. N/C<br/>6. CATHODE</p>                        | <p>STYLE 16:<br/>PIN 1. ANODE/CATHODE<br/>2. BASE<br/>3. EMITTER<br/>4. COLLECTOR<br/>5. ANODE<br/>6. CATHODE</p> | <p>STYLE 17:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. ANODE/CATHODE<br/>4. ANODE<br/>5. CATHODE<br/>6. COLLECTOR</p>       |  |

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



- |  |   |
|--|---|
| <p>XXX = Specific Device Code<br/>A = Assembly Location<br/>Y = Year<br/>W = Work Week<br/>▪ = Pb-Free Package</p> | <p>XXX = Specific Device Code<br/>M = Date Code<br/>▪ = Pb-Free Package</p> |
|--|---|

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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