MOSFET – Power, N-Channel, SUPERFET III, FRFET

650 V, 75 A, 27.4 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ $T_J = 150^{\circ}C$
- Typ. $R_{DS(on)} = 23 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 259 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 1972 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

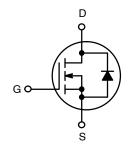
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



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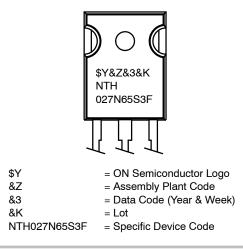
V _{DSS}	R _{DS(ON)} MAX	I _D MAX		
650 V	27.4 m Ω @ 10 V	75 A		



POWER MOSFET



MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Parameter	NTH027N65S3F-F155	Unit V	
V _{DSS}	Drain to Source Voltage			650
V _{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
ID	Drain Current	– Continuous (T _C = 25°C)	75	А
		– Continuous (T _C = 100°C)	60	
I _{DM}	Drain Current	– Pulsed (Note 1)	187.5	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		1610	mJ
I _{AS}	Avalanche Current (Note 2)		15	А
E _{AR}	Repetitive Avalanche Energy (Note 1)		5.95	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P _D	Power Dissipation	(T _C = 25°C)	595	W
		- Derate Above 25°C	4.76	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 15 \text{ A}, \text{ R}_{G} = 25 \Omega$, starting $T_{J} = 25^{\circ}\text{C}$. 3. $I_{SD} \leq 37.5 \text{ A}, \text{ di/dt} \leq 200 \text{ A/}\mu\text{s}, \text{V}_{DD} \leq 400 \text{ V}$, starting $T_{J} = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	NTH027N65S3F-F155	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTH027N65S3F-F155	NTH027N65S3F	TO-247	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
OFF CHARACT	ERISTICS	•				
BV _{DSS} Drain to Source Break	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 1 \text{ mA}, \text{ T}_{J} = 25^{\circ}\text{C}$	650	-	-	V
		$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 1 \text{ mA}, \text{ T}_{J} = 150^{\circ}\text{C}$	700	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 15 mA, Referenced to 25°C	-	0.61	_	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μΑ
		V_{DS} = 520 V, T_{C} = 125°C	-	361	-	
I _{GSS}	Gate to Body Leakage Current	$V_{GS}=\pm30~\text{V},~V_{DS}=0~\text{V}$	-	-	±100	nA
ON CHARACTE	RISTICS	•				
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.0 \text{ mA}$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 35 A	-	23	27.4	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 37.5 A	-	56	-	S
DYNAMIC CHAI	RACTERISTICS	•		•		
C _{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	-	7690	-	pF
C _{oss}	Output Capacitance		-	200	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	1972	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	352	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 37.5 A, V _{GS} = 10 V (Note 4)	-	259	-	nC
Q _{gs}	Gate to Source Gate Charge		-	72	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	99	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1.2	-	Ω
SWITCHING CH	IARACTERISTICS	•				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, \text{ I}_{D} = 37.5 \text{ A}, \text{ V}_{GS} = 10 \text{ V}$	-	49	-	ns
t _r	Turn-On Rise Time	R _g = 2 Ω (Note 4)	-	47	-	ns
t _{d(off)}	Turn-Off Delay Time		-	131	-	ns
t _f	Turn-Off Fall Time	1	-	34	-	ns
SOURCE-DRAII	N DIODE CHARACTERISTICS					
۱ _S	Maximum Continuous Source to Drain Diode Forward Current			-	75	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			-	187.5	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 37.5 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 37.5 A,	-	168	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/µs	-	1014	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

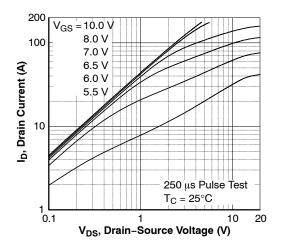
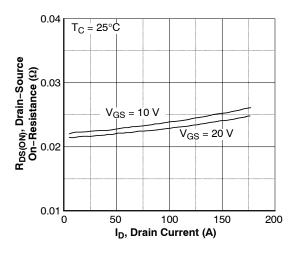
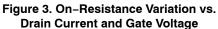


Figure 1. On-Region Characteristics





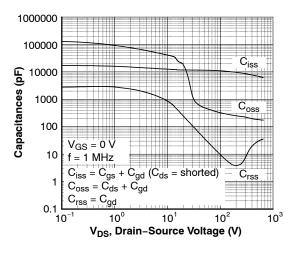


Figure 5. Capacitance Characteristics

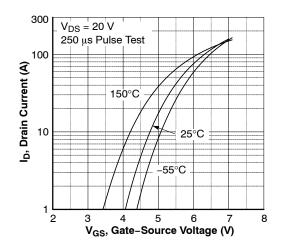
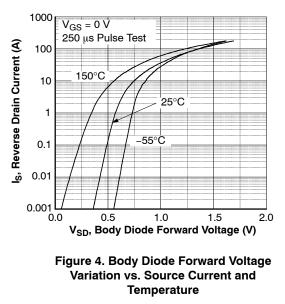


Figure 2. Transfer Characteristics



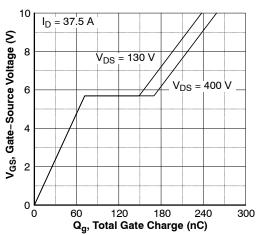
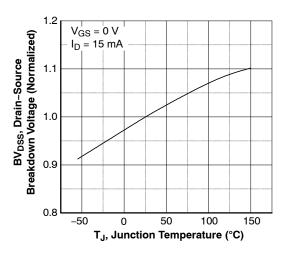
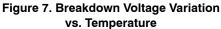


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)





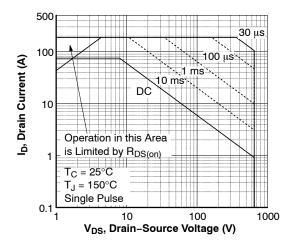


Figure 9. Maximum Safe Operating Area

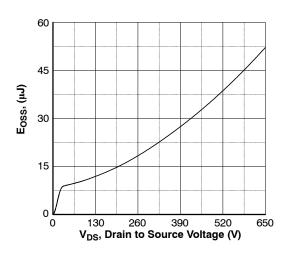


Figure 11. E_{OSS} vs. Drain to Source Voltage

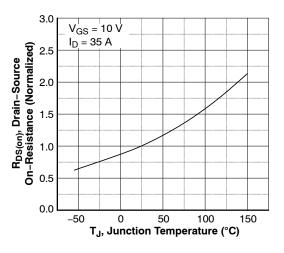


Figure 8. On–Resistance Variation vs. Temperature

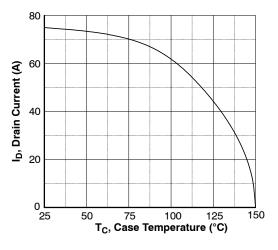


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

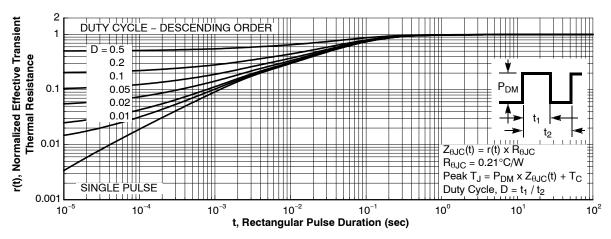
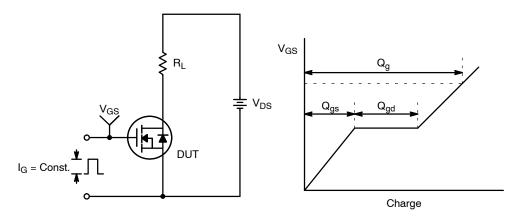


Figure 12. Transient Thermal Response Curve





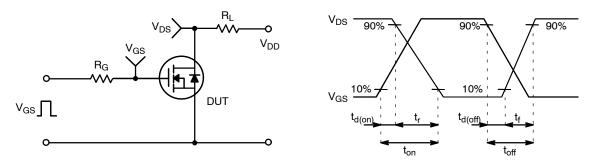
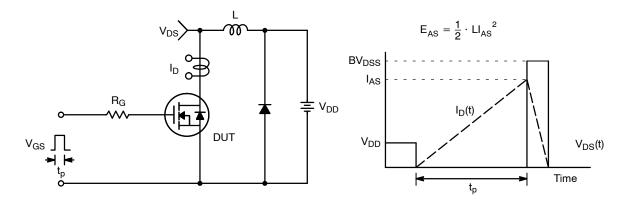


Figure 14. Resistive Switching Test Circuit & Waveforms





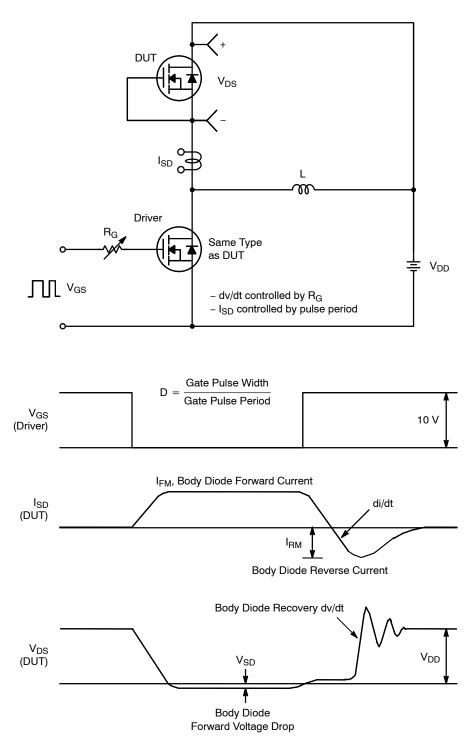
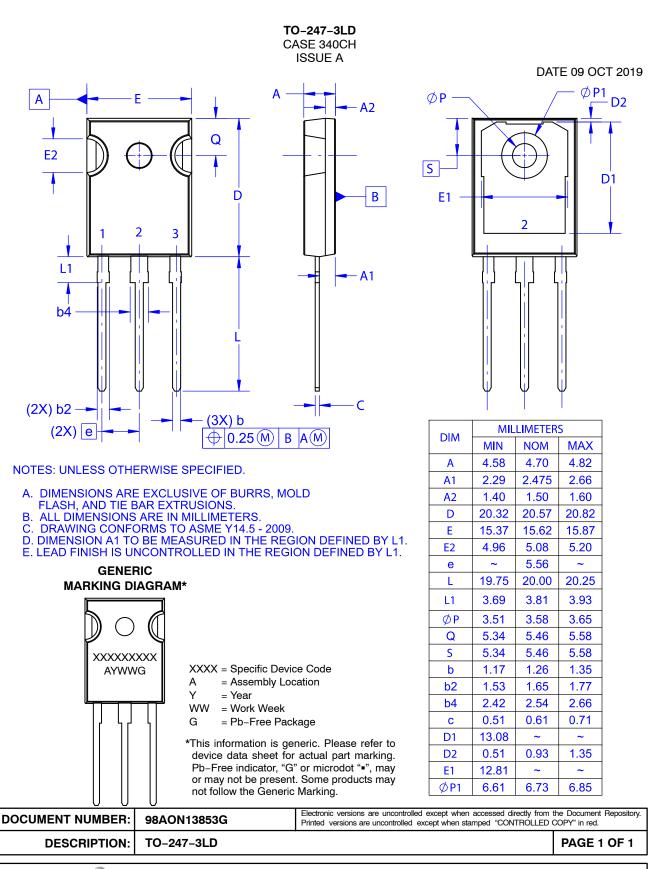


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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