NTLLD4901NF

MOSFET – Power, Dual, N-Channel with Integrated Schottky WDFN, (3 mm x 3 mm)

30 V, High Side 11 A / Low Side 13 A

Features

- Co−Packaged Power Stage Solution to Minimize Board Space
- Low Side MOSFET with Integrated Schottky
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

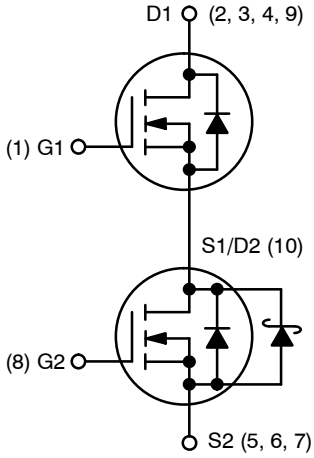
Applications

- DC−DC Converters
- System Voltage Rails
- Point of Load

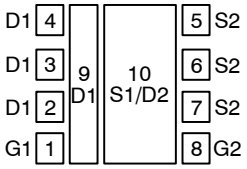
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1 Top FET 30 V	17.4 mΩ @ 10 V	11 A
	25 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	13.3 mΩ @ 10 V	13 A
	20 mΩ @ 4.5 V	



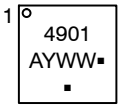
PIN CONNECTIONS



(Bottom View)

MARKING DIAGRAM

WDFN8
CASE 511BP



4901	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter				Symbol	Value	Unit
Drain−to−Source Voltage			Q1	V_{DSS}	30	V
Drain−to−Source Voltage			Q2			
Gate−to−Source Voltage			Q1	V_{GS}	±20	V
Gate−to−Source Voltage			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	Q1	I_D	8.3	A
		T_A = 85°C			6.0	
		T_A = 25°C	Q2		9.6	
		T_A = 85°C			6.9	
Power Dissipation RθJA (Note 1)		T_A = 25°C	Q1	P_D	1.82	W
			Q2		1.88	
Continuous Drain Current $R_{\theta JA} \le 10$ s (Note 1)		T_A = 25°C	Q1	I_D	11	A
		T_A = 85°C			8	
		T_A = 25°C	Q2		13	
		T_A = 85°C			9.1	
Power Dissipation $R_{\theta JA} \le 10$ s (Note 1)		T_A = 25°C	Q1	P_D	3.23	W
			Q2		3.27	
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	Q1	I_D	5.5	A
		T_A = 85°C			4.0	
		T_A = 25°C	Q2		6.3	
		T_A = 85°C			4.5	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25 °C	Q1	P_D	0.80	W
			Q2		0.81	
Pulsed Drain Current		TA = 25°C tp = 10 μs	Q1	I_{DM}	65	A
			Q2		70	
Operating Junction and Storage Temperature			Q1	T_J, T_{STG}	−55 to +150	°C
			Q2			
Source Current (Body Diode)			Q1	I_S	4.2	A
			Q2		6.0	
Drain to Source DV/DT				dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 9.0 A_{pk}, L = 0.3 mH, R_G = 25 Ω)			Q1	EAS	12	mJ
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 9.5 A_{pk}, L = 0.3 mH, R_G = 25 Ω)			Q2	EAS	13.5	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)				T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu
2. Surface−mounted on FR4 board using the minimum recommended pad size of 90 mm^2

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	FET	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 3)	Q1	$R_{\theta JA}$	68.8	°C/W
	Q2		66.4	
Junction−to−Ambient − Steady State (Note 4)	Q1	$R_{\theta JA}$	156.4	
	Q2		153.9	
Junction−to−Ambient − (t ≤ 10 s) (Note 3)	Q1	$R_{\theta JA}$	38.7	
	Q2		38.2	

3. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu
4. Surface−mounted on FR4 board using the minimum recommended pad size of 90 mm^2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	Q1	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
	Q2				30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	Q1	$V_{(BR)DSS}$ / T_J				18		mV / °C
	Q2					15		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1	μA
				T_J = 125°C			10	
	Q2		V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			500	
Gate−to−Source Leakage Current	Q1	I_{GSS}	V_{GS} = 0 V, VDS = ±20 V				±100	nA
	Q2						±100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	Q1	$V_{GS(TH)}$	V_{GS} = VDS, I_D = 250 μA		1.2		2.2	V
	Q2				1.2		2.2	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)}$ / T_J				4.5		mV / °C
	Q2					4.0		
Drain−to−Source On Resistance	Q1	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 9 A		14	17.4	mΩ
			V_{GS} = 4.5 V	I_D = 9 A		20	25	
	Q2		V_{GS} = 10 V	I_D = 11 A		11	13.3	
			V_{GS} = 4.5 V	I_D = 11 A		16	20	
Forward Transconductance	Q1	g_{FS}	V_{DS} = 1.5 V, I_D = 9 A			16		S
	Q2					18		
CHARGES, CAPACITANCES & GATE RESISTANCE								
Input Capacitance	Q1	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			605		pF
	Q2					660		
Output Capacitance	Q1	C_{OSS}				190		
	Q2					325		
Reverse Capacitance	Q1	C_{RSS}				102		
	Q2					17.5		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 9 A		6.5		nC
	Q2				5.0		
Threshold Gate Charge	Q1	$Q_{G(TH)}$			1.1		
	Q2				1.1		
Gate−to−Source Charge	Q1	Q_{GS}			1.9		
	Q2				2.0		
Gate−to−Drain Charge	Q1	Q_{GD}			3.2		
	Q2				1.46		
Total Gate Charge	Q1	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 9 A		12		nC
	Q2				10.6		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 9 A, R_G = 3.0 Ω		8.0		ns
	Q2				7.5		
Rise Time	Q1	t_r			7.2		
	Q2				11.2		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			11		
	Q2				11.6		
Fall Time	Q1	t_f			3.3		
	Q2				1.9		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	Q1	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 9 A, R_G = 3.0 Ω		4.2		ns
	Q2				4.3		
Rise Time	Q1	t_r			11.6		
	Q2				11.4		
Turn−Off Delay Time	Q1	$t_{d(OFF)}$			14.1		
	Q2				14.3		
Fall Time	Q1	t_f			2.0		
	Q2				1.3		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Voltage	Q1	V_{SD}	V_{GS} = 0 V, I_S = 3 A; T_J = 25°C		0.80	1.2	V
			V_{GS} = 0 V, I_S = 3 A; T_J = 125°C		0.65		
	Q2		V_{GS} = 0 V, I_S = 2 A; T_J = 25°C		0.50	0.80	
			V_{GS} = 0 V, I_S = 2 A; T_J = 125°C		0.45		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 3 A		17.9		ns
	Q2				23.3		
Charge Time	Q1	ta			9.0		
	Q2				11.3		
Discharge Time	Q1	tb			9.0		
	Q2				12		
Reverse Recovery Charge	Q1	Q_{RR}			8.0		nC
	Q2				12		
PACKAGE PARASITIC VALUES							
Source Inductance	Q1	L_S	T_A = 25°C		0.36		nH
	Q2				0.36		
Drain Inductance	Q1	L_D			0.054		nH
	Q2				0.054		
Gate Inductance	Q1	L_G			1.3		nH
	Q2				1.3		
Gate Resistance	Q1	R_G			0.8		Ω
	Q2				0.8		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTLLD4901NFTWG	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

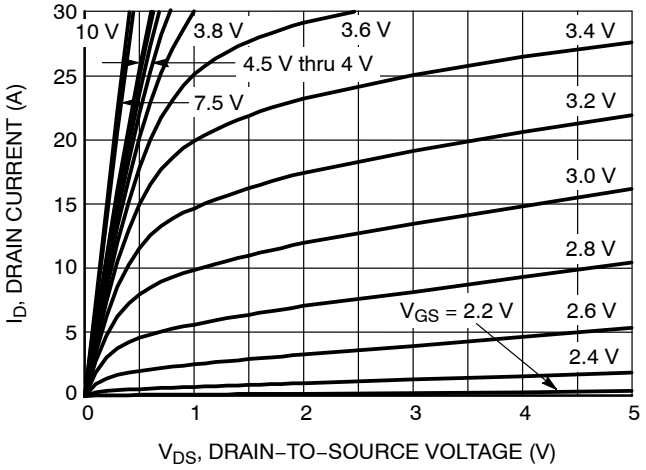


Figure 1. On−Region Characteristics

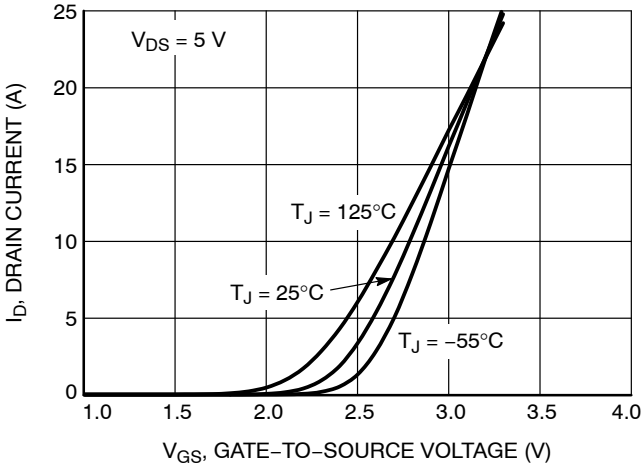


Figure 2. Transfer Characteristics

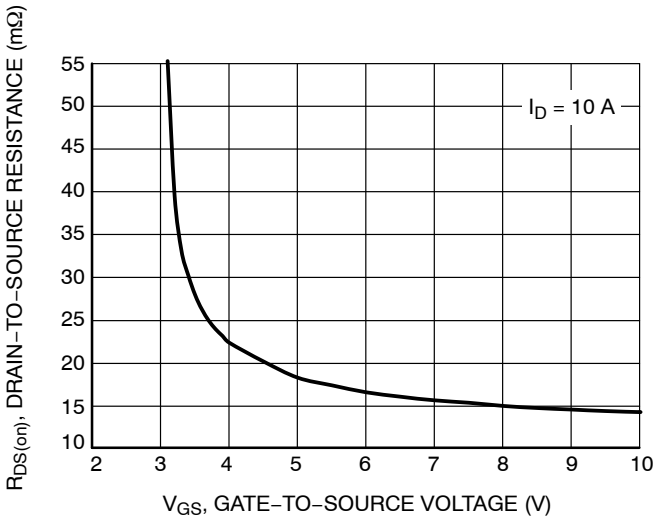


Figure 3. On−Resistance vs. Gate−to−Source Resistance

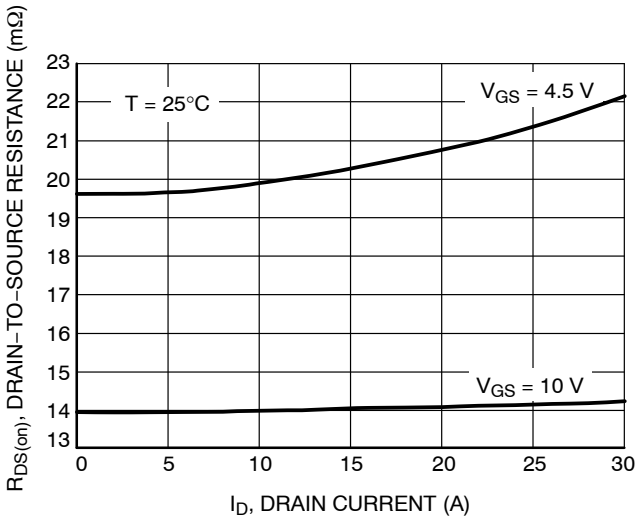


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

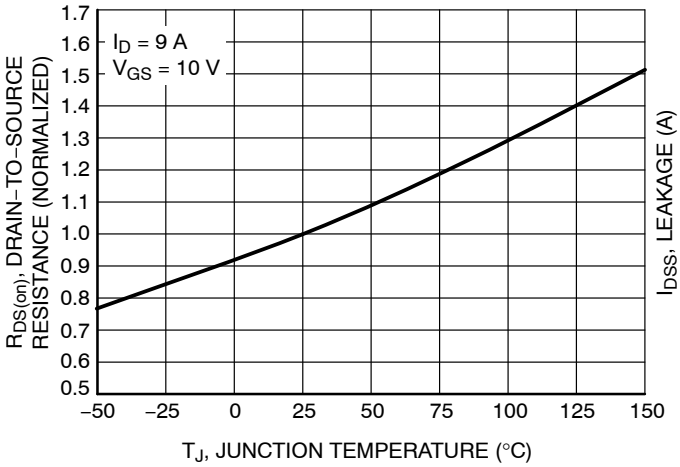


Figure 5. On−Resistance Variation with Temperature

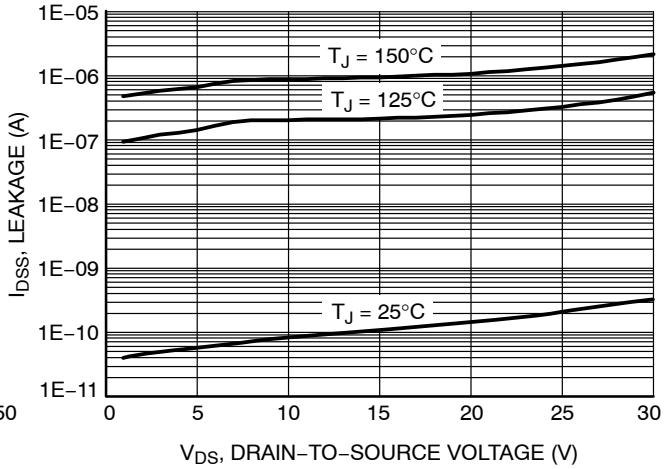


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1

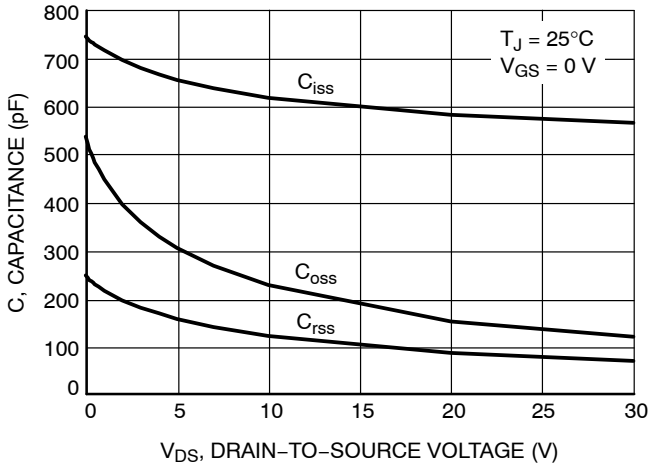


Figure 7. Capacitance Variation

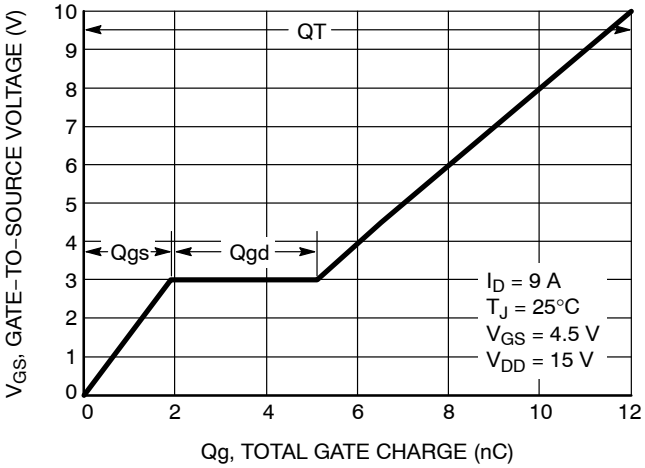


Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

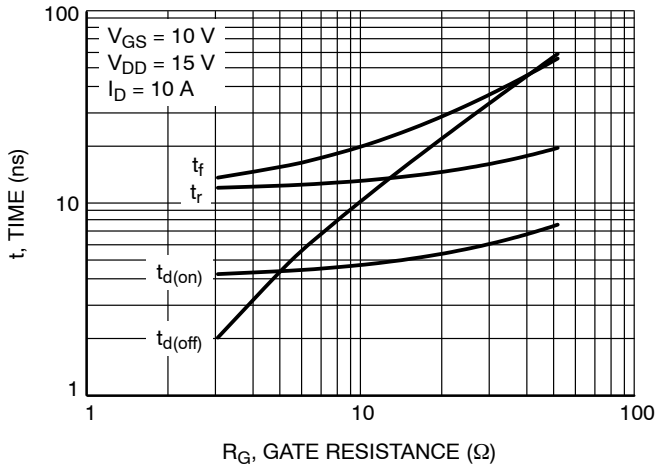


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

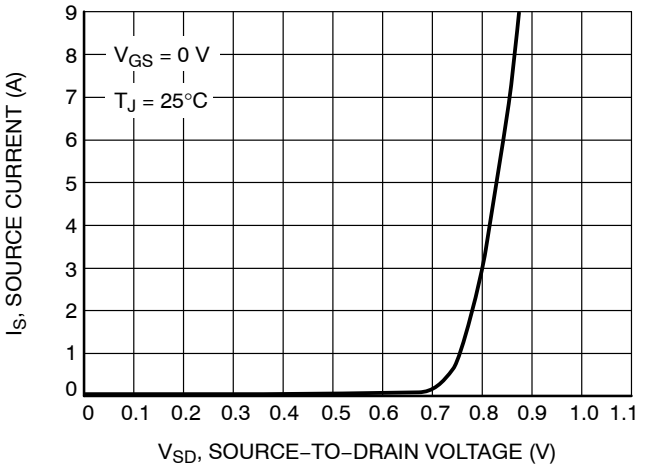


Figure 10. Diode Forward Voltage vs. Current

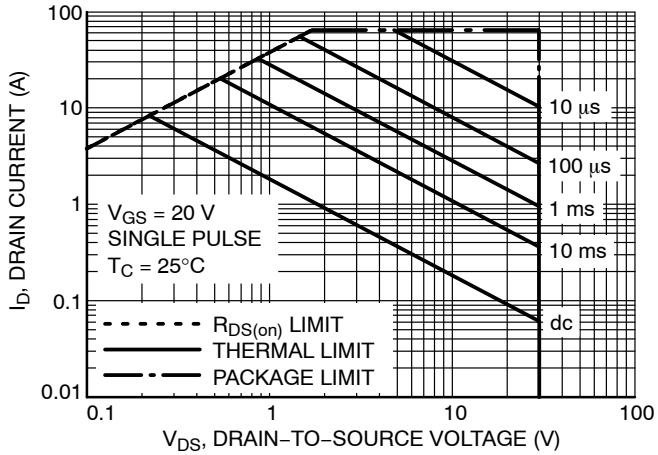


Figure 11. Maximum Rated Forward Biased Safe Operating Area

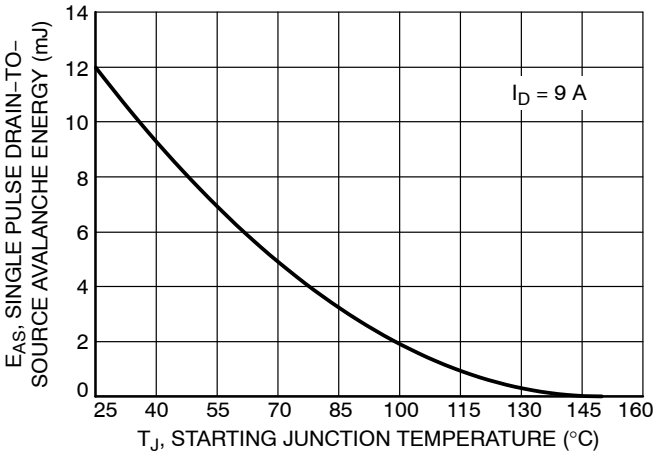


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS – Q1

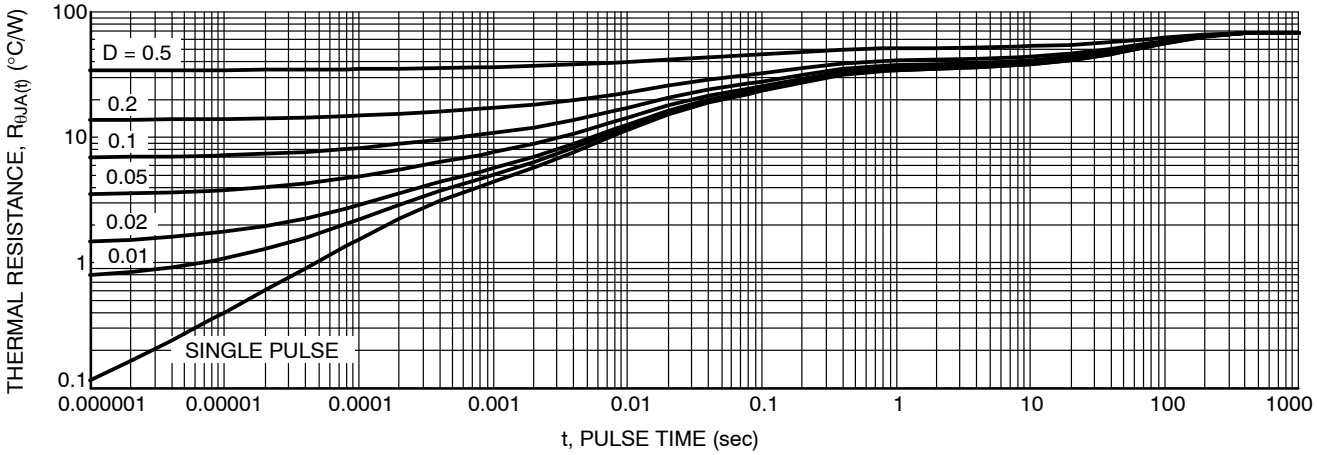


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS – Q2

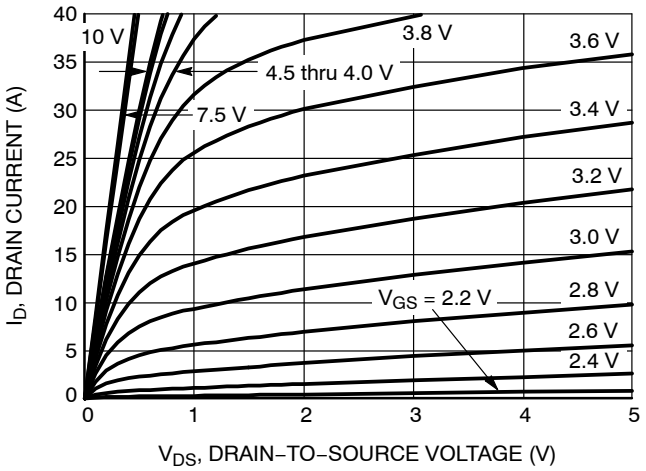


Figure 14. On−Region Characteristics

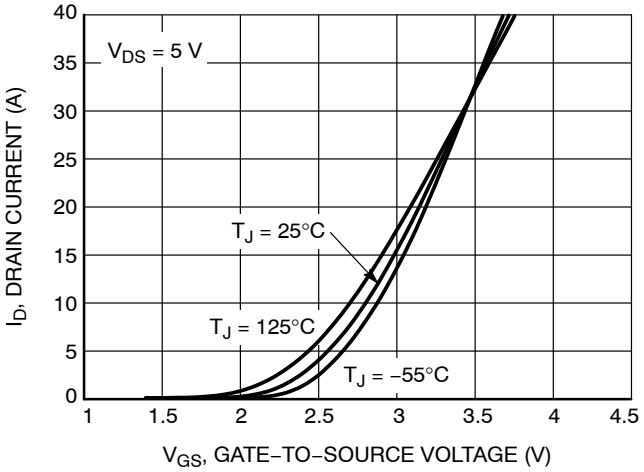


Figure 15. Transfer Characteristics

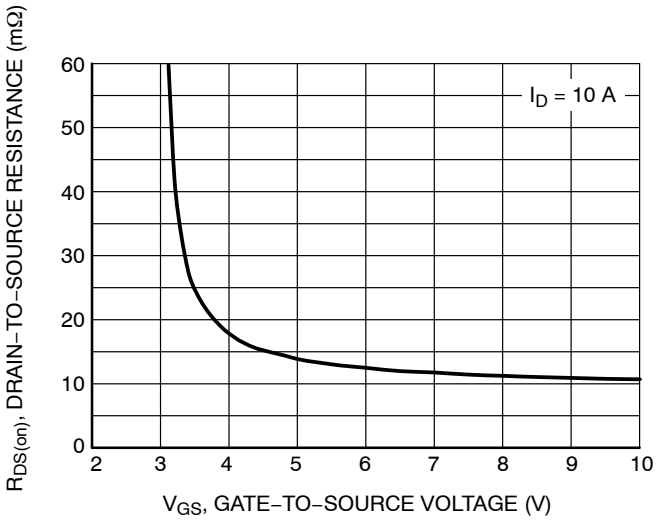


Figure 16. On−Resistance vs. Gate−to−Source Resistance

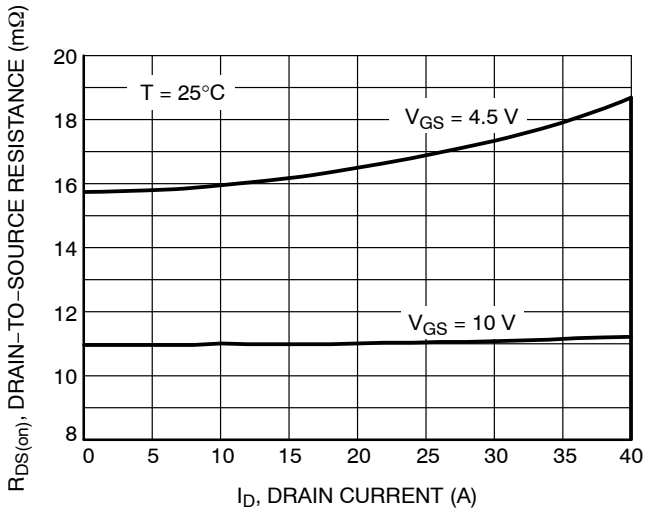


Figure 17. On−Resistance vs. Drain Current and Gate Voltage

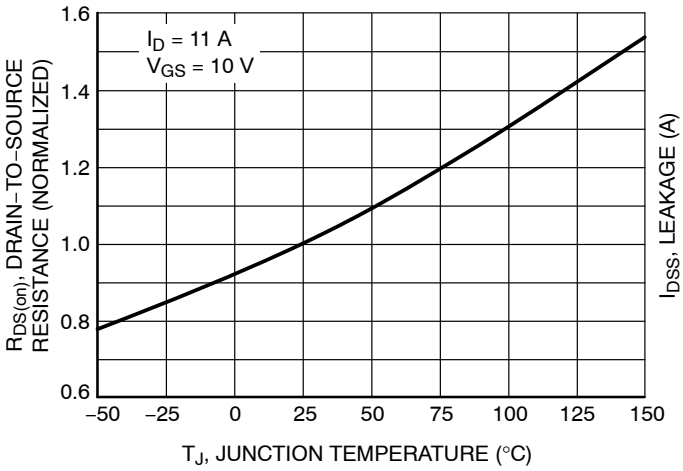


Figure 18. On−Resistance Variation with Temperature

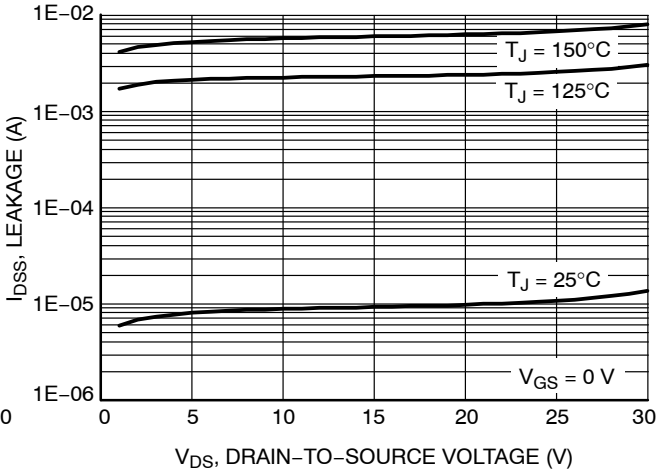


Figure 19. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

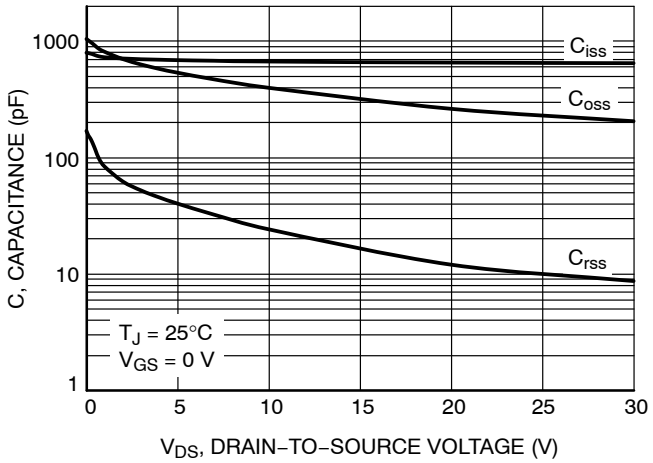


Figure 20. Capacitance Variation

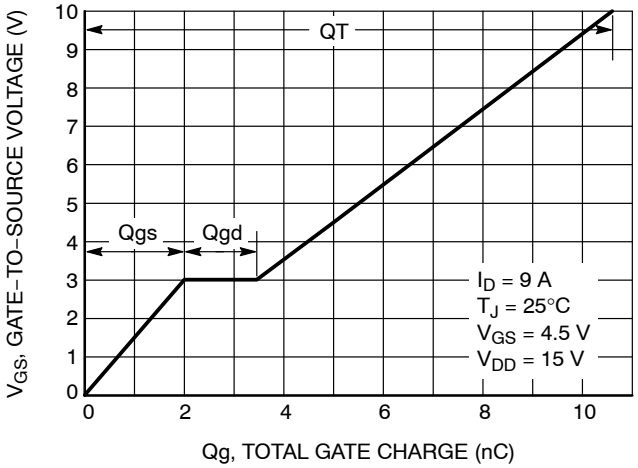


Figure 21. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

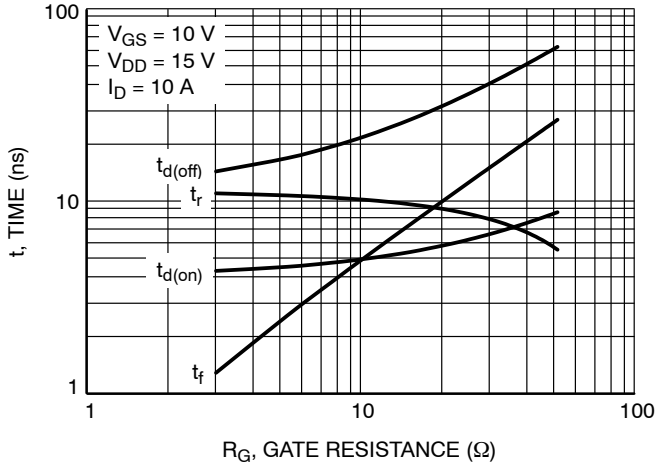


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

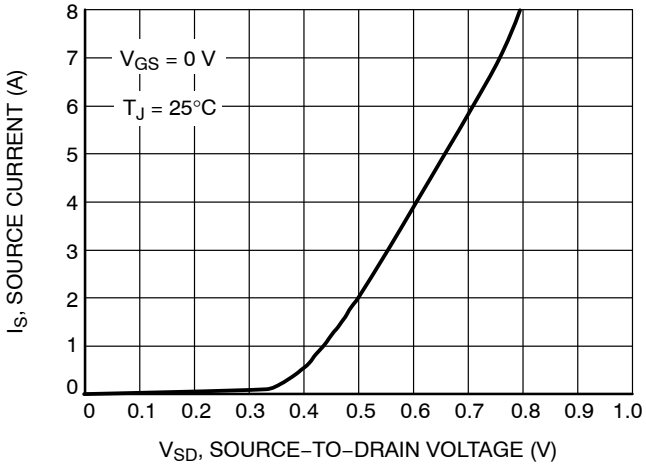


Figure 23. Diode Forward Voltage vs. Current

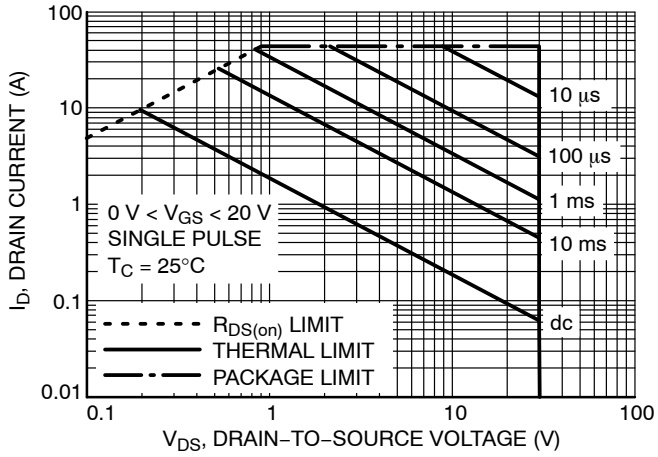


Figure 24. Maximum Rated Forward Biased Safe Operating Area

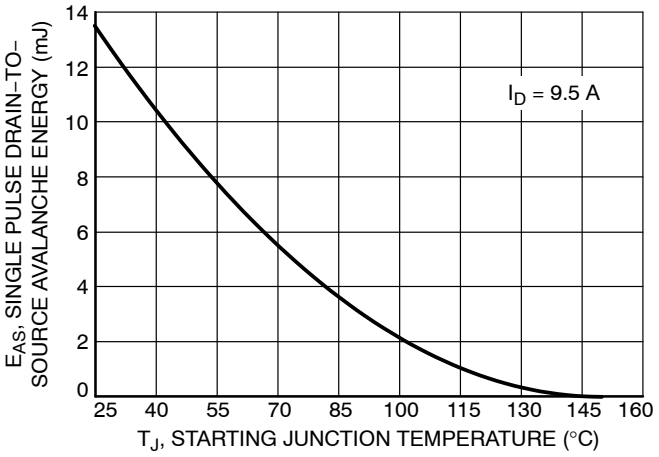


Figure 25. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS – Q2

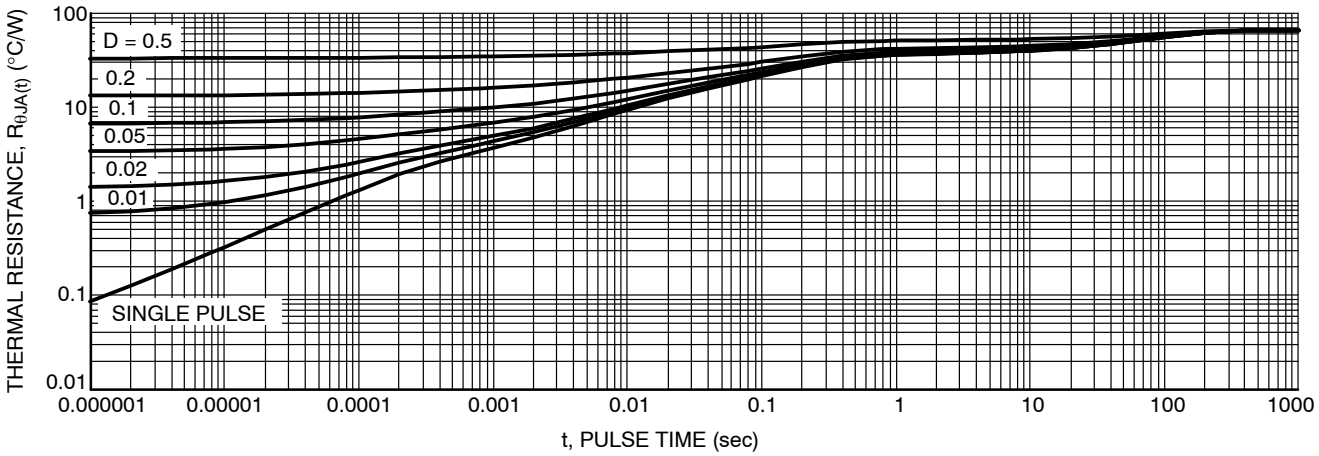


Figure 26. Thermal Response

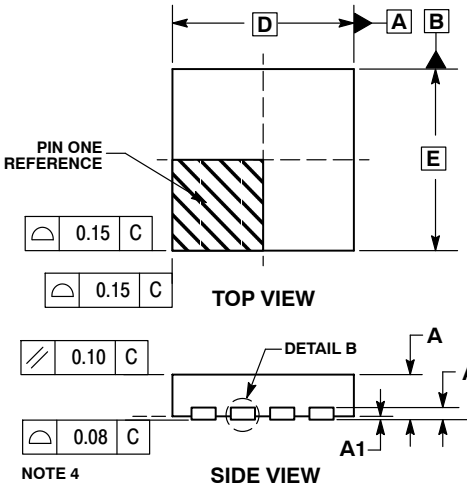
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

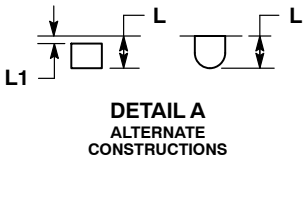
ON Semiconductor®

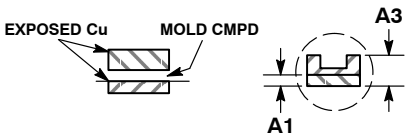
WDFN8 3x3, 0.65P
CASE 511BP
ISSUE B

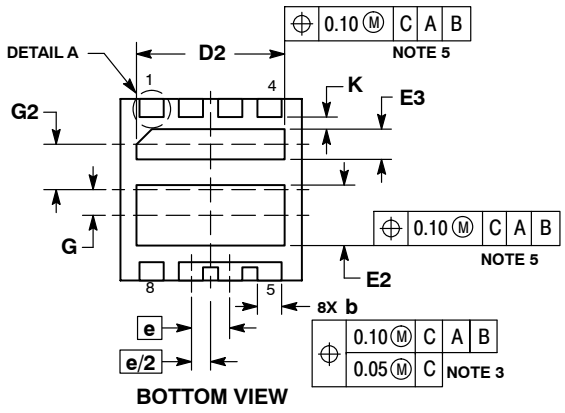
DATE 17 JUL 2012

SCALE 2:1





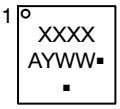




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.05 AND 0.15 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.30	0.50
D	3.00 BSC	
D2	2.35	2.55
E	3.00 BSC	
E2	0.90	1.10
E3	0.40	0.60
e	0.65 BSC	
G	0.43 BSC	
G2	0.68 BSC	
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

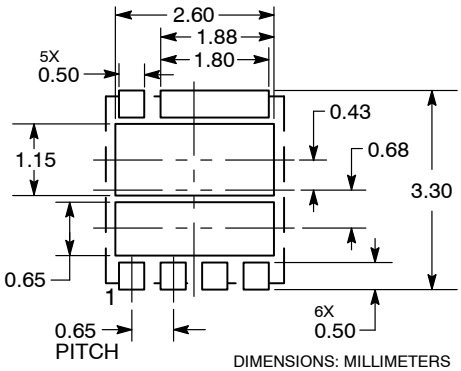


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
PIN 1. GATE 1
2. DRAIN 1
3. DRAIN 1
4. DRAIN 1
5. SOURCE 2
6. SOURCE 2
7. SOURCE 2
8. GATE 2
9. DRAIN 1
10. SOURCE 1/DRAIN 2

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