

# MOSFET – Power, Dual, N-Channel, Power Clip, Trench, Asymmetric 30 V



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## NTMFD001N03P9

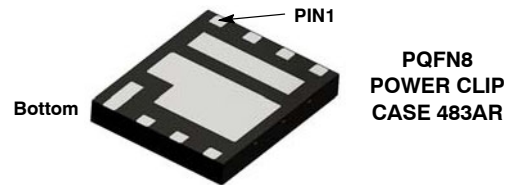
### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

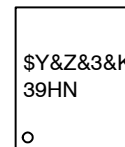
### Typical Applications

- DC-DC Converters
- System Voltage Rails

FET	$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
Q1	30 V	5.0 m $\Omega$ @ 10 V	57 A
		6.5 m $\Omega$ @ 4.5 V	
Q2	30 V	1.0 m $\Omega$ @ 10 V	165 A
		1.2 m $\Omega$ @ 4.5 V	

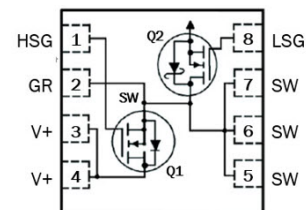
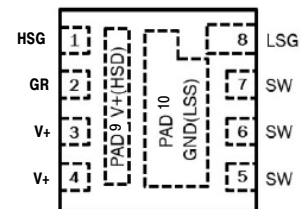


### MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Numeric Date Code
- &K = Lot Code
- 39HN = Specific Device Code

### ELECTRICAL CONNECTION



### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

# NTMFD001N03P9

**Table 1. MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Q1	Q2	Unit		
Drain-to-Source Voltage	$V_{DSS}$	30	30	V		
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	+16 V -12 V	V		
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	57	165	A
		$T_C = 85^\circ\text{C}$		41	119	
Power Dissipation $R_{\theta JC}$ (Note 3)		$T_C = 25^\circ\text{C}$	$P_D$	25	41	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	16	38	A
		$T_A = 85^\circ\text{C}$		12	27	
Power Dissipation $R_{\theta JA}$ (Note 1, 3)		$T_A = 25^\circ\text{C}$	$P_D$	2.1	2.3	W
Continuous Drain Current $R_{\theta JA}$ (Note 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	11	25	A
		$T_A = 85^\circ\text{C}$		8	18	
Power Dissipation $R_{\theta JA}$ (Note 2, 3)		$T_A = 25^\circ\text{C}$	$P_D$	0.96	1.04	W
Pulsed Drain Current		$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	300	500	A
Single Pulse Drain-to-Source Avalanche Energy Q1: $I_L = 5.3 A_{pk}, L = 3 \text{ mH}$ (Note 4) Q2: $I_L = 8.35 A_{pk}, L = 3 \text{ mH}$ (Note 4)			$E_{AS}$	42	104	mJ
Operating Junction and Storage Temperature			$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 2. THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Q1 Max	Q2 Max	Units
Junction-to-Case – Steady State (Note 1, 3)	$R_{\theta JC}$	5.0	3.0	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1, 3)	$R_{\theta JA}$	60	55	
Junction-to-Ambient – Steady State (Note 2, 3)	$R_{\theta JA}$	130	120	

- Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 2 oz Cu pad.
- Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design.  $R_{\theta CA}$  is determined by the user's board design.
- Q1 100% UIS tested at  $L = 0.1 \text{ mH}, I_{AS} = 20 \text{ A}$ .  
Q2 100% UIS tested at  $L = 0.1 \text{ mH}, I_{AS} = 47 \text{ A}$ .

# NTMFD001N03P9

**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Q1	30			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	Q2	30			
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\ \mu\text{A}, \text{ ref to } 25^\circ\text{C}$	Q1		15		mV/ $^\circ\text{C}$
		$I_D = 50\text{ mA}, \text{ ref to } 25^\circ\text{C}$	Q2		16		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	Q1		1	$\mu\text{A}$
				Q2		500	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$	Q1			100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = 16\text{ V}$	Q2			100	

**ON CHARACTERISTICS** (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	Q1	1.0		3.0	V
		$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	Q2	1.0		3.0	
Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 250\ \mu\text{A}, \text{ ref to } 25^\circ\text{C}$	Q1		-5		mV/ $^\circ\text{C}$
		$I_D = 50\text{ mA}, \text{ ref to } 25^\circ\text{C}$	Q2		-3		
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$	Q1		4.5	5.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$			5.4	6.5	
		$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$	Q2		0.75	1.0	
		$V_{GS} = 4.5\text{ V}, I_D = 37\text{ A}$			0.9	1.2	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 14\text{ A}$	Q1		93		S
		$V_{DS} = 5\text{ V}, I_D = 37\text{ A}$	Q2		248		
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	Q1		1		$\Omega$
			Q2		1		

**CHARGES & CAPACITANCES**

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$	Q1		1224		pF	
			Q2		6575			
Output Capacitance	$C_{OSS}$		Q1		397		pF	
			Q2		2086			
Reverse Capacitance	$C_{RSS}$		Q1		42		pF	
			Q2		138			
Total Gate Charge	$Q_{G(TOT)}$		Q1: $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 14\text{ A}$ Q2: $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 37\text{ A}$	Q1		7.9		nC
				Q2		43		
Gate-to-Drain Charge	$Q_{GD}$	Q1			2.0		nC	
		Q2			9.5			
Gate-to-Source Charge	$Q_{GS}$	Q1			3.1		nC	
		Q2			15.8			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 14\text{ A}$		Q1		17		nC
		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 37\text{ A}$		Q2		93		

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

# NTMFD001N03P9

**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit	
<b>SWITCHING CHARACTERISTICS, <math>V_{GS} = 4.5\text{ V}</math> (Note 6)</b>								
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}$ Q1: $I_D = 14\text{ A}$ , $V_{DD} = 15\text{ V}$ , $R_G = 6\ \Omega$ Q2: $I_D = 37\text{ A}$ , $V_{DD} = 15\text{ V}$ , $R_G = 6\ \Omega$	Q1		36		ns	
			Q2		12.6			
Rise Time	$t_{r(ON)}$		Q1		30.7		ns	
			Q2		21.5			
Turn-Off Delay Time	$t_{d(OFF)}$		Q1		64.7		ns	
			Q2		17.5			
Fall Time	$t_f$		Q1		23.5		ns	
			Q2		7.3			
<b>SWITCHING CHARACTERISTICS, <math>V_{GS} = 10\text{ V}</math> (Note 6)</b>								
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}$ Q1: $I_D = 17\text{ A}$ , $V_{DD} = 15\text{ V}$ , $R_G = 6\ \Omega$ Q2: $I_D = 40\text{ A}$ , $V_{DD} = 15\text{ V}$ , $R_G = 6\ \Omega$	Q1		8.0		ns	
			Q2		8.6			
Rise Time	$t_{r(ON)}$		Q1		2.0		ns	
			Q2		18.2			
Turn-Off Delay Time	$t_{d(OFF)}$		Q1		23.5		ns	
			Q2		4.5			
Fall Time	$t_f$		Q1		2.0		ns	
			Q2		4.5			
<b>SOURCE-TO-DRAIN DIODE CHARACTERISTICS</b>								
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}$ , $I_S = 14\text{ A}$	$T_J = 25^\circ\text{C}$	Q1		0.79	1.2	V
			$T_J = 125^\circ\text{C}$			0.66		
		$V_{GS} = 0\text{ V}$ , $I_S = 37\text{ A}$	$T_J = 25^\circ\text{C}$	Q2		0.77	1.2	
			$T_J = 125^\circ\text{C}$			0.63		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}$ Q1: $I_S = 14\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ Q2: $I_S = 37\text{ A}$ , $di/dt = 240\text{ A}/\mu\text{s}$	Q1		23		ns	
			Q2		4.6			
Reverse Recovery Charge	$Q_{RR}$		Q1		8.0		nC	
			Q2		68.3			

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$   
 6. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS – Q1

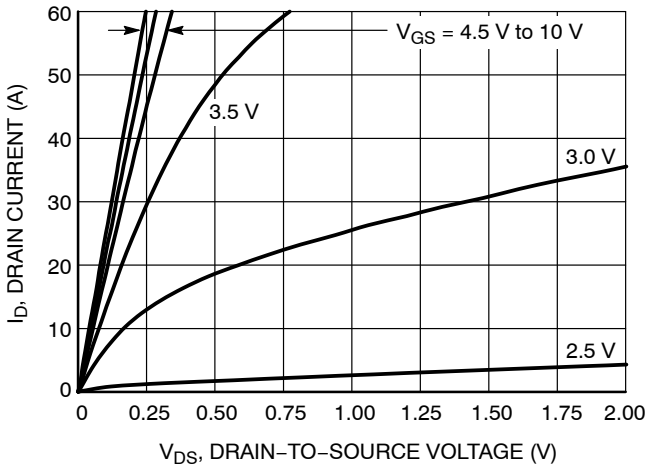


Figure 1. On-Region Characteristics

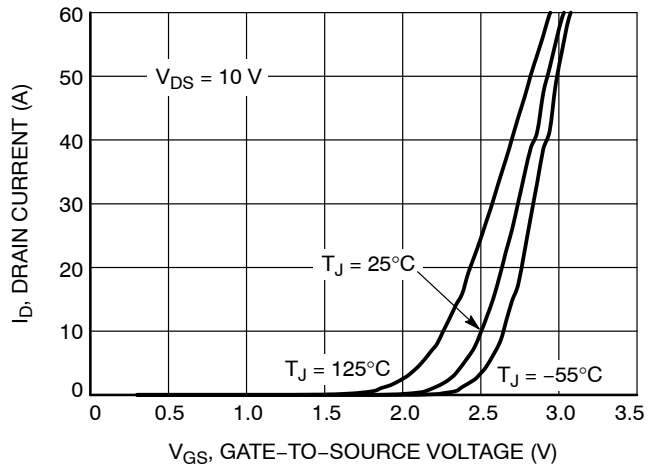


Figure 2. Transfer Characteristics

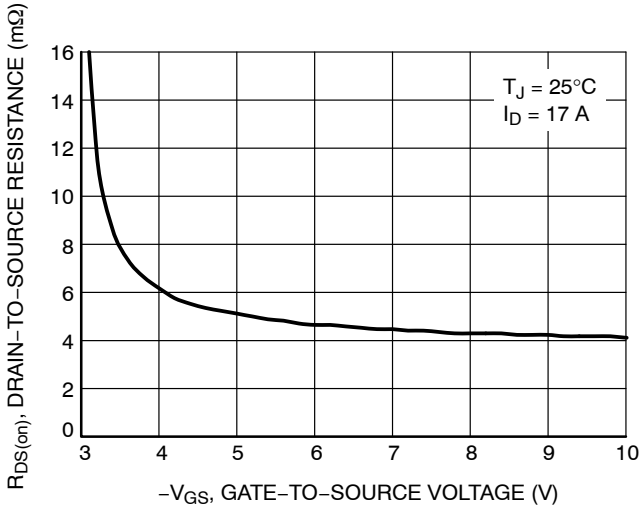


Figure 3. On-Resistance vs. Gate-to-Source Voltage

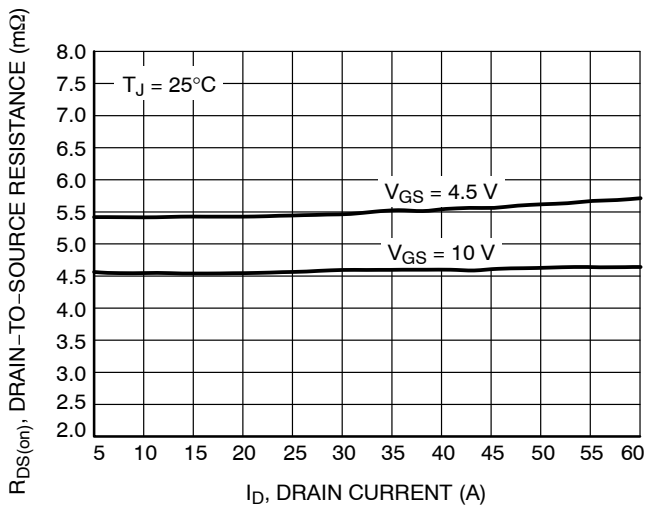


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

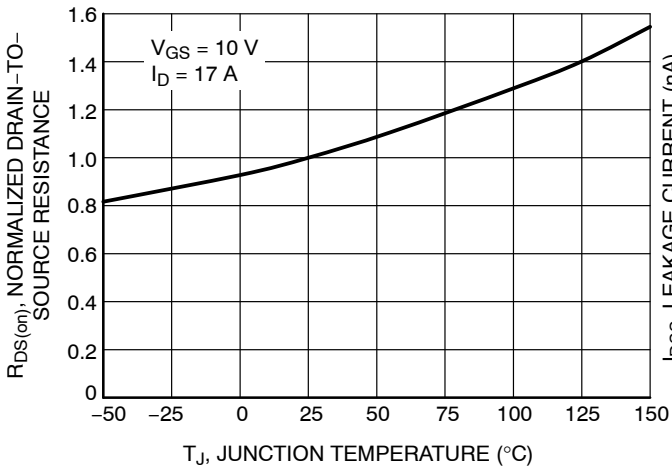


Figure 5. On-Resistance Variation with Temperature

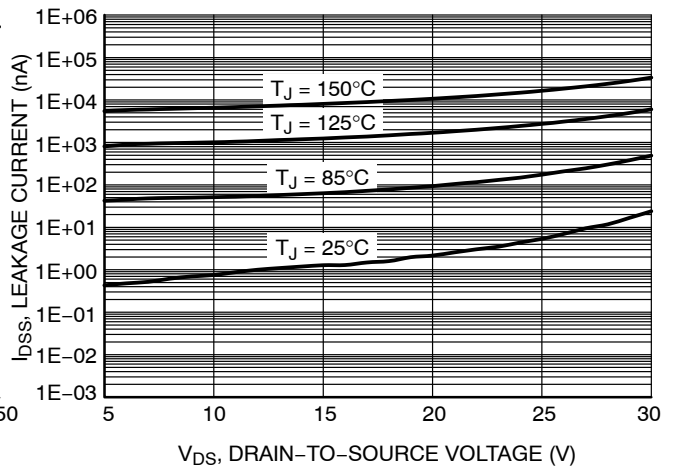
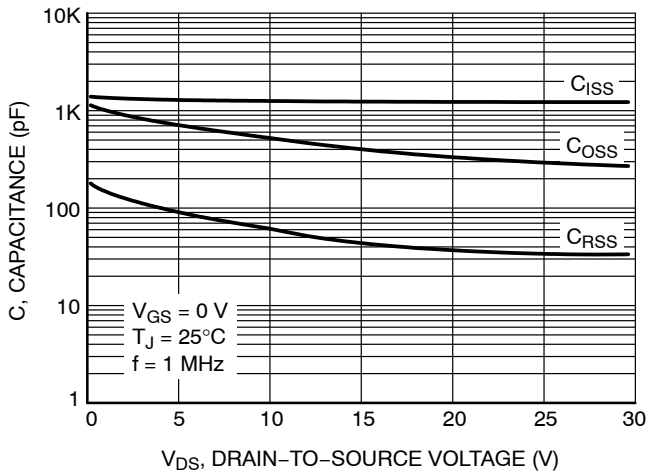


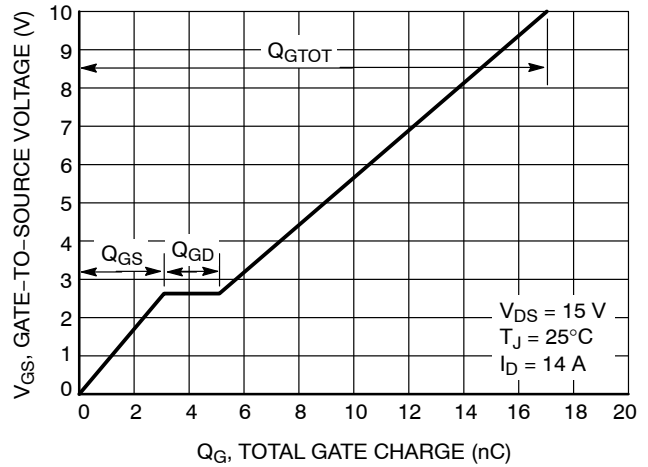
Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTMFD001N03P9

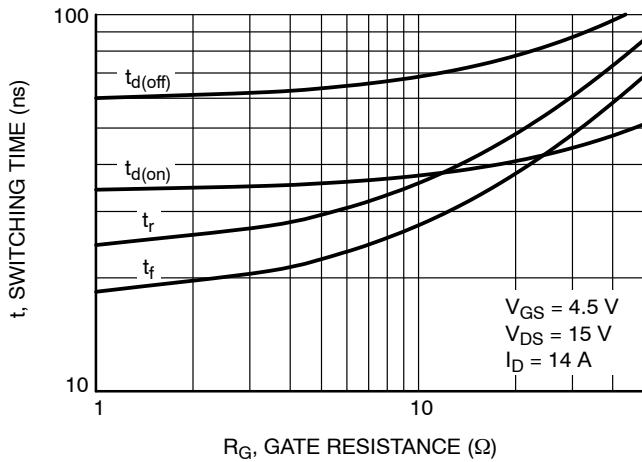
## TYPICAL CHARACTERISTICS – Q1



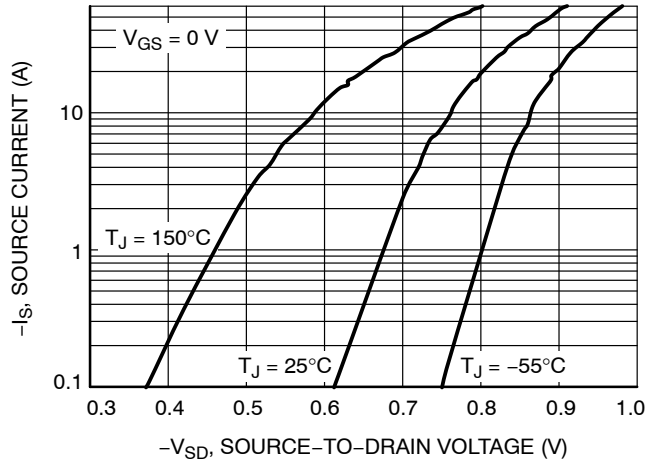
**Figure 7. Capacitance Variation**



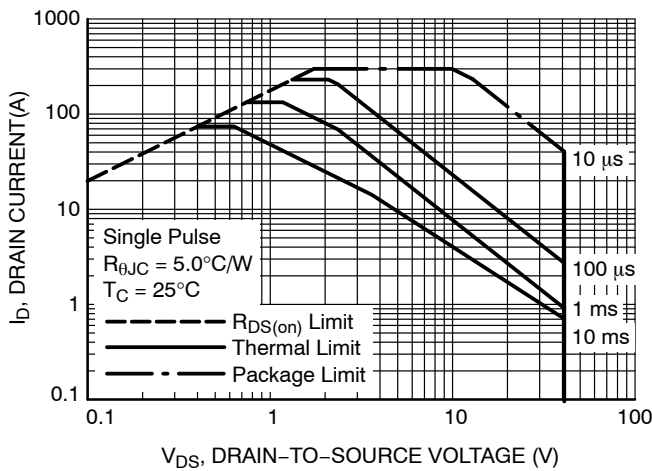
**Figure 8. Gate-to-Source Voltage vs. Total Charge**



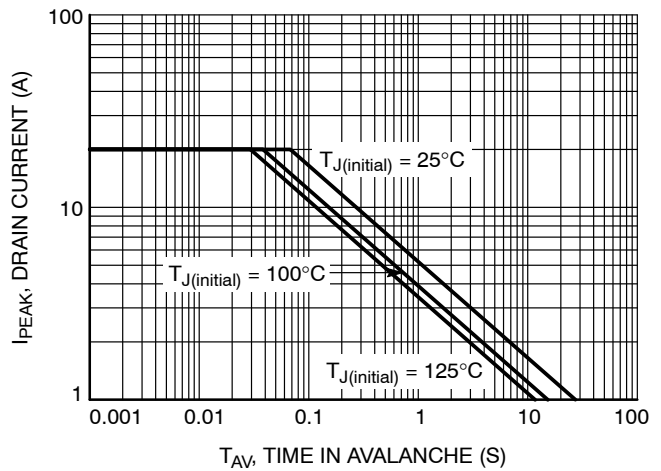
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Drain Current vs. Time in Avalanche**

# NTMFD001N03P9

## TYPICAL CHARACTERISTICS – Q1

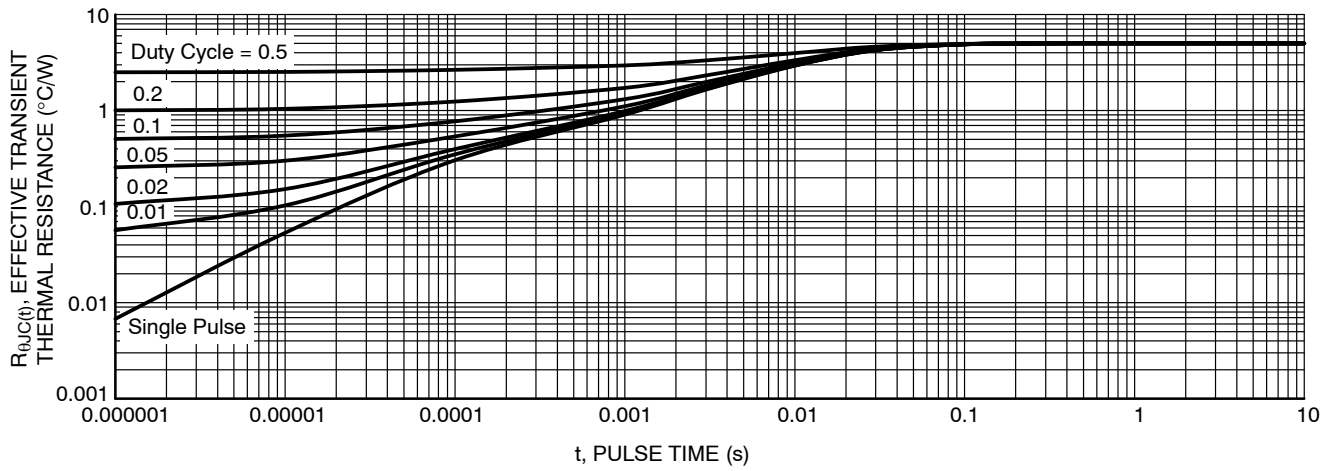


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS – Q2

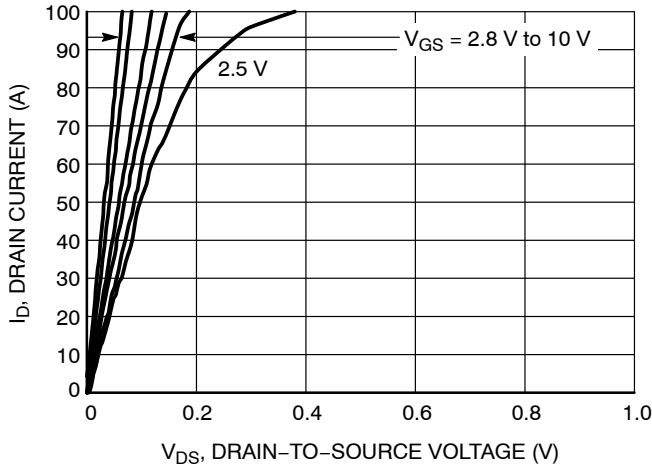


Figure 14. On-Region Characteristics

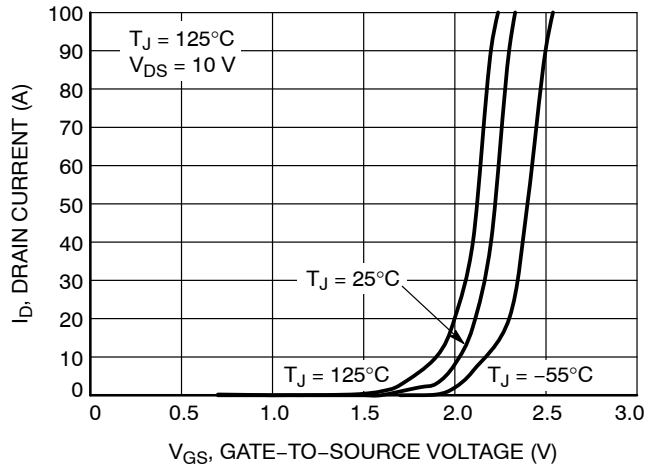


Figure 15. Transfer Characteristics

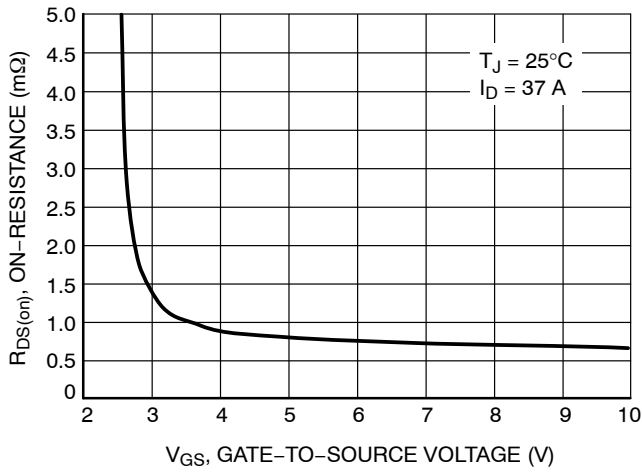


Figure 16. On-Resistance vs. Gate-to-Source Voltage

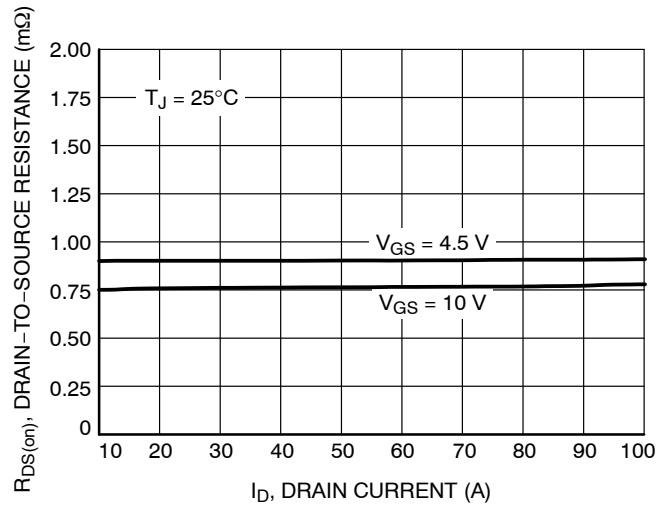


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

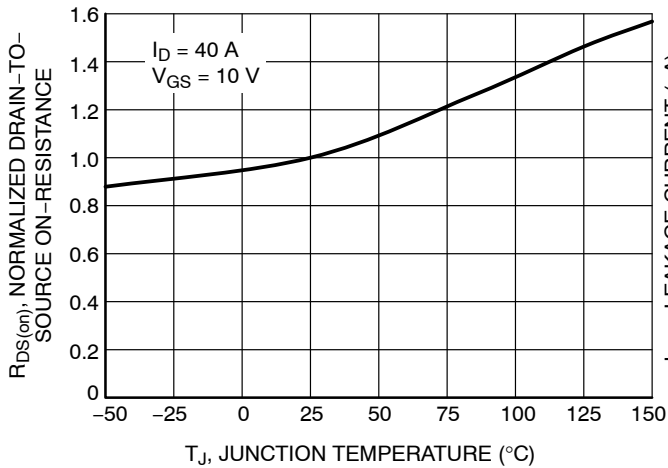


Figure 18. On-Resistance Variation with Temperature

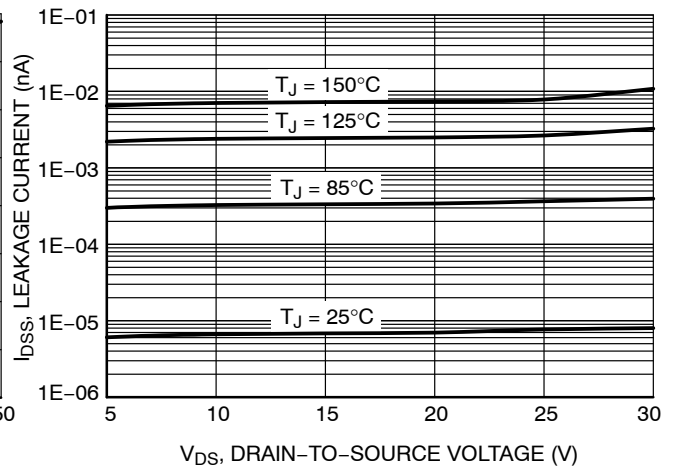


Figure 19. Drain-to-Source Leakage Current vs. Voltage



TYPICAL CHARACTERISTICS – Q2

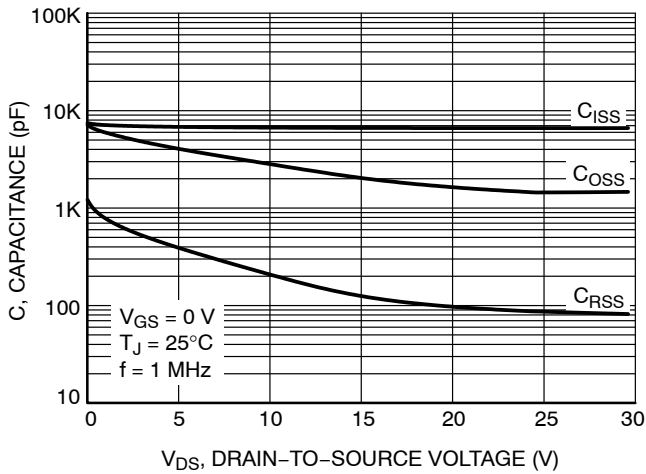


Figure 20. Capacitance Variation

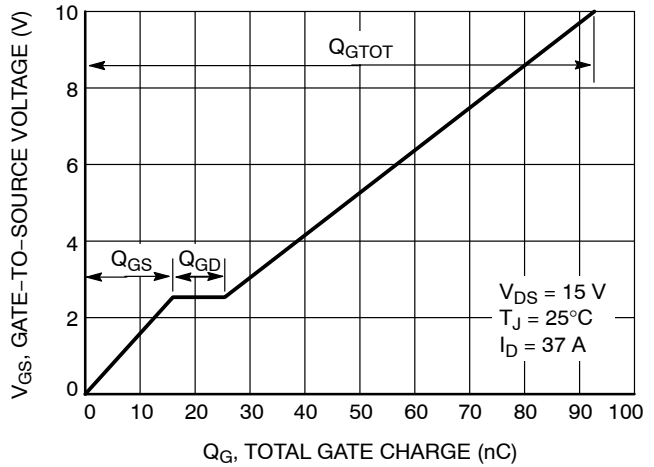


Figure 21. Gate-to-Source Voltage vs. Total Charge

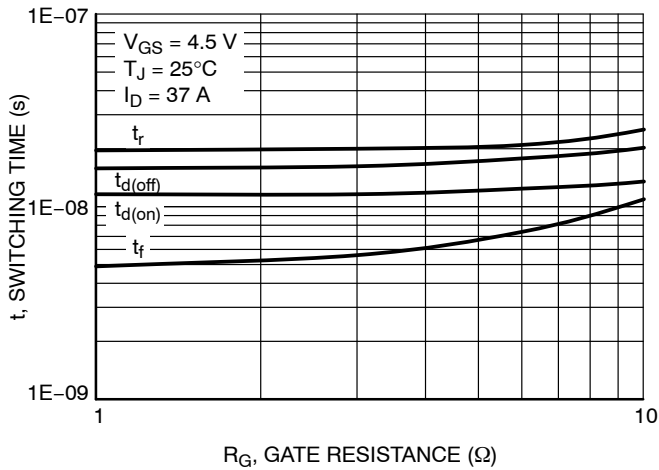


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

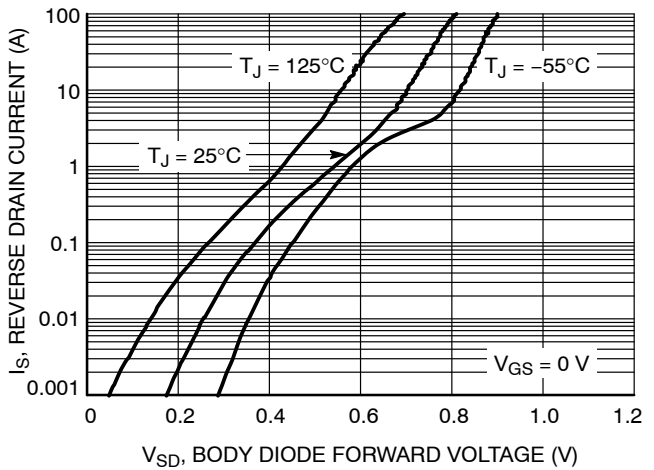


Figure 23. Diode Forward Voltage vs. Current

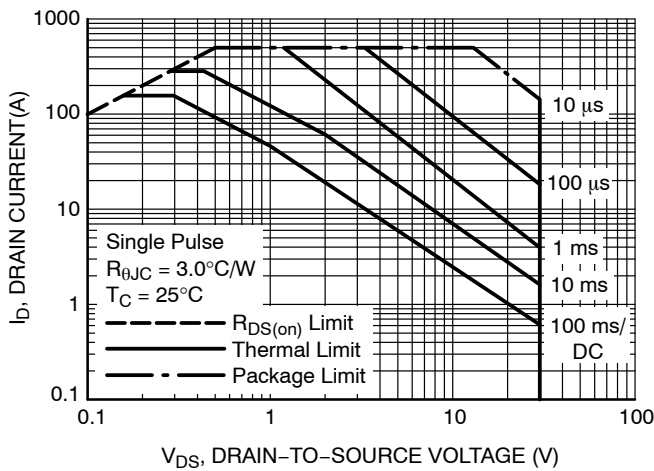


Figure 24. Maximum Rated Forward Biased Safe Operating Area

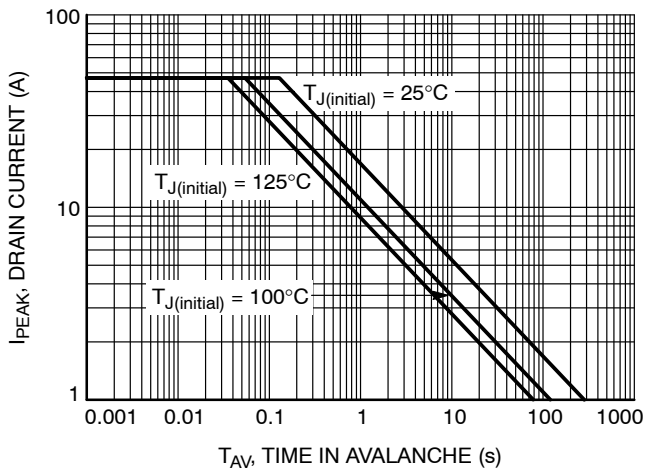


Figure 25. Maximum Drain Current vs. Time in Avalanche

# NTMFD001N03P9

## TYPICAL CHARACTERISTICS – Q2

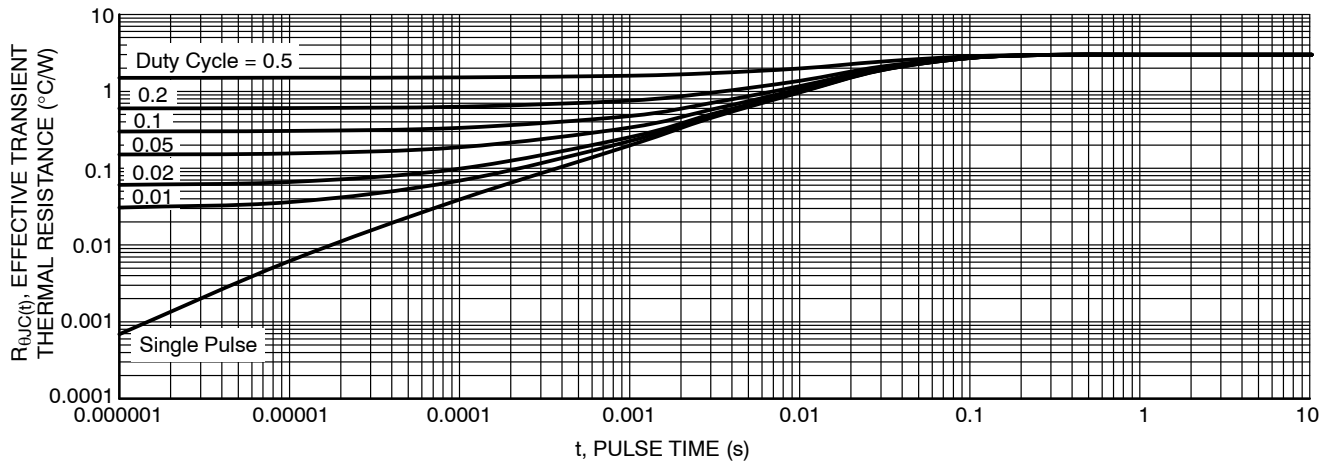
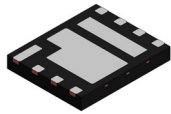


Figure 26. Transient Thermal Impedance

### ORDERING INFORMATION

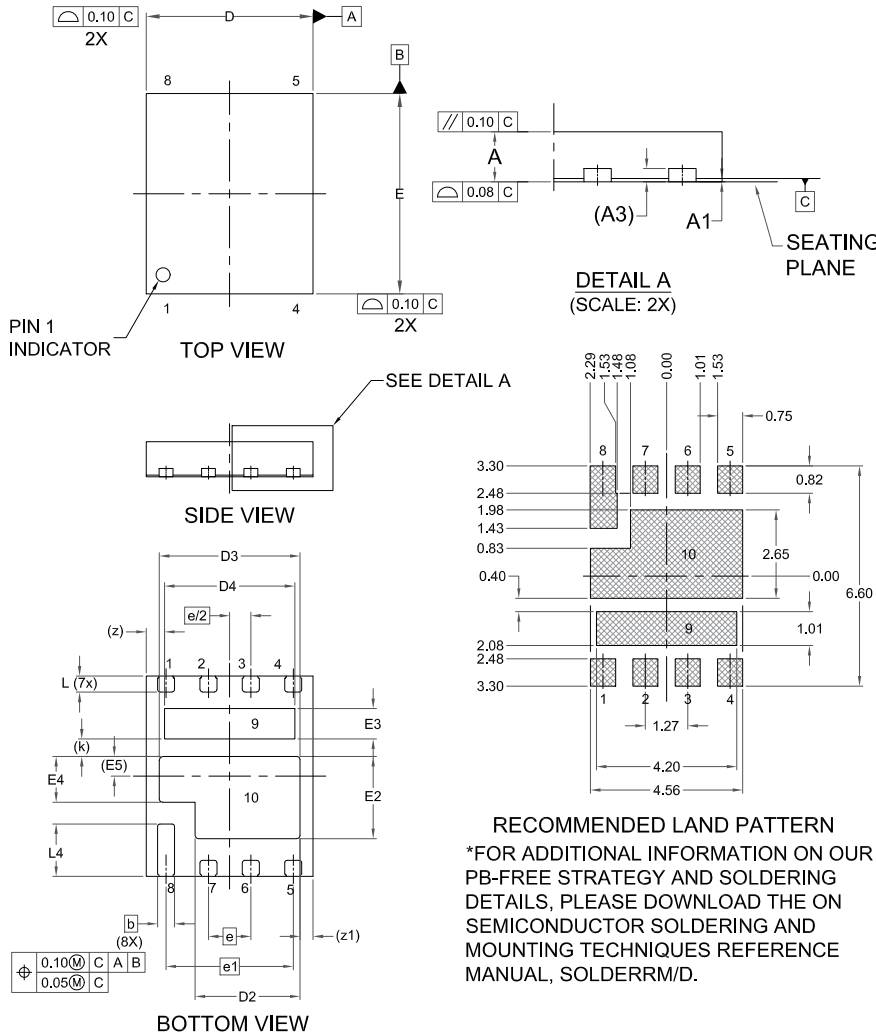
Device	Package	Shipping
NTMFD001N03P9	DFN8 (Pb-Free)	3000 / Tape & Reel

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**PQFN8 5.00x6.00x0.75, 1.27P**  
CASE 483AR  
ISSUE D

DATE 06 NOV 2023



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5	0.59 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.52 REF		
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

**RECOMMENDED LAND PATTERN**  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON13666G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PQFN8 5.00x6.00x0.75, 1.27P</b>	<b>PAGE 1 OF 1</b>

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