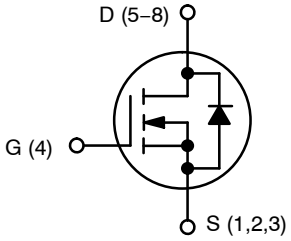
MOSFET - Power, Single N-Channel, Logic Level, SO-8FL

40 V, 0.49 mΩ, 455 A

NTMFS0D5N04XL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.49 mΩ @ 10 V	455 A
	0.78 mΩ @ 4.5 V	



N–CHANNEL MOSFET

Features

- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low Q_{RR} with Soft Recovery to Minimize E_{RR} Loss and Voltage Spike
- Low Q_G and Capacitance to Minimize Driving and Switching Loss
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

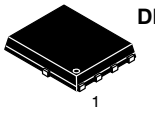
- High Switching Frequency DC–DC Conversion
- Synchronous Rectification

MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	40	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	455	A
		T_C = 100°C		322	
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	194	W
		T_C = 100°C		97.3	
Pulsed Drain Current	T_A = 25°C, t_p = 100 μs		I_{DM}	2474	A
Pulsed Sourced Current (Body Diode)			I_{SM}	2474	
Operating Junction and Storage Temperature Range			T_J, T_{STG}	–55 to +175	°C
Source Current (Body Diode)			I_S	306	A
Single Pulse Drain–to–Source Avalanche Energy (I_{Lpk} = 94 A)			E_{AS}	1325	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

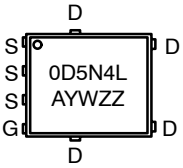
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface–mounted on FR4 board using 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. $R_{\theta JCT}$ Thermal Resistance – Junction to Case Top = 20 °C/W.



DFNW5 (SO–8FL)
CASE 506FA

MARKING DIAGRAM



0D5N4L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.77	°C/W
Thermal Resistance, Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	38	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA. referenced to 25°C			16.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS							
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A, T_J = 25°C			0.39	0.49	mΩ
		V_{GS} = 4.5 V, I_D = 50 A, T_J = 25°C			0.54	0.78	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 330 μA, T_J = 25°C		1.3		2.2	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 330 μA			−5.35		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A			277		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz			9444		pF
Output Capacitance	C_{OSS}				2468		
Reverse Transfer Capacitance	C_{RSS}				38		
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DS} = 20 V			95		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 50 A			57		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 50 A			127		
Threshold Gate Charge	$Q_{G(TH)}$				15		
Gate−to−Source Charge	Q_{GS}				27		
Gate−to−Drain Charge	Q_{GD}				9		
Gate Plateau Voltage	V_{GP}				2.8		V
Gate Resistance	R_G	f = 1 MHz			0.48		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DS} = 20 V, I_D = 50 A, R_G = 2.5 Ω			11		ns
Rise Time	t_r				10		
Turn−Off Delay Time	$t_{d(OFF)}$				55		
Fall Time	t_f				24		
DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.78	1.2	V
			T_J = 125°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DS} = 20 V, dI_S/dt = 300 A/μs, I_S = 50 A			40.5		ns
Charge Time	t_a				22.2		
Discharge Time	t_b				18.3		
Reverse Recovery Charge	Q_{RR}				108		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

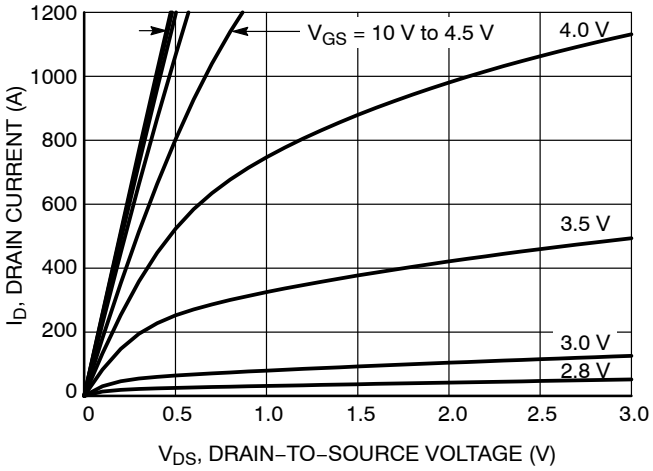


Figure 1. On−Region Characteristics

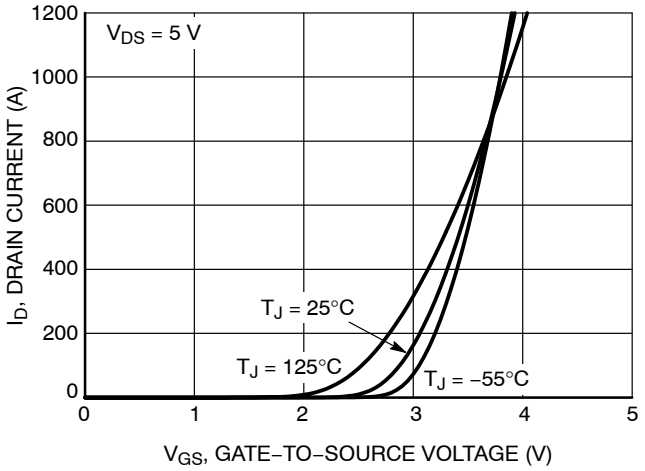


Figure 2. Transfer Characteristics

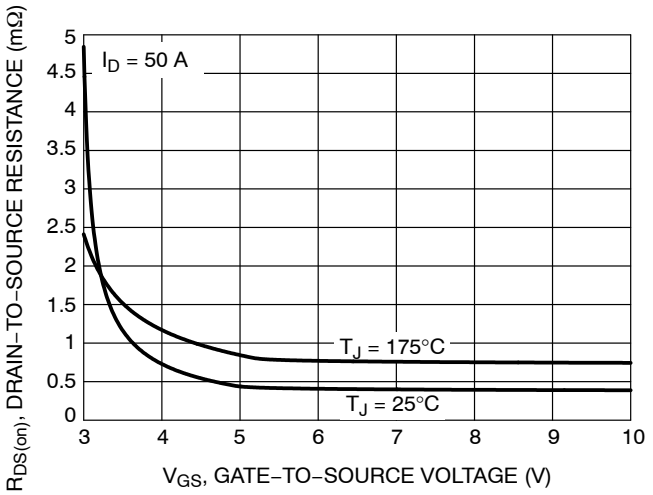


Figure 3. On−Resistance vs. Gate−to−Source Voltage

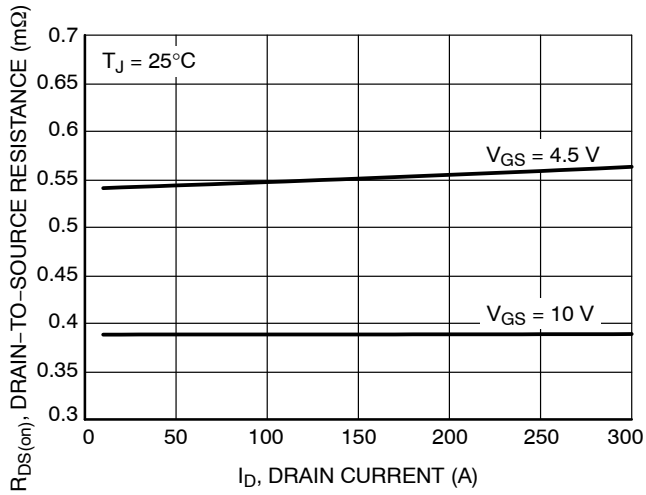


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

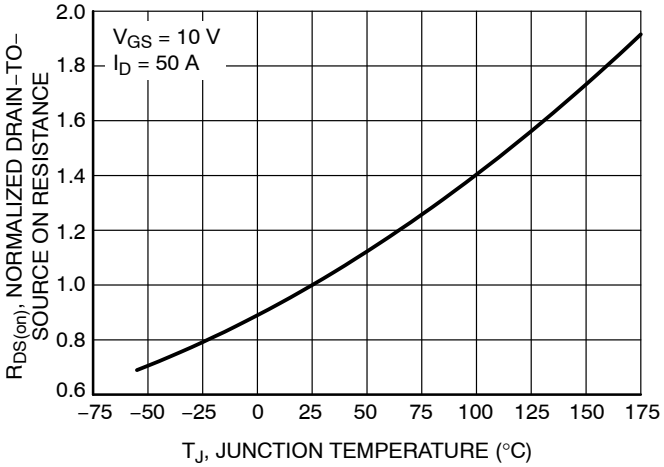


Figure 5. On−Resistance Variation with Temperature

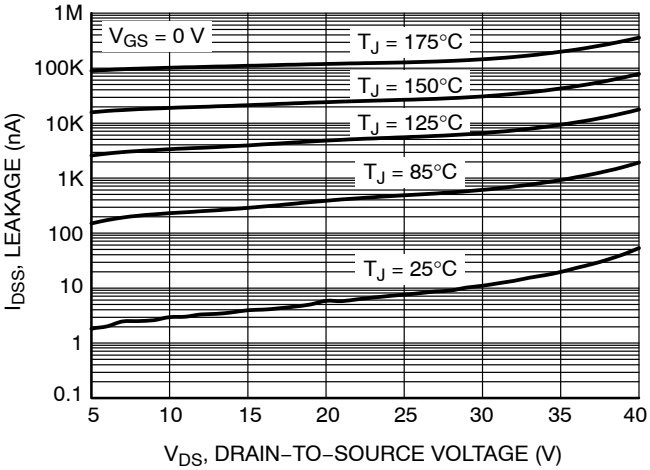


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

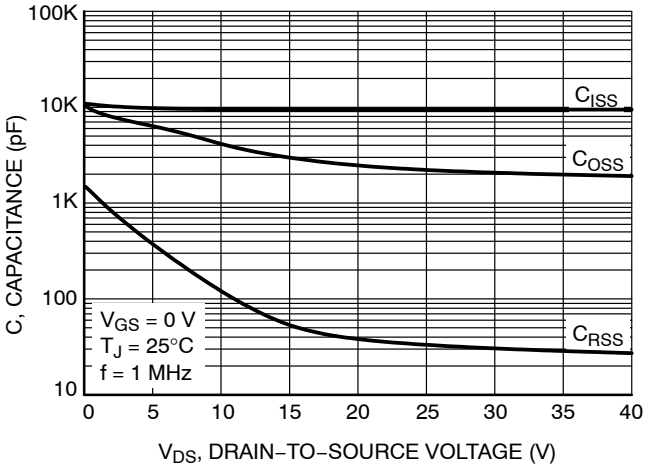


Figure 7. Capacitance Variation

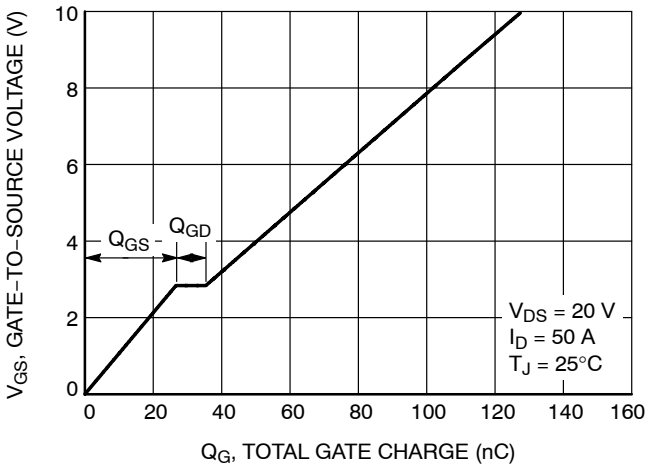


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

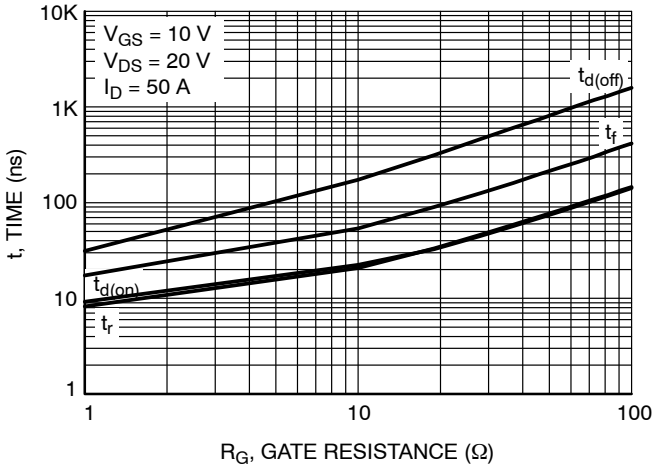


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

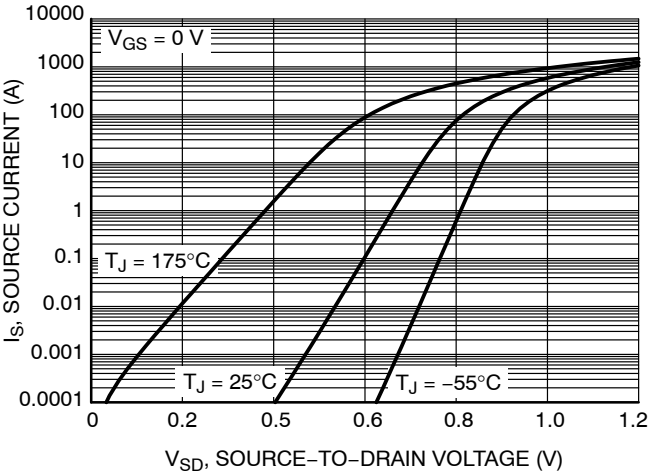


Figure 10. Diode Forward Voltage vs. Current

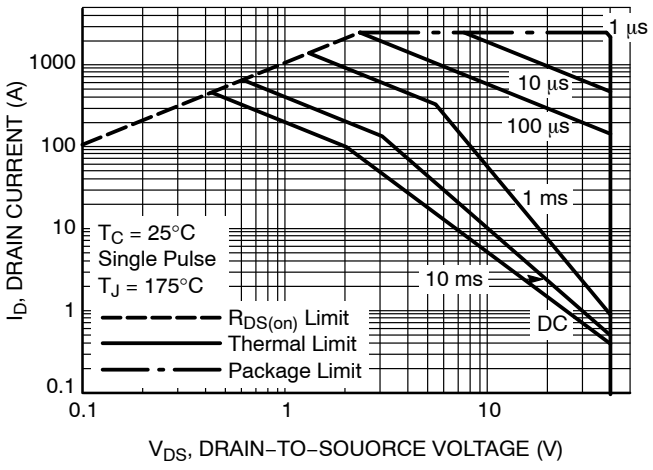


Figure 11. Safe Operating Area (SOA)

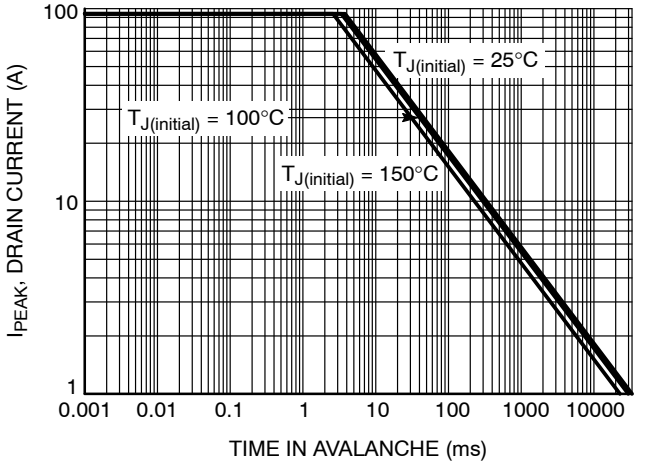


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

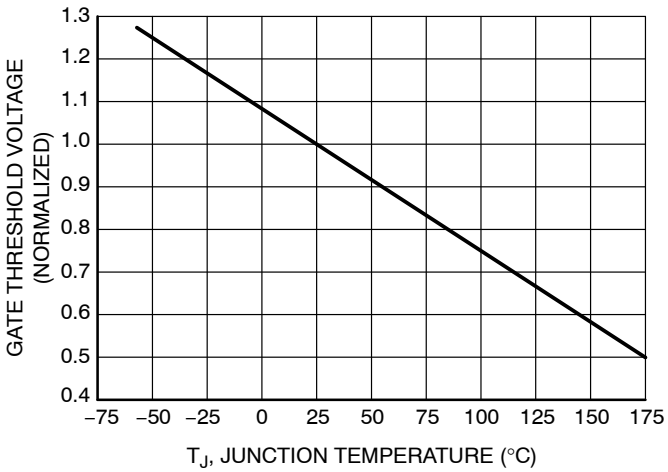


Figure 13. Gate Threshold Voltage vs. Junction Temperature

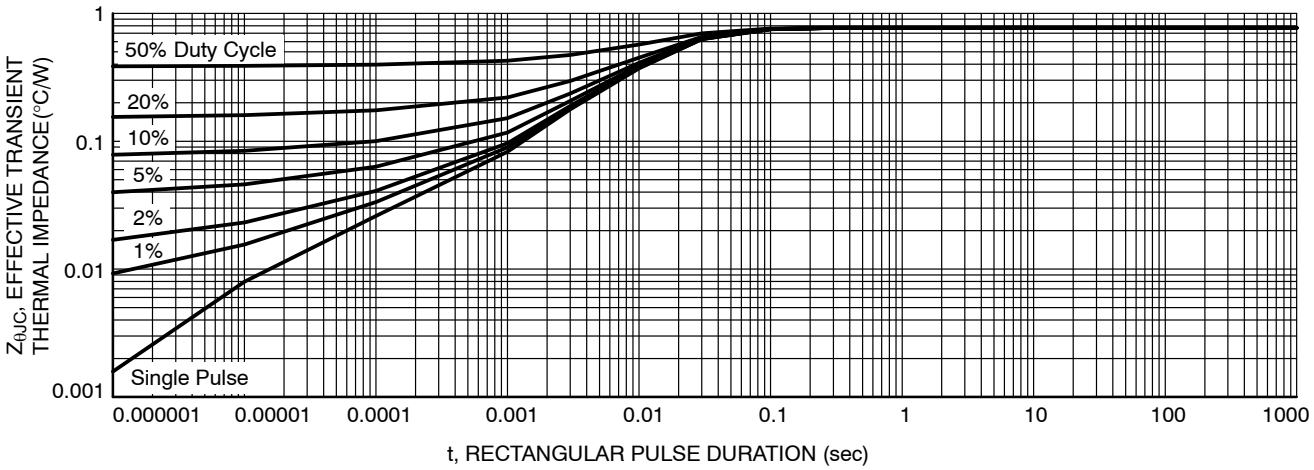


Figure 14. Thermal Characteristics

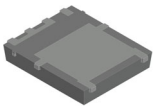
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS0D5N04XLT1G	0D5N4L	DFNW5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

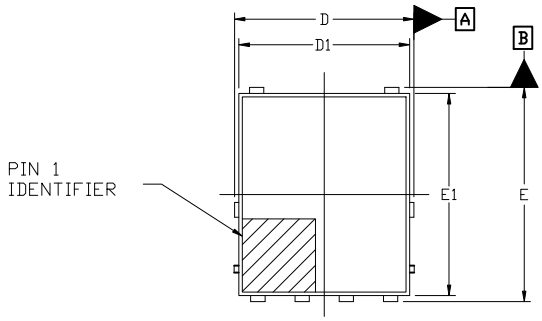
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

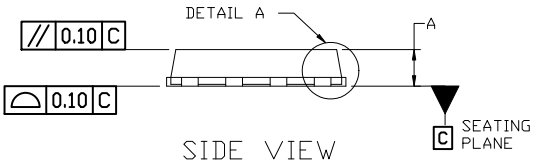


DFN5 5x6, 1.27P
CASE 506FA
ISSUE O

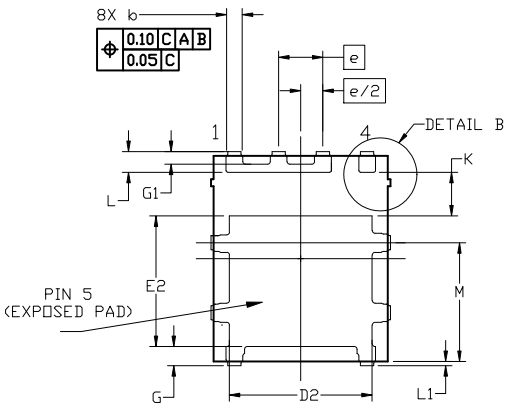
DATE 16 FEB 2021



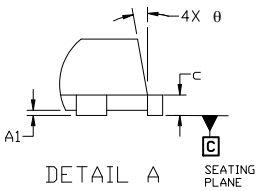
TOP VIEW

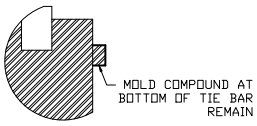


SIDE VIEW



BOTTOM VIEW

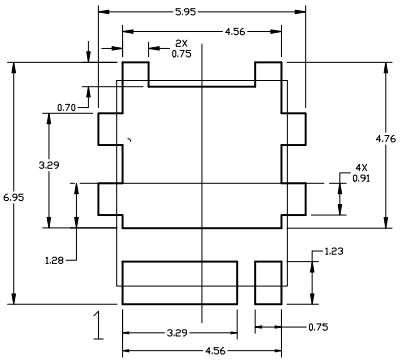




DETAIL B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

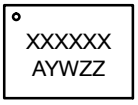
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.80	5.00	5.20
D2	3.90	4.10	4.30
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.55	3.75	3.95
e	1.27 BSC		
G	0.50	0.55	0.70
G1	0.26	0.36	0.46
k	1.10	1.25	1.40
L	0.50	0.60	0.70
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON21323H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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