



# NTMFS4C08N

- Surface-mounted on FR4 board using the minimum recommended pad size.
- This is the absolute maximum rating. Parts are 100% tested at  $T_J = 25^\circ\text{C}$ ,  $V_{GS} = 10\text{ V}$ ,  $I_L = 21\text{ Apk}$ ,  $E_{AS} = 22\text{ mJ}$ .

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	49.8	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	164.6	
Junction-to-Ambient – ( $t \leq 10\text{ s}$ ) (Note 4)	$R_{\theta JA}$	21.0	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSS(t)}$	$V_{GS} = 0\text{ V}$ , $I_{D(aval)} = 8.4\text{ A}$ , $T_{case} = 25^\circ\text{C}$ , $t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			13.8		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1.3		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.9		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 18\text{ A}$	4.6	5.8	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	6.8	8.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}$ , $I_D = 15\text{ A}$		42		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $V_{DS} = 15\text{ V}$		1113	1670	$\text{pF}$
Output Capacitance	$C_{OSS}$			702		
Reverse Transfer Capacitance	$C_{RSS}$			39		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 15\text{ V}$ , $f = 1\text{ MHz}$		0.035		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}$ , $V_{DS} = 15\text{ V}$ ; $I_D = 30\text{ A}$		8.4		$\text{nC}$
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate-to-Source Charge	$Q_{GS}$			3.5		
Gate-to-Drain Charge	$Q_{GD}$			3.3		
Gate Plateau Voltage	$V_{GP}$			3.4		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}$ , $V_{DS} = 15\text{ V}$ ; $I_D = 30\text{ A}$		18.2	

### SWITCHING CHARACTERISTICS (Note 7)

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>SWITCHING CHARACTERISTICS</b> (Note 7)							
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.0		ns	
Rise Time	$t_r$			33			
Turn-Off Delay Time	$t_{d(OFF)}$			15			
Fall Time	$t_f$			4.0			
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		ns	
Rise Time	$t_r$			26			
Turn-Off Delay Time	$t_{d(OFF)}$			19			
Fall Time	$t_f$			3.0			
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.1	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$		28.3		ns	
Charge Time	$t_a$			14.5			
Discharge Time	$t_b$			13.8			
Reverse Recovery Charge	$Q_{RR}$			15.3		nC	

6. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

7. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

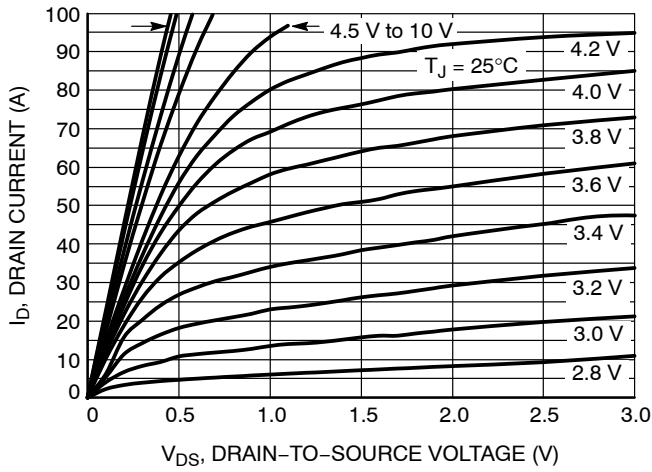


Figure 1. On-Region Characteristics

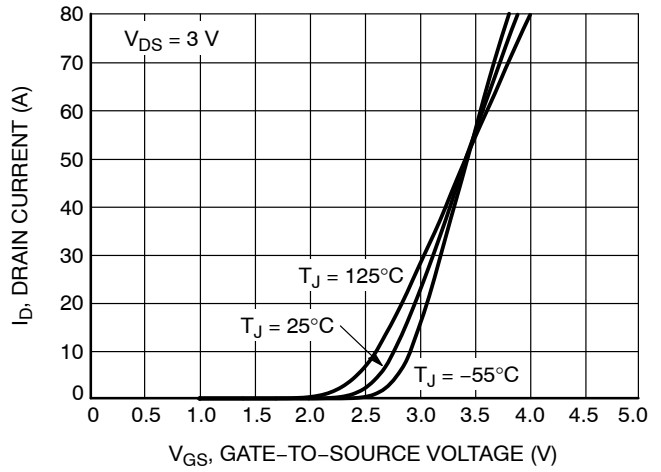


Figure 2. Transfer Characteristics

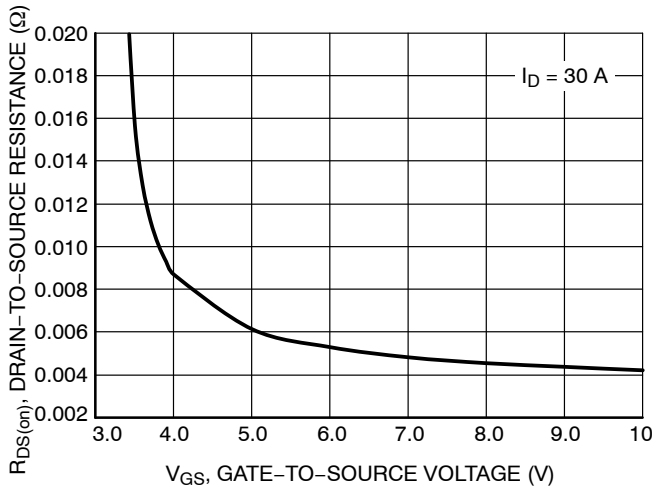


Figure 3. On-Resistance vs.  $V_{GS}$

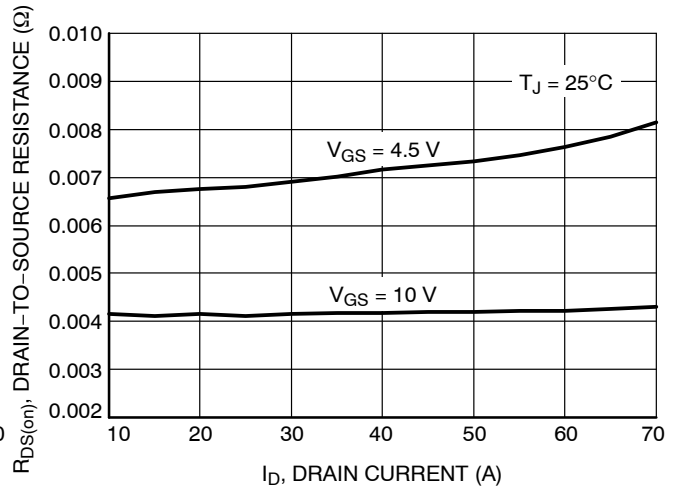


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

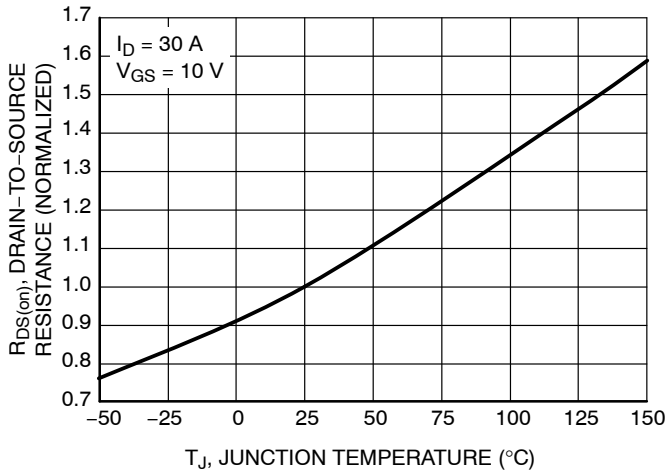


Figure 5. On-Resistance Variation with Temperature

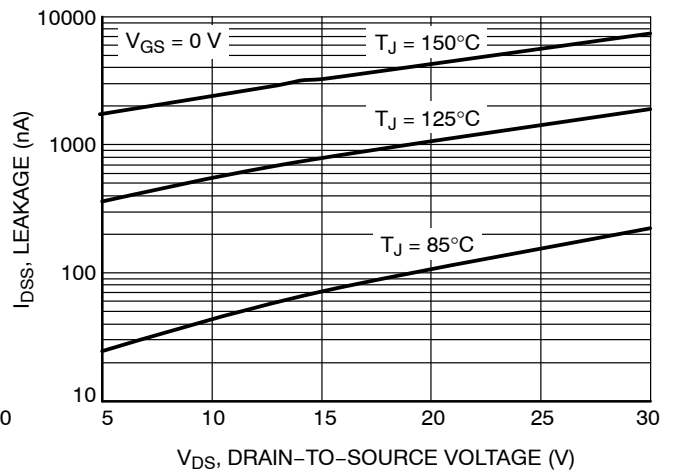


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

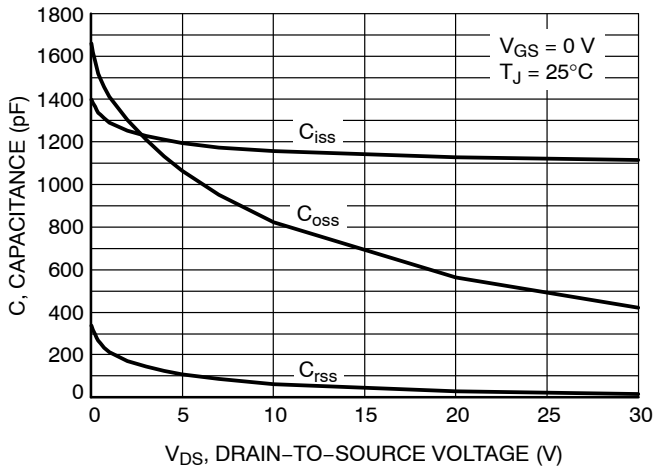


Figure 7. Capacitance Variation

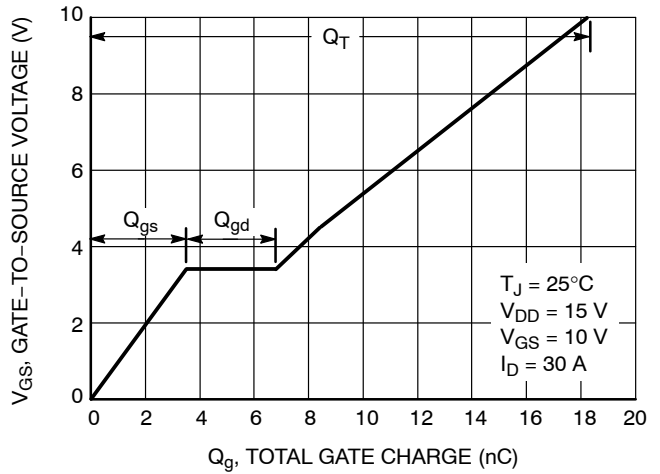


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

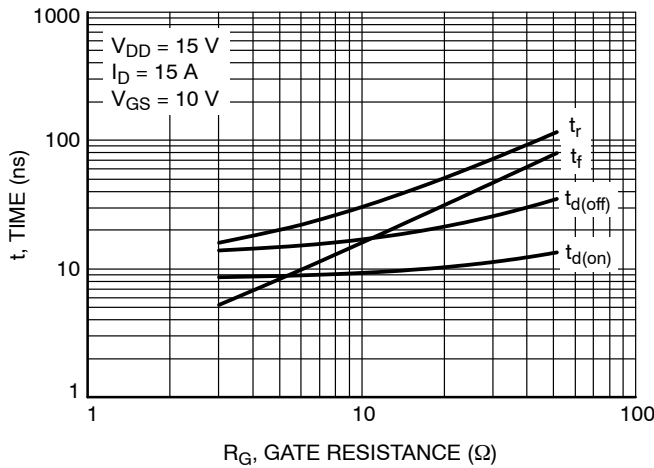


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

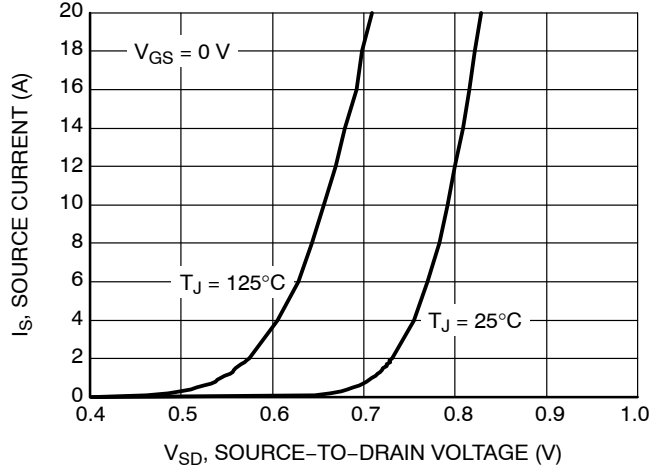


Figure 10. Diode Forward Voltage vs. Current

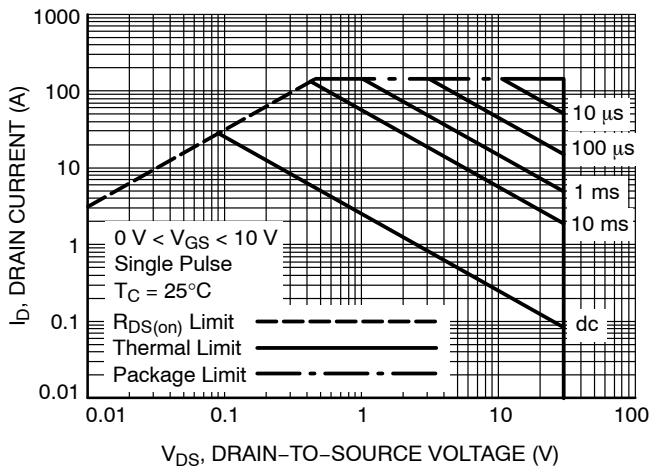


Figure 11. Maximum Rated Forward Biased Safe Operating Area

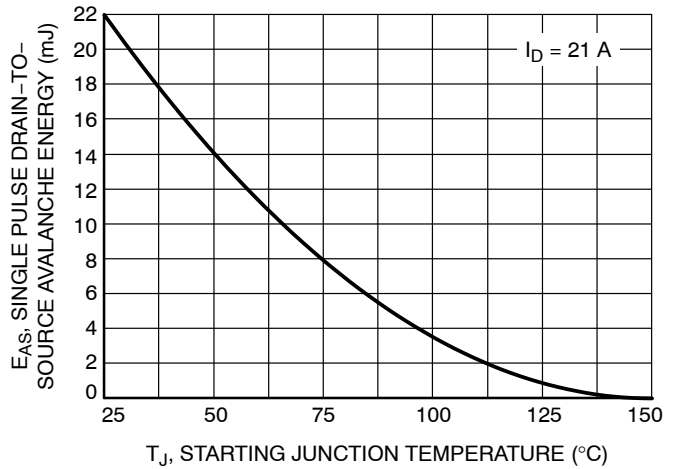


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## TYPICAL CHARACTERISTICS

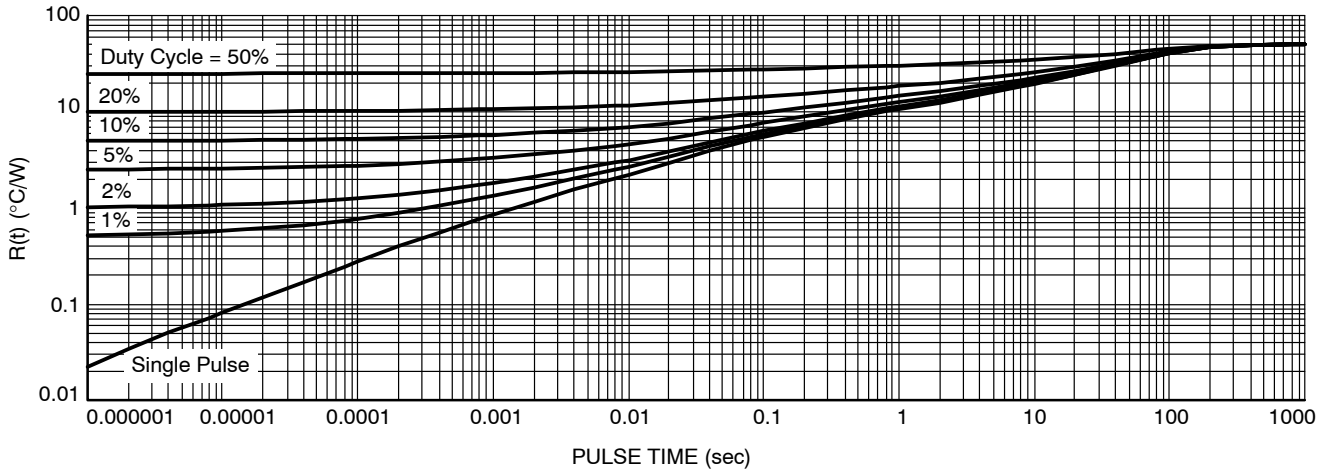


Figure 13. Thermal Response

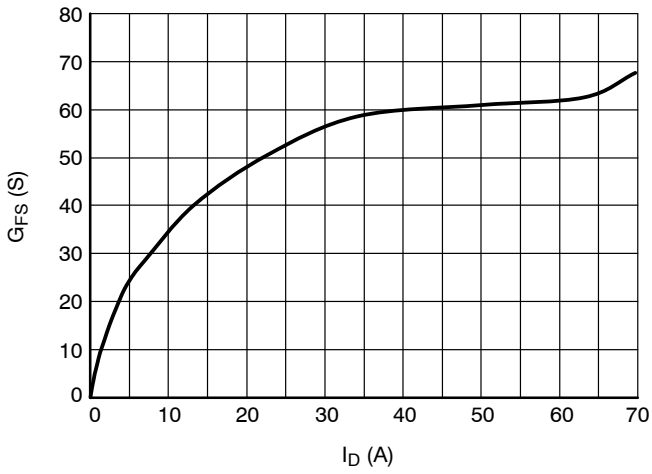


Figure 14.  $G_{FS}$  vs.  $I_D$

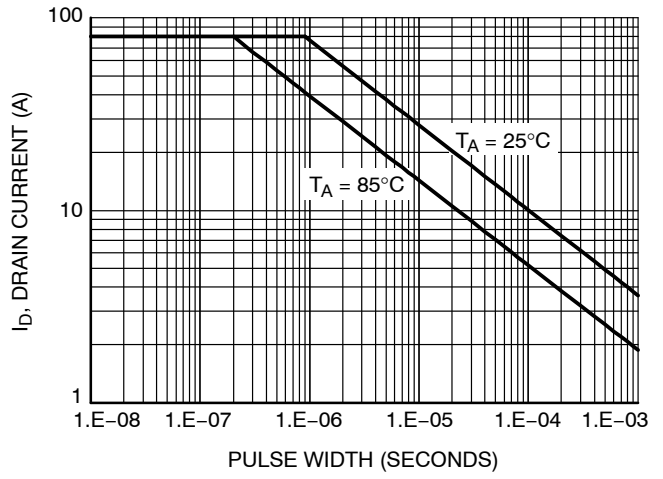
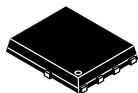


Figure 15. Avalanche Characteristics

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

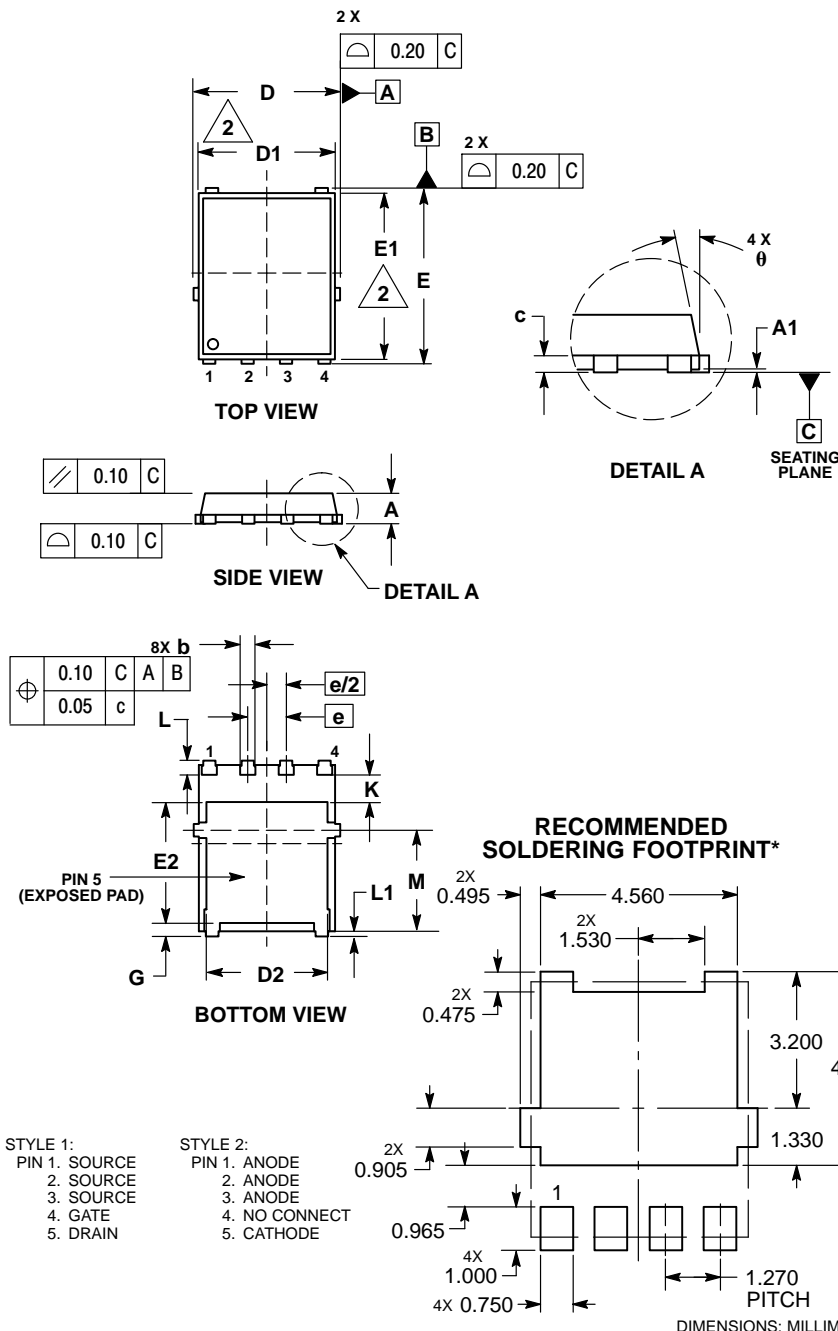
ON Semiconductor®



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)