# **MOSFET** - Power, Single

# **N-Channel**

80 V, 6.7 mΩ, 80 A

# NTMFS6H836N

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	80	V
Gate-to-Source Voltage	9		V <sub>GS</sub>	±20	V
Continuous Drain		T <sub>C</sub> = 25°C	I <sub>D</sub>	74	Α
Current R <sub>θJC</sub> (Notes 1, 3)	Steady	T <sub>C</sub> = 100°C		53	
Power Dissipation	State	T <sub>C</sub> = 25°C	$P_{D}$	89	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		44	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	15	Α
Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady	T <sub>A</sub> = 100°C		11	
Power Dissipation	State	T <sub>A</sub> = 25°C	$P_{D}$	3.7	W
R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 100°C		1.8	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I <sub>DM</sub>	432	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	74	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 4.6 A)			E <sub>AS</sub>	521	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.7	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	40.6	

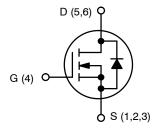
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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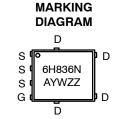
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	$6.7~\mathrm{m}\Omega$ @ $10~\mathrm{V}$	80 A



**N-CHANNEL MOSFET** 



DFN5 (SO-8FL) CASE 488AA STYLE 1



= Assembly Location

= Year W = Work Week ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

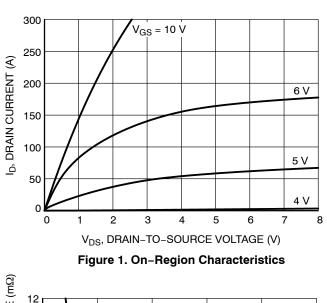
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS							•	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		80			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				39		mV/°C	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C			10		
		V <sub>DS</sub> = 80 V	T <sub>J</sub> = 125°C			100	μΑ	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>G</sub>	<sub>S</sub> = 20 V			100	nA	
ON CHARACTERISTICS (Note 4)								
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D}$	= 95 μΑ	2.0		4.0	V	
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-7.3		mV/°C	
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A		5.6	6.7		
		V <sub>GS</sub> = 6 V	I <sub>D</sub> = 15 A		8.2	11.4	mΩ	
Forward Transconductance	9FS	V <sub>DS</sub> =15 V, I <sub>D</sub> = 25 A			97		S	
CHARGES, CAPACITANCES & GATE RE	SISTANCE							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 40 V			1640		pF	
Output Capacitance	C <sub>OSS</sub>				230			
Reverse Transfer Capacitance	C <sub>RSS</sub>				8.0			
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V; I <sub>D</sub> = 25 A			25		nC	
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V; I <sub>D</sub> = 25 A			5.2			
Gate-to-Source Charge	Q <sub>GS</sub>				8.5			
Gate-to-Drain Charge	$Q_GD$				4.3			
Plateau Voltage	$V_{GP}$				4.9		V	
SWITCHING CHARACTERISTICS (Note	5)					•		
Turn-On Delay Time	t <sub>d(ON)</sub>				16			
Rise Time	t <sub>r</sub>	$V_{GS} = 10 \text{ V}, V_{D}$	s = 64 V.		45		1	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 25 \text{ A}, R_G = 2.5 \Omega$			41		ns -	
Fall Time	t <sub>f</sub>				34			
DRAIN-SOURCE DIODE CHARACTERIS	STICS					•		
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.8	1.2		
			T <sub>J</sub> = 125°C		0.7		_ V	
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dIS/dt = 100 A/μs, I <sub>S</sub> = 25 A			43			
Charge Time	t <sub>a</sub>				29		ns	
Discharge Time	t <sub>b</sub>				15		1	
Reverse Recovery Charge	Q <sub>RR</sub>				54		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

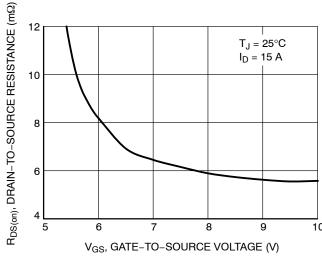
5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



300 250 T<sub>J</sub> = 25°C ID, DRAIN CURRENT (A) 200 150 100 50  $T_J = -55^{\circ}C$ 0 0 5 6 7 2 8 10 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 2. Transfer Characteristics



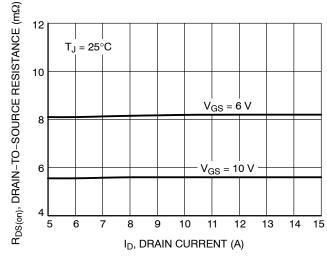
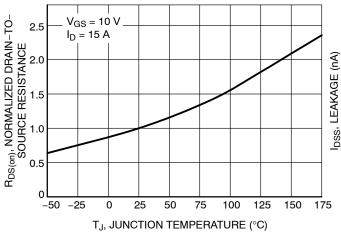


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



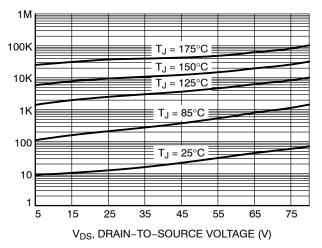


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**

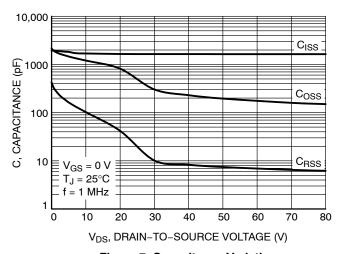


Figure 7. Capacitance Variation

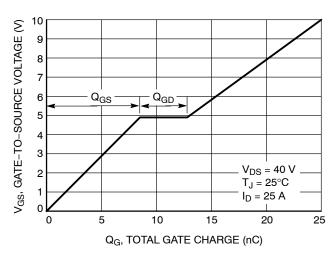


Figure 8. Gate-to-Source Voltage vs. Total Charge

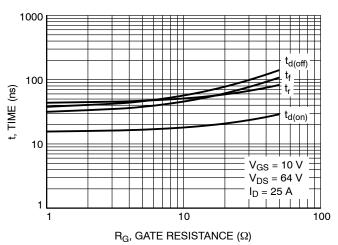


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

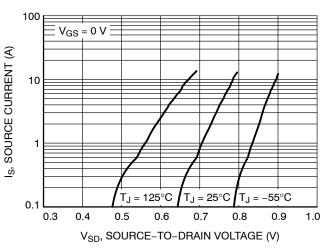


Figure 10. Diode Forward Voltage vs. Current

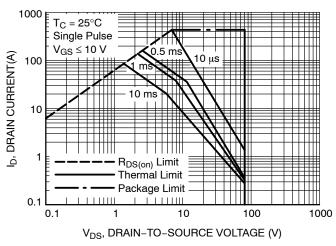


Figure 11. Maximum Rated Forward Biased Safe Operating Area

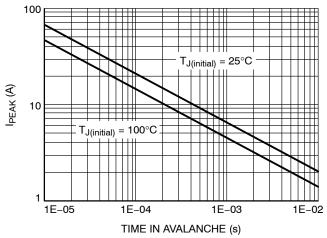


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

### **TYPICAL CHARACTERISTICS**

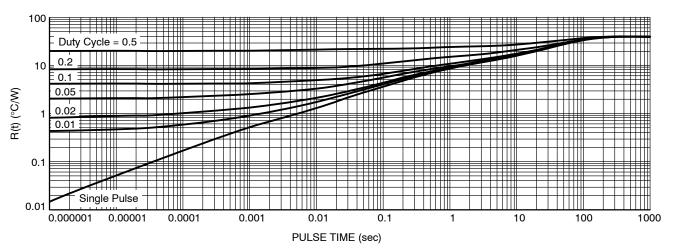


Figure 13. Thermal Characteristics

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTMFS6H836NT1G	6H836N	DFN5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



0.10

0.10

SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

**DATE 25 JUN 2018** 

#### NOTES:

BURRS

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
  CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
M	3.00	3.40	3.80	
A	0 0		12 °	

#### **GENERIC** MARKING DIAGRAM\*



XXXXXX = Specific Device Code

= Assembly Location Α

Υ = Year W = Work Week ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





**DETAIL A** 

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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