NTMYS010N04CL

Power MOSFET
40 V, 10.3 mΩ, 38 A, Single N−Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	38	A
		T_C = 100°C		27	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	28	W
		T_C = 100°C		14	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	14	A
		T_A = 100°C		9.9	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.8	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	187	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to + 175	°C
Source Current (Body Diode)			I_S	24	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 1.9 A)			E_{AS}	62	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

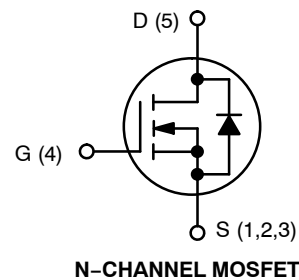| Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	$R_{\theta JC}$	5.3	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.
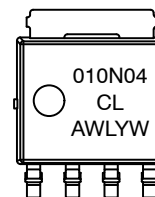
ON Semiconductor®

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	10.3 mΩ @ 10 V	38 A
	17.6 mΩ @ 4.5 V	

D (5)

G (4)

S (1,2,3)

N−CHANNEL MOSFET

MARKING DIAGRAM

LFPAK4 CASE 760AB

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010N04
CL
AWLYW
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010N04CL	= Specific Device Code
A	= Assembly Location
WL	=Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NTMYS010N04CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 20 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		8.6	10.3	mΩ
		V_{GS} = 4.5 V	I_D = 20 A		14.5	17.6	
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 20 A			33		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			570		pF
Output Capacitance	C_{OSS}				230		
Reverse Transfer Capacitance	C_{RSS}				11		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 20 A			7.3		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A			3.4		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.9		nC
Gate−to−Source Charge	Q_{GS}				1.6		
Gate−to−Drain Charge	Q_{GD}				1.0		
Plateau Voltage	V_{GP}				3.4		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 20 A, R_G = 1 Ω			7		ns
Rise Time	t_r				43		
Turn−Off Delay Time	$t_{d(OFF)}$				11		
Fall Time	t_f				2		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.88	1.2	V
			T_J = 125°C		0.79		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 20 A			18		ns
Charge Time	t_a				9		
Discharge Time	t_b				9		
Reverse Recovery Charge	Q_{RR}				6.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width $\leq$ 300 μs, duty cycle $\leq$ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS
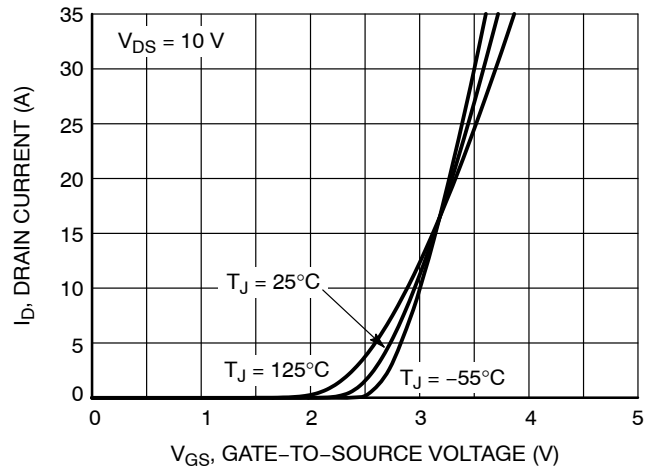

Figure 1. On−Region Characteristics

Figure 2. Transfer Characteristics

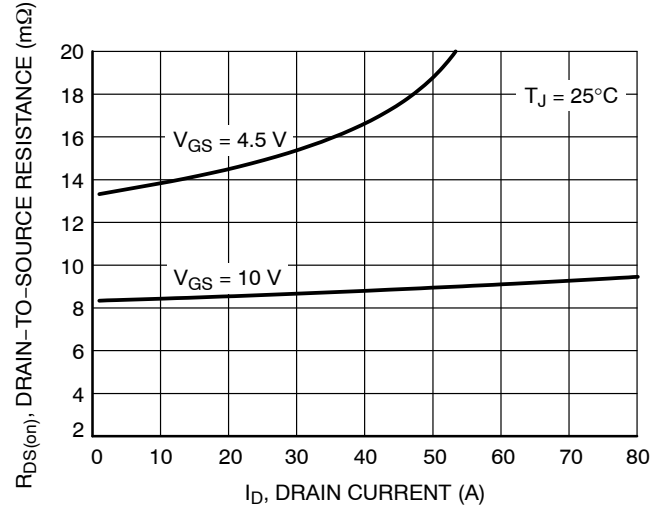Figure 3. On−Resistance vs. Gate−to−Source Voltage

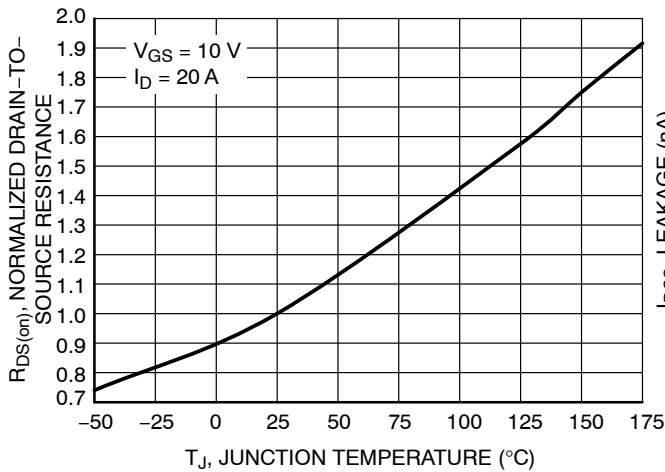Figure 4. On−Resistance vs. Drain Current and Gate Voltage

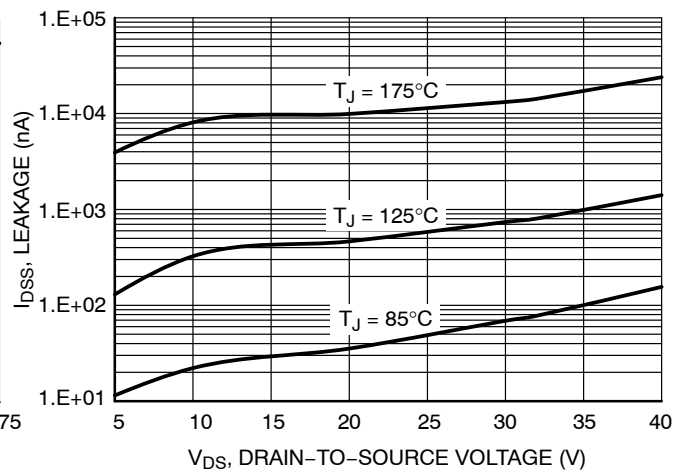Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage

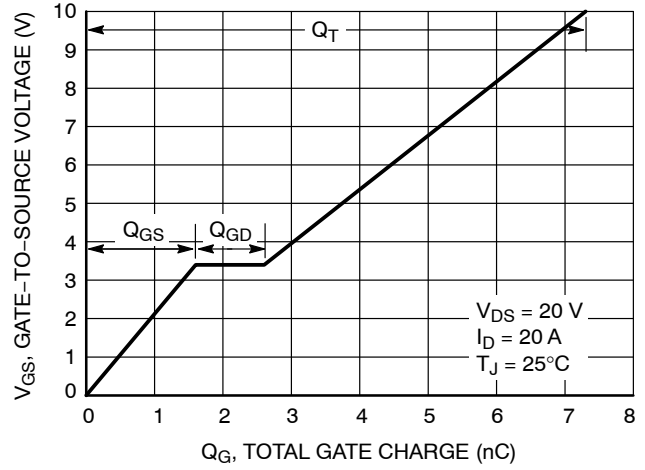## TYPICAL CHARACTERISTICS

Figure 7. Capacitance Variation
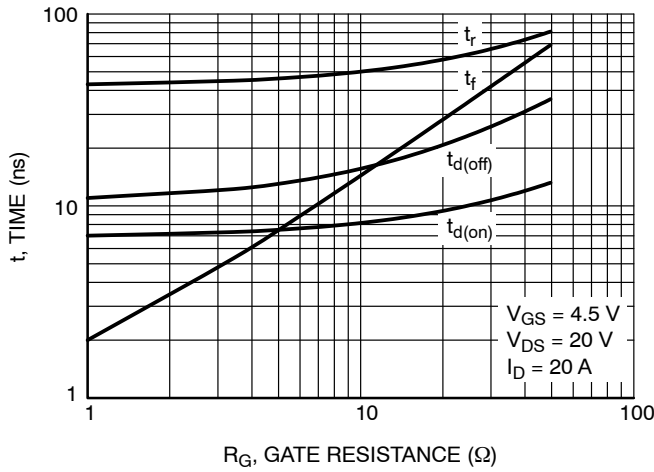
Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
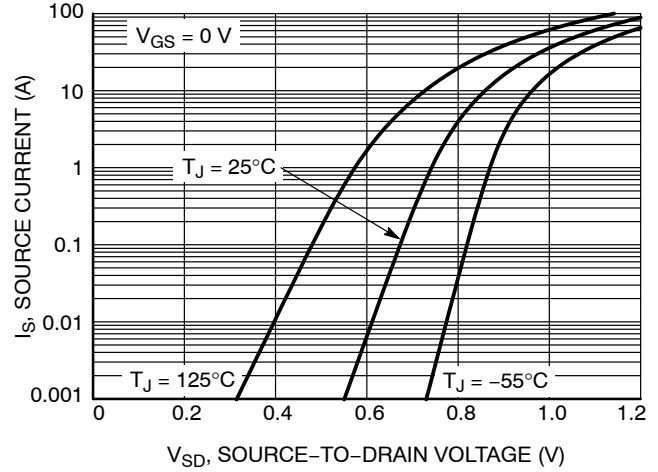
Figure 10. Diode Forward Voltage vs. Current
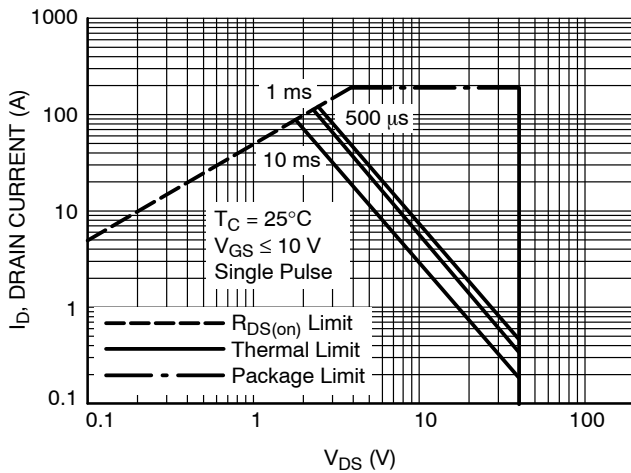
Figure 11. Safe Operating Area
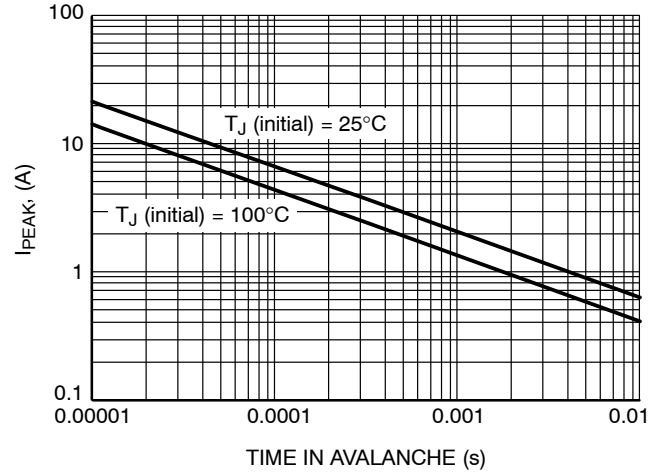
Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS
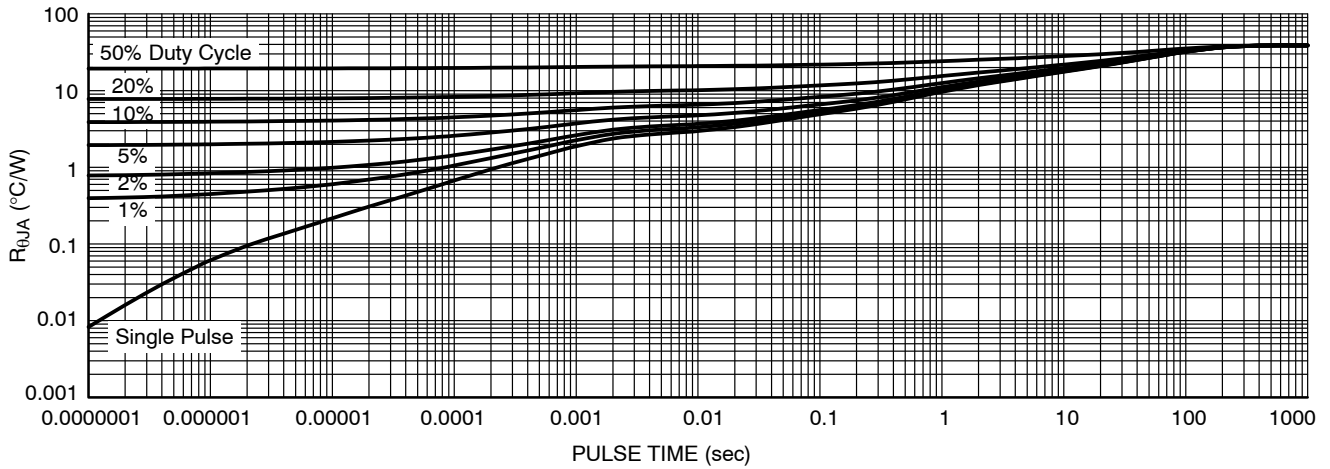
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NTMYS010N04CLTWG	010N04CL	LFPAK4 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LFPAK4 5x6
CASE 760AB
ISSUE C

DATE 19 NOV 2019

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

TOP VIEW

SIDE VIEW

DETAIL 'A'
SCALE: 2:1

BOTTOM VIEW

RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 REF		
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b3	2.00	2.10	2.20
b4	0.70	0.80	0.90
b5	0.55	0.65	0.75
b6	0.31 REF		
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.05	4.15	4.25
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
E	4.80	4.90	5.00
E1	3.10	3.20	3.30
E2	5.00	5.15	5.30
e	1.27 BSC		
1/2e	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.80	0.90	1.00
L2	0.90	1.10	1.30
L3	0.00	0.10	0.20
q	0°	4°	8°

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
AWLYW

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON82777G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	LFPAK4 5x6		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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