

# NUP8011MU

## ESD Protection Diode Array Low Clamping Voltage

This integrated surge protection device is designed for applications requiring transient overvoltage protection. It is intended for use in sensitive equipment such as computers, printers, business machines, communication systems, and other applications. Its integrated design provides very effective and reliable protection for eight separate lines using only one package. These devices are ideal for situations where board space is at a premium.

### Features

- Low Clamping Voltage
- UDFN Package, 1.2 x 1.8 mm
- Standoff Voltage: 4.3 V
- Low Leakage Current
- IEC61000-4-2, Level 4 ESD Protection
- Moisture Sensitivity Level 1
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Protects the Line Against Transient Voltage Conditions
- Minimize Power Consumption of the System
- Minimize PCB Board Space

### Applications

- ESD Protection for Data Lines
- Wireless Phones
- Handheld Products
- Notebook Computers
- LCD Displays

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Value	Unit
Steady State Power – 1 Diode (Note 1)	$P_D$	380	mW
Thermal Resistance, Junction-to-Ambient Above $25^\circ\text{C}$ , Derate	$R_{\theta JA}$	327 3.05	$^\circ\text{C}/\text{W}$ $\text{mW}/^\circ\text{C}$
Maximum Junction Temperature	$T_{Jmax}$	150	$^\circ\text{C}$
Operating Temperature Range	$T_{OP}$	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature (10 seconds duration)	$T_L$	260	$^\circ\text{C}$
IEC 61000-4-2 (ESD)Contact		$\pm 8.0$	kV
Machine Model – Class C	MM	400	V
Human Body Model – Class 3B	HBM	8.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

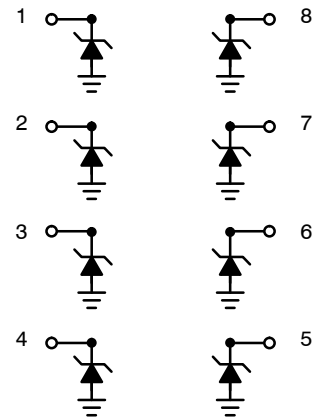
1. Only 1 diode under power. For all 4 diodes under power,  $P_D$  will be 25%.  
Mounted on FR-4 board with min pad.

See Application Note AND8308/D for further description of survivability specs.



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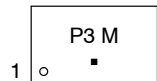


(Top View)



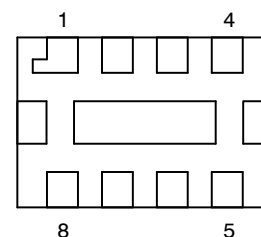
UDFN8  
CASE 517AD

### MARKING DIAGRAM



- P3 = Specific Device Code
- M = Month Code
- = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping
NUP8011MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel

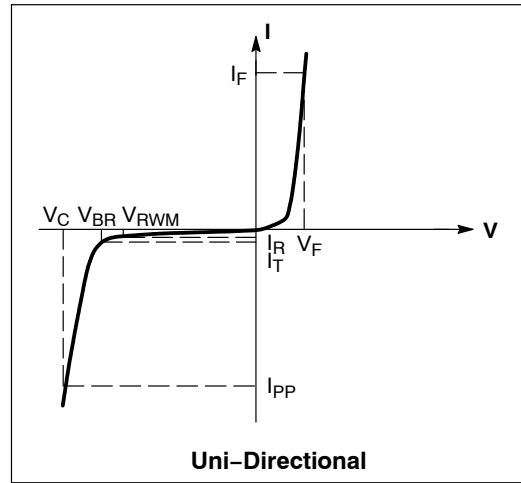
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NUP8011MU

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and $f = 1.0$ MHz



\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Device	Device Marking	Breakdown Voltage $V_{BR}$ @ 1 mA (V)			Leakage Current $I_{RM}$ @ $V_{RM}$		Typ Capacitance @ 0 V Bias (pF) (Note 2)		Typ Capacitance @ 3 V Bias (pF) (Note 2)		$V_C$ Per IEC61000-4-2 (Note 3)
		Min	Nom	Max	$V_{RWM}$	$I_{RWM}$ ( $\mu\text{A}$ )	Typ	Max	Typ	Max	
NUP8011MUTAG	P3	6.47	6.8	7.14	4.3	1.0	12	14	6.7	9.5	Figures 1 and 2 (See Below)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Capacitance of one diode at  $f = 1$  MHz,  $V_R = 0$  V,  $T_A = 25^\circ\text{C}$
- For test procedure see Figures 3 and 4 and Application Note AND8307/D.

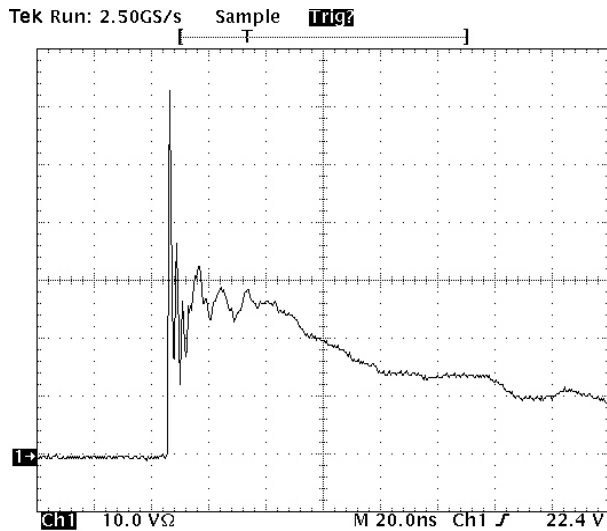


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

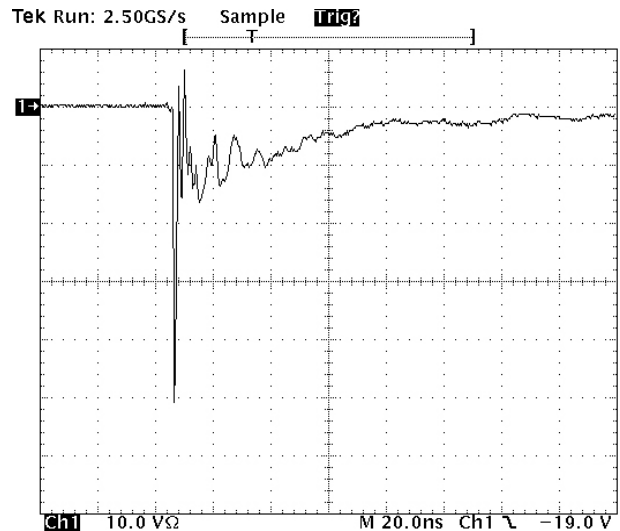


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 3. IEC61000-4-2 Spec

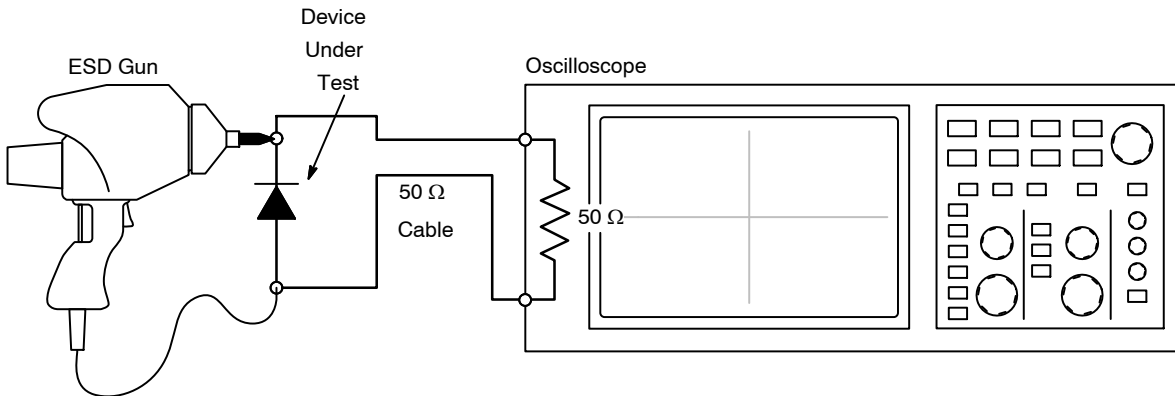


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

**ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

# NUP8011MU

## TYPICAL ELECTRICAL CHARACTERISTICS

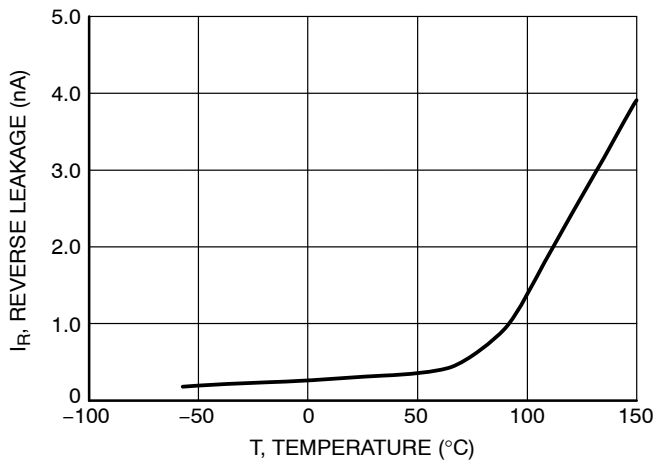


Figure 5. Reverse Leakage versus Temperature

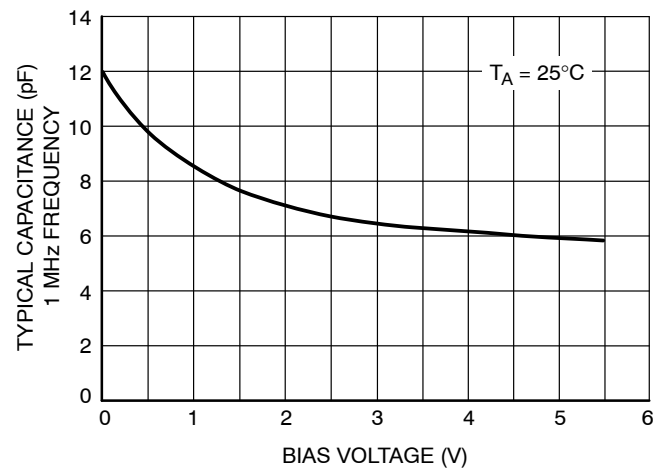


Figure 6. Capacitance

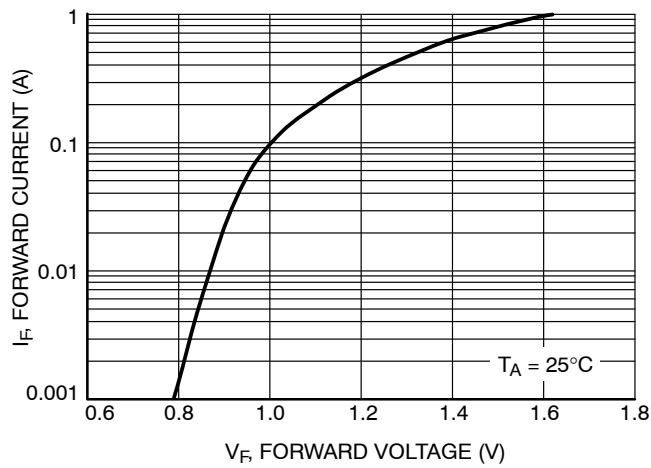


Figure 7. Forward Voltage

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

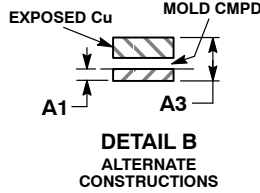
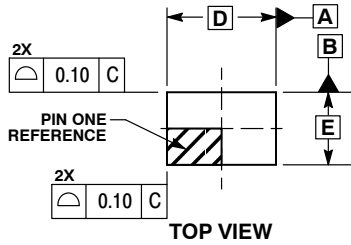
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SCALE 4:1

### UDFN8 1.8x1.2, 0.4P CASE 517AD ISSUE D

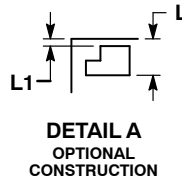
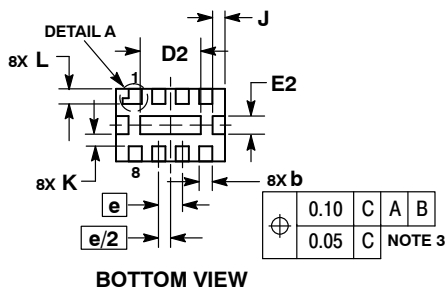
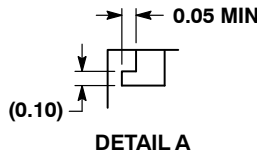
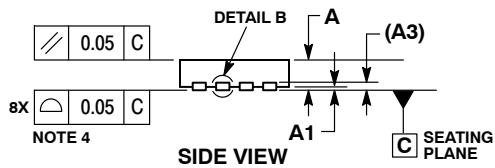
DATE 23 OCT 2012



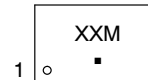
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
D2	0.90	1.10
E2	0.20	0.30
J	0.19	REF
K	0.20	TYP
L	0.20	0.30
L1	---	0.10



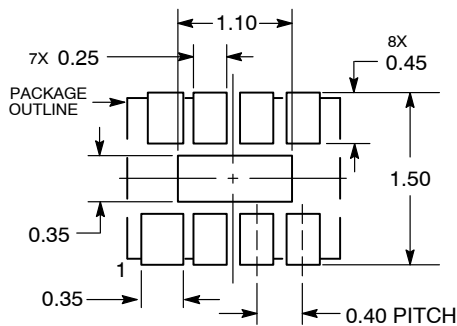
### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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[ESD119B1W01005E6327XTSA1](#) [ESD5V0J4-TP](#) [ESD5V0L1B02VH6327XTSA1](#) [ESD7451N2T5G](#) [19180-510](#) [CPDT-5V0USP-HF](#)  
[3.0SMCJ33CA-F](#) [3.0SMCJ36A-F](#) [HSPC16701B02TP](#) [D3V3Q1B2DLP3-7](#) [D55V0M1B2WS-7](#) [DESD5V0U1BL-7B](#) [DRTR5V0U4SL-7](#)  
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