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# NVATS5A107PLZ

## Power MOSFET

–40 V, 17 mΩ, –55 A, P-Channel



ON Semiconductor®

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Automotive Power MOSFET designed for compact and efficient designs and including high thermal performance. AEC-Q101 qualified MOSFET and PPAP capable suitable for automotive applications.

### Features

- Low On-Resistance
- High Current Capability
- 100% Avalanche Tested
- AEC-Q101 qualified and PPAP capable
- ATPAK package is pin-compatible with DPAK (TO-252)
- Pb-Free, Halogen Free and RoHS compliance

### Typical Applications

- Reverse Battery Protection
- Load Switch
- Automotive Front Lighting
- Automotive Body Controllers

### SPECIFICATIONS

ABSOLUTE MAXIMUM RATING at Ta = 25°C (Note 1)

Parameter	Symbol	Value	Unit
Drain to Source Voltage	V <sub>DSS</sub>	–40	V
Gate to Source Voltage	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D</sub>	–55	A
Drain Current (Pulse) PW ≤ 10 μs, duty cycle ≤ 1%	I <sub>DP</sub>	–165	A
Power Dissipation Tc = 25°C	P <sub>D</sub>	60	W
Operating Junction and Storage Temperature	T <sub>j</sub> , T <sub>stg</sub>	–55 to +175	°C
Avalanche Energy (Single Pulse) (Note 2)	E <sub>AS</sub>	80	mJ
Avalanche Current (Note 3)	I <sub>AV</sub>	–25	A

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2 : V<sub>DD</sub> = –10 V, L = 200 μH, I<sub>AV</sub> = –25 A

3 : L ≤ 200 μH, Single pulse

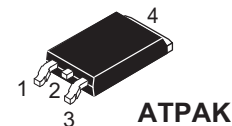
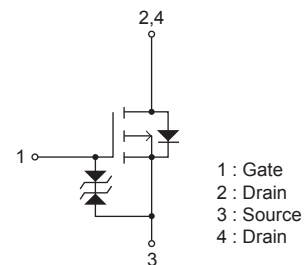
### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Case Steady State (Tc = 25°C)	R <sub>θJC</sub>	2.5	°C/W
Junction to Ambient (Note 4)	R <sub>θJA</sub>	80.1	°C/W

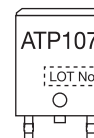
Note 4 : Surface mounted on FR4 board using a 130 mm<sup>2</sup>, 1 oz. Cu pad.

V <sub>DSS</sub>	R <sub>DS(on)</sub> Max	I <sub>D</sub> Max
–40 V	17 mΩ @ –10 V	–55 A
	26 mΩ @ –4.5 V	

### ELECTRICAL CONNECTION P-Channel



### MARKING



### ORDERING INFORMATION

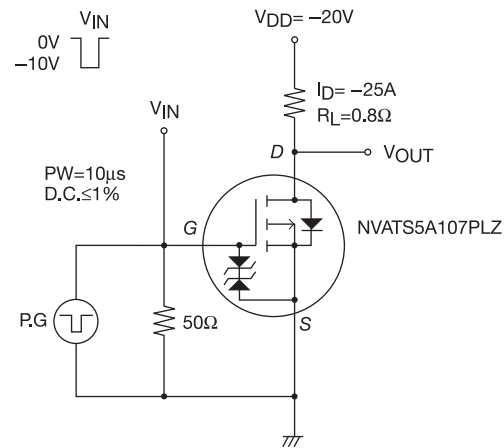
See detailed ordering and shipping information on page 6 of this data sheet.

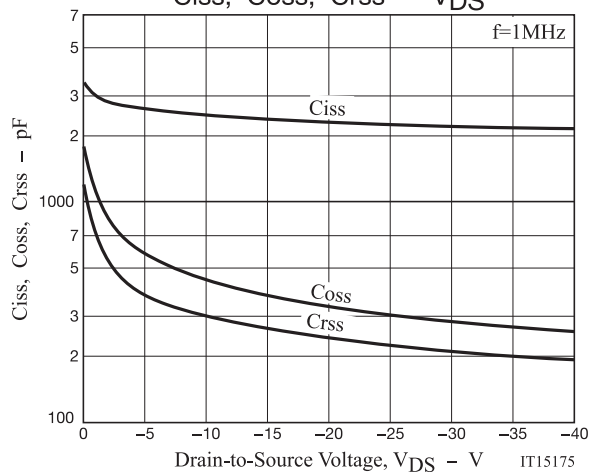
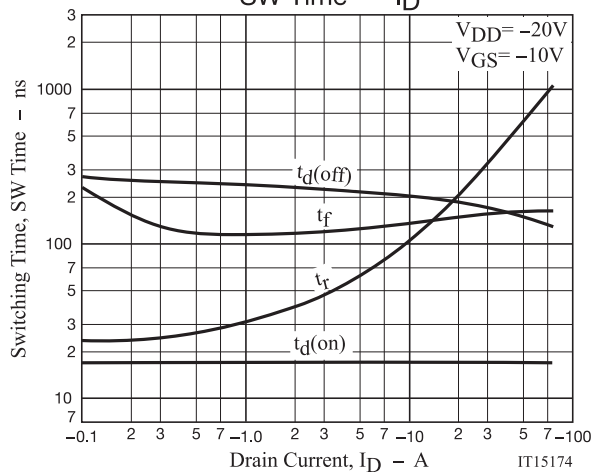
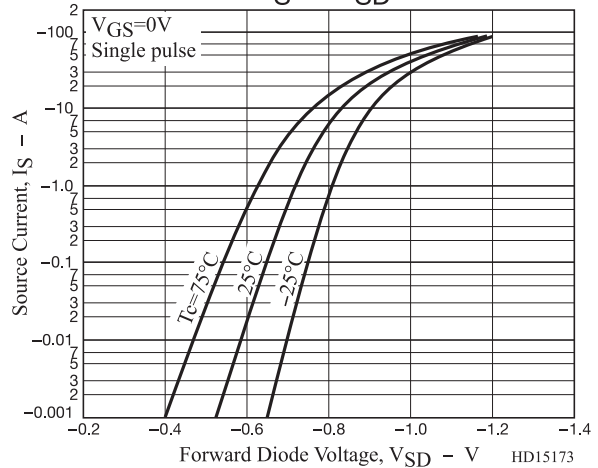
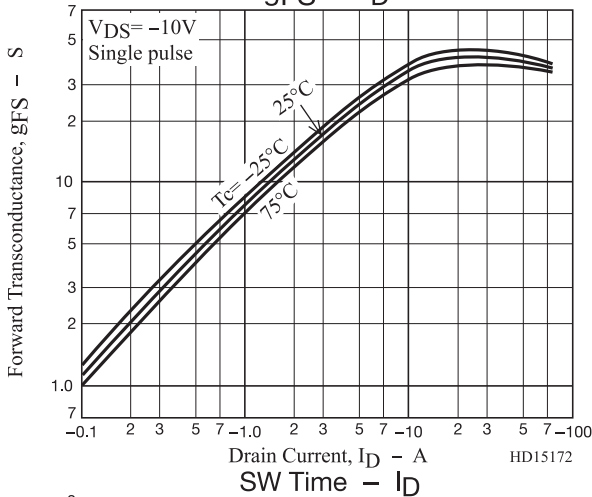
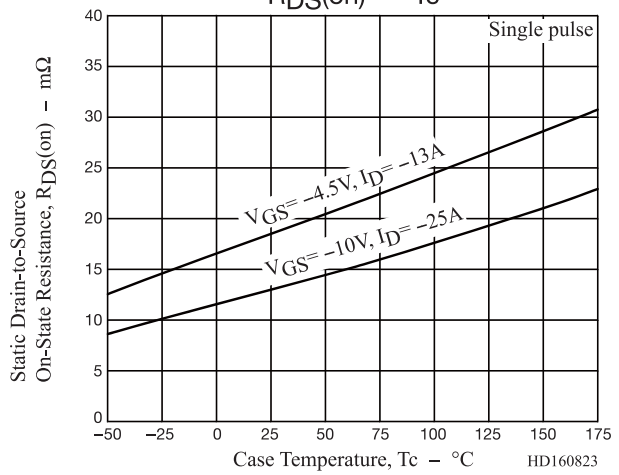
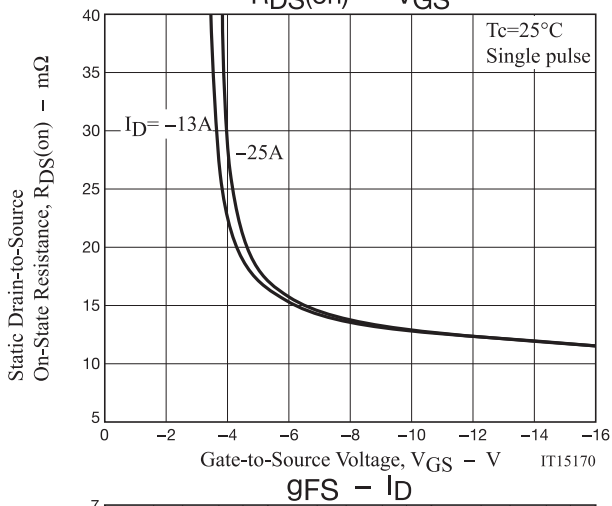
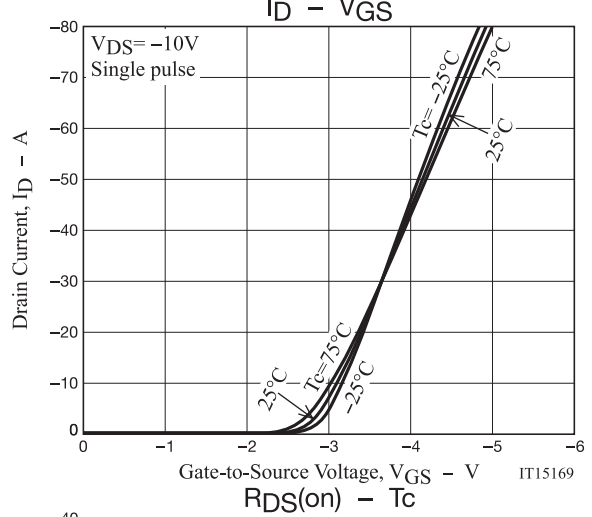
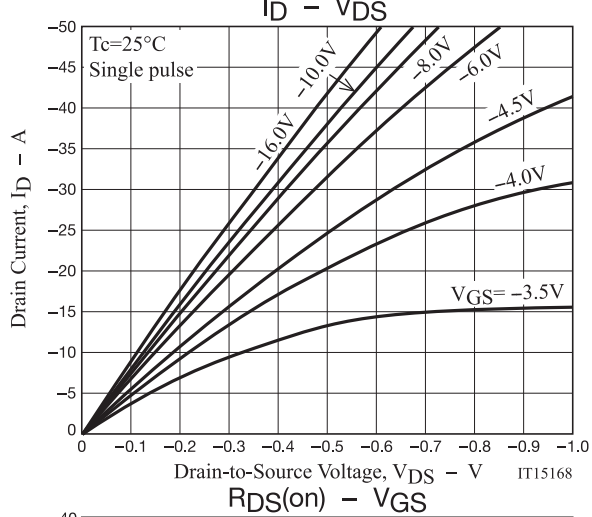
**ELECTRICAL CHARACTERISTICS at Ta = 25°C (Note 5)**

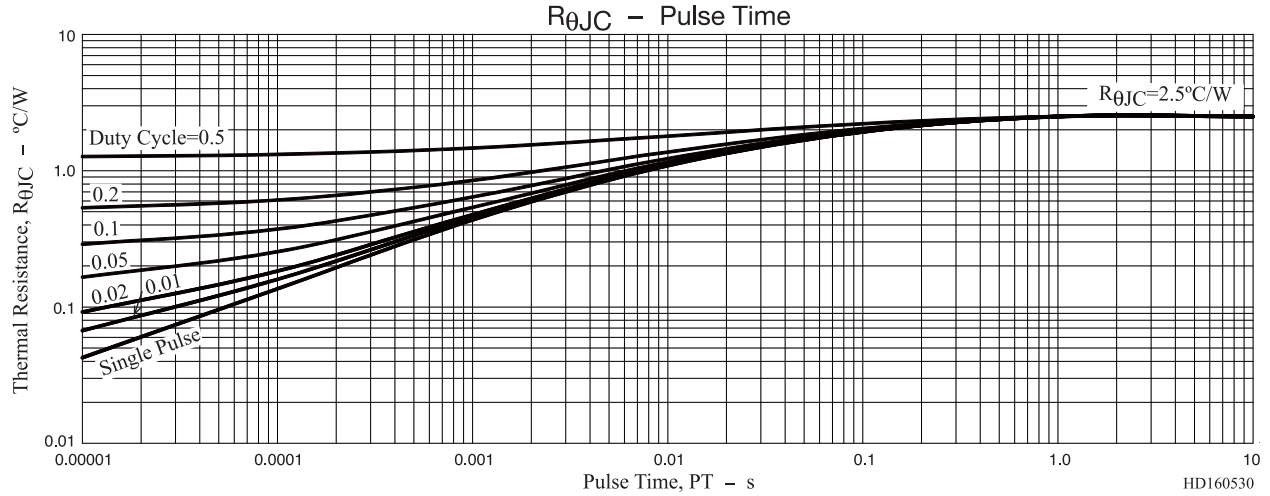
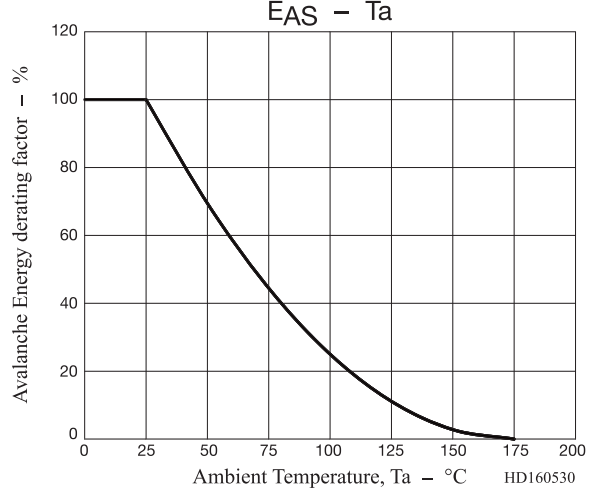
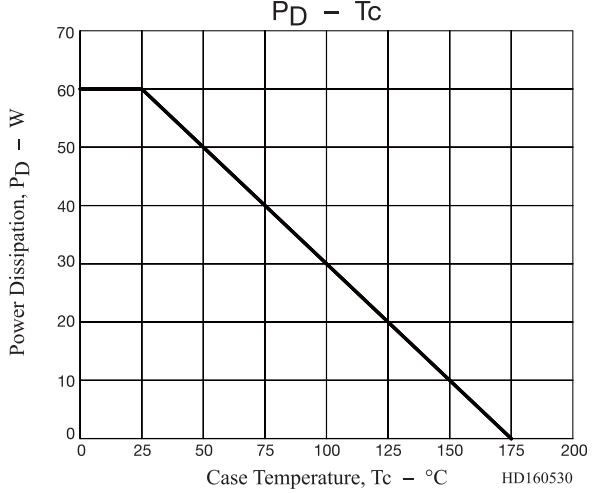
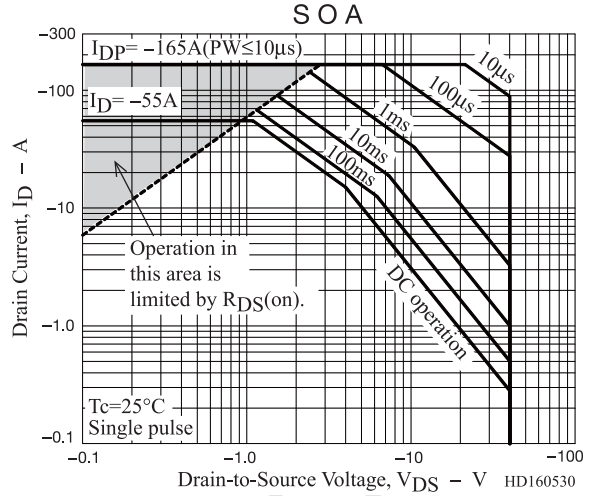
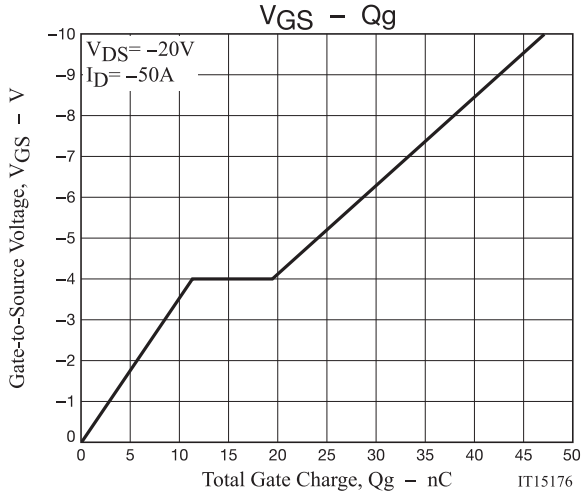
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	V(BR)DSS	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0 V	-40			V
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-1	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.2		-2.6	V
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -25 A		40		S
Static Drain to Source On-State Resistance	R <sub>DS(on)1</sub>	I <sub>D</sub> = -25 A, V <sub>GS</sub> = -10 V		13	17	mΩ
	R <sub>DS(on)2</sub>	I <sub>D</sub> = -13 A, V <sub>GS</sub> = -4.5 V		18.5	26	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -20 V, f = 1 MHz		2,400		pF
Output Capacitance	C <sub>oss</sub>			330		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			240		pF
Turn-ON Delay Time	t <sub>d(on)</sub>	See Fig.1		17		ns
Rise Time	t <sub>r</sub>			260		ns
Turn-OFF Delay Time	t <sub>d(off)</sub>			190		ns
Fall Time	t <sub>f</sub>			160		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A		47		nC
Gate to Source Charge	Q <sub>gs</sub>			11.5		nC
Gate to Drain "Miller" Charge	Q <sub>gd</sub>			8		nC
Forward Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = -50 A, V <sub>GS</sub> = 0 V		-1.02	-1.5	V

Note 5 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

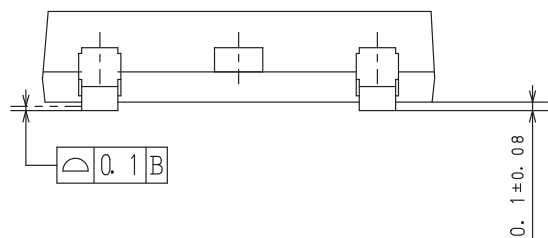
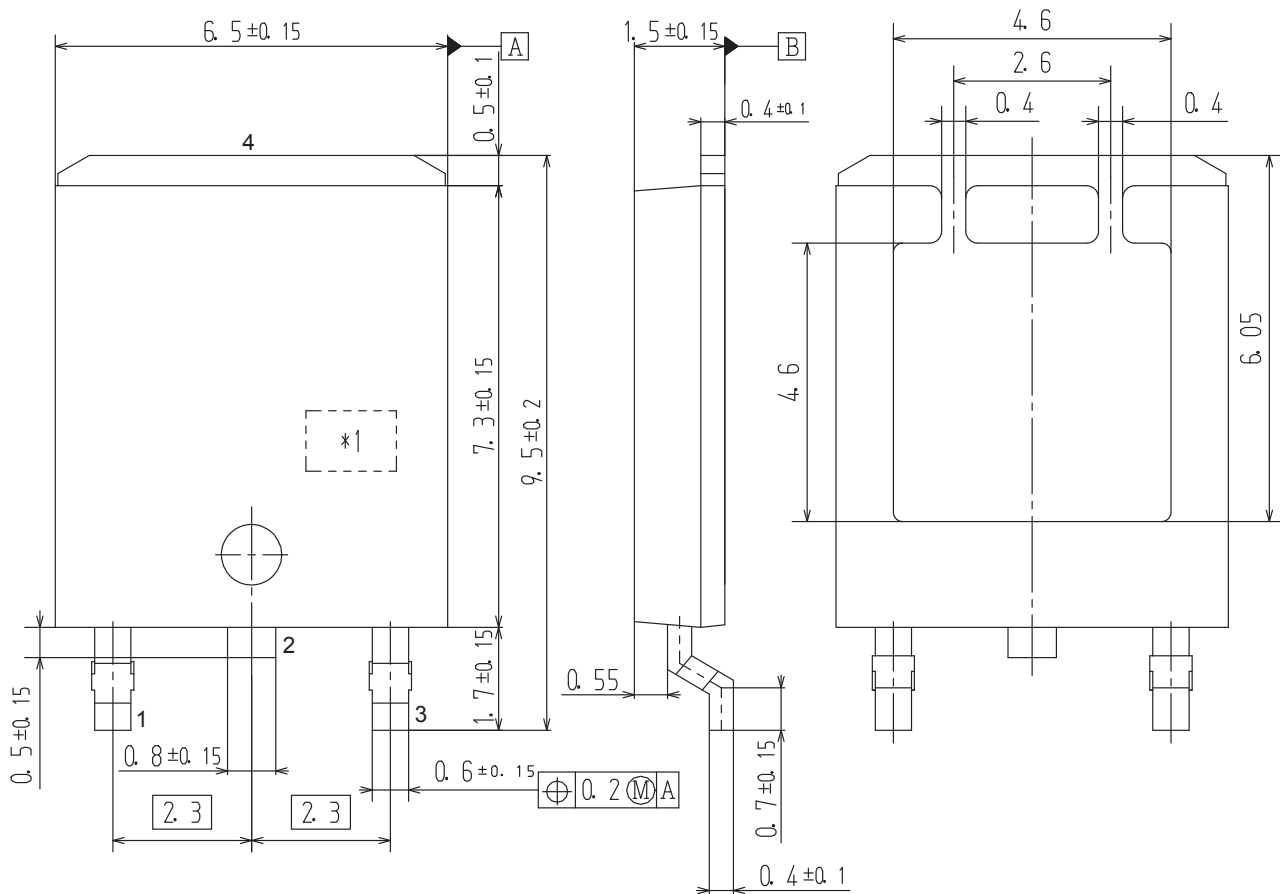
**Fig.1 Switching Time Test Circuit**







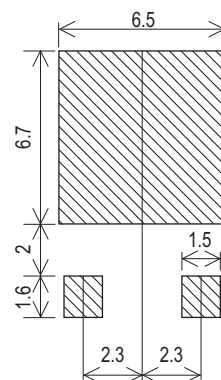
**DPAK (Single Gauge) / ATPAK**  
CASE 369AM  
ISSUE O



Pin2 is idle pin with electrical designation only carried

\*1: Lot indication

**RECOMMENDED SOLDERING FOOTPRINT**



- 1 : Gate
- 2 : Drain
- 3 : Source
- 4 : Drain

**ORDERING INFORMATION**

Device	Marking	Package	Shipping (Qty / Packing)
NVATS5A107PLZT4G	ATP107	DPAK(Single Gauge) / ATPAK (Pb-Free / Halogen Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

Note on usage : Since the NVATS5A107PLZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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