MOSFET - N-Channel Shielded Gate PowerTrench®
150 V, 15 mΩ, 61.3 A

NVDS015N15MC

ON Semiconductor®

www.onsemi.com

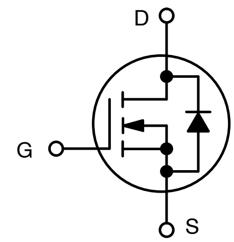
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 15 mΩ at V_{GS} = 10 V, I_D = 29 A
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Primary Side for 48 V Isolated Bus
- SR for MV Secondary Applications

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	15 mΩ @ 10 V	61.3 A



N−CHANNEL MOSFET

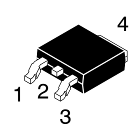
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	150	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	61.3	A
		T_C = 100°C		43.4	
Power Dissipation $R_{\theta JC}$ (Note 2)		T_C = 25°C	P_D	107.1	W
		T_C = 100°C		53.6	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	10.5	A
		T_A = 100°C		7.4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	382	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	89.3	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 4.4 A)			E_{AS}	1301	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

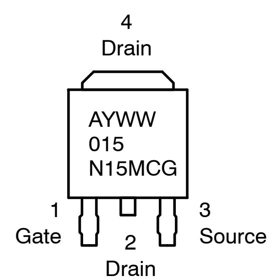
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM



DPAK
CASE 369C



015N15MCG	=	Specific Device Code
A	=	Assembly Location
Y	=	Year
WW	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NVDS015N15MCT4G	DPAK (Pb−Free)	2500 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State (Note 2)	$R_{\theta JC}$	1.4	°C/W
Junction–to–Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	47.9	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		150			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			83		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V	T_J = 25°C			1.0	μA
			T_J = 125°C		1.1		
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 162 μA		2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 162 μA, ref to 25°C			−8.2		mV/°C
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 29 A			11.8	15	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 29 A			58		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 75 V			2120		pF
Output Capacitance	C_{OSS}				595		
Reverse Transfer Capacitance	C_{RSS}				10.5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 75 V; I_D = 29 A			27		nC
Threshold Gate Charge	$Q_{G(TH)}$				7		
Gate–to–Source Charge	Q_{GS}				11		
Gate–to–Drain Charge	Q_{GD}				4		
Plateau Voltage	V_{GP}				5.5		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 75 V, I_D = 29 A, R_G = 6 Ω			16		ns
Rise Time	t_r				5		
Turn–Off Delay Time	$t_{d(OFF)}$				21		
Fall Time	t_f				4		
DRAIN–SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 29 A	T_J = 25°C		0.89	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V, dI_S/dt = 300 A/μs, I_S = 29 A			49		ns
Reverse Recovery Charge	Q_{RR}				197		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V, dI_S/dt = 1000 A/μs, I_S = 29 A			34		ns
Reverse Recovery Charge	Q_{RR}				345		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

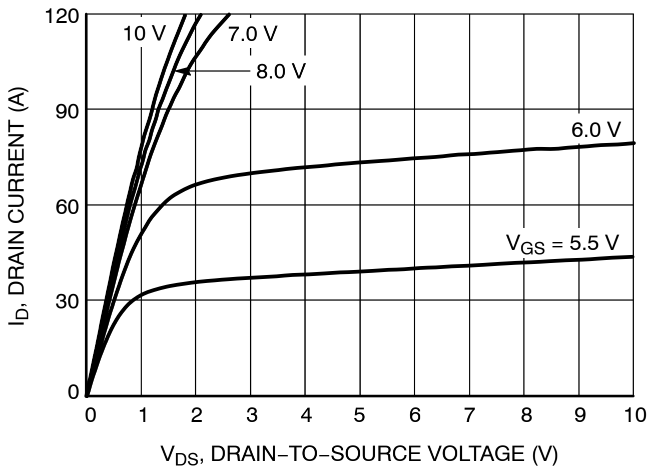


Figure 1. On−Region Characteristics

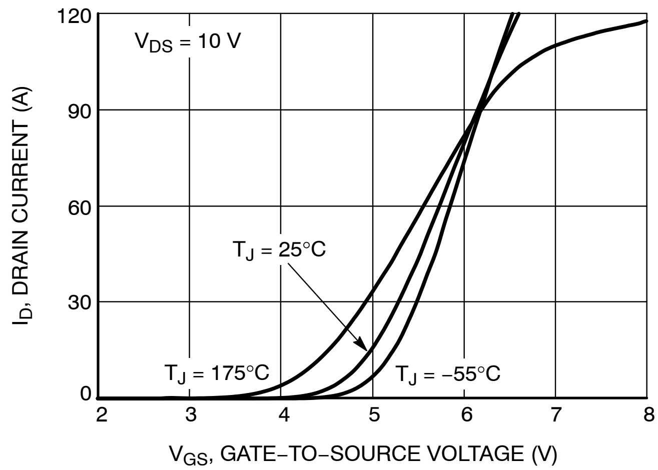


Figure 2. Transfer Characteristics

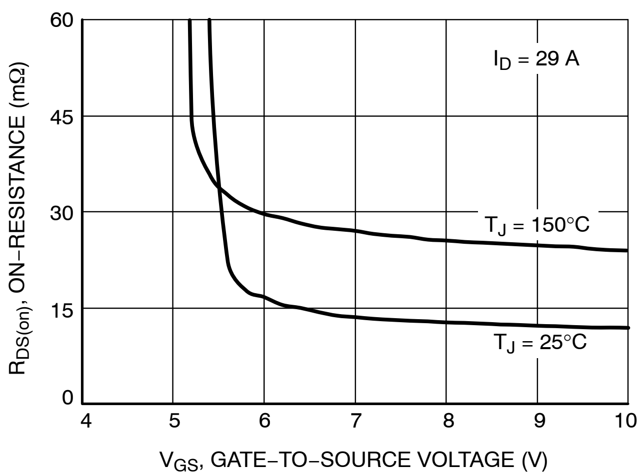


Figure 3. On−Resistance vs. Gate−to−Source Voltage

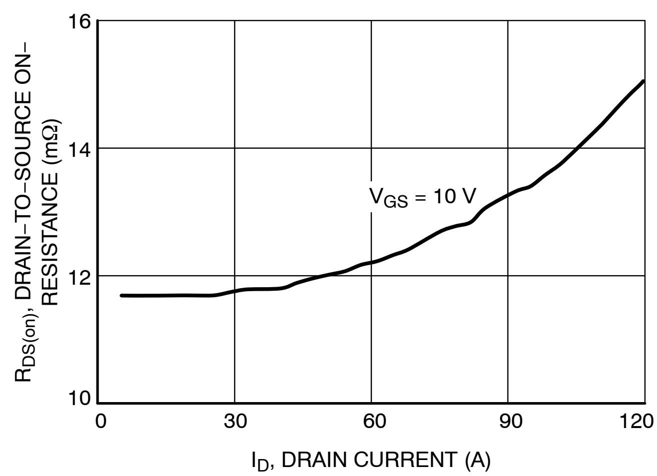


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

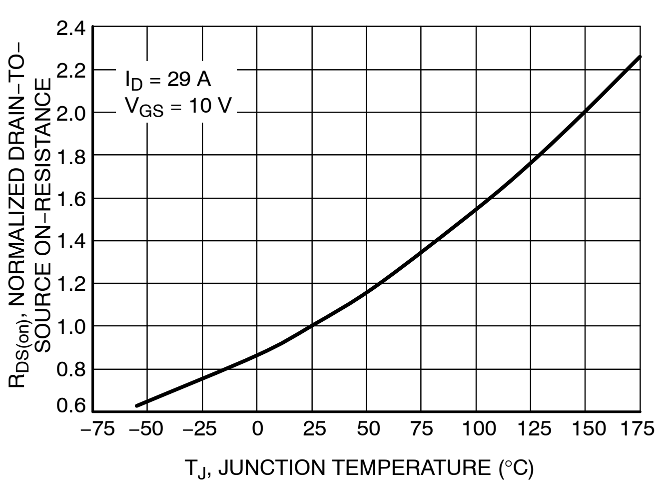


Figure 5. Normalized On−Resistance vs. Junction Temperature

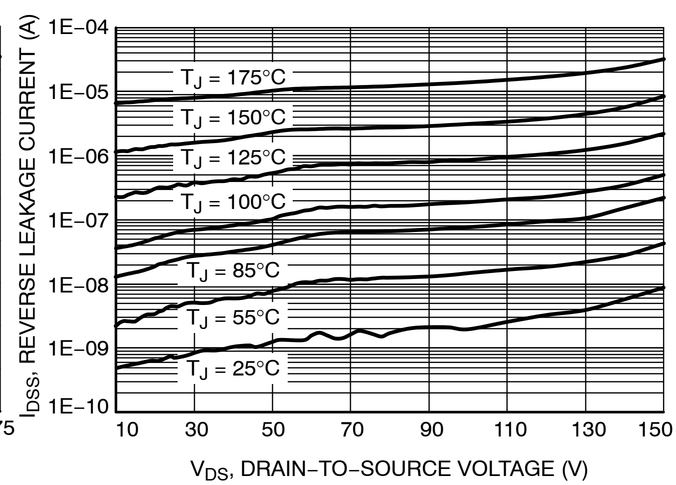


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

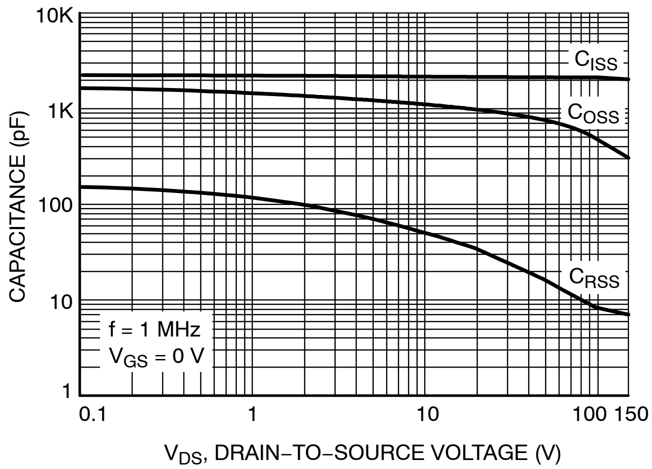


Figure 7. Capacitance vs. Drain−to−Source Voltage

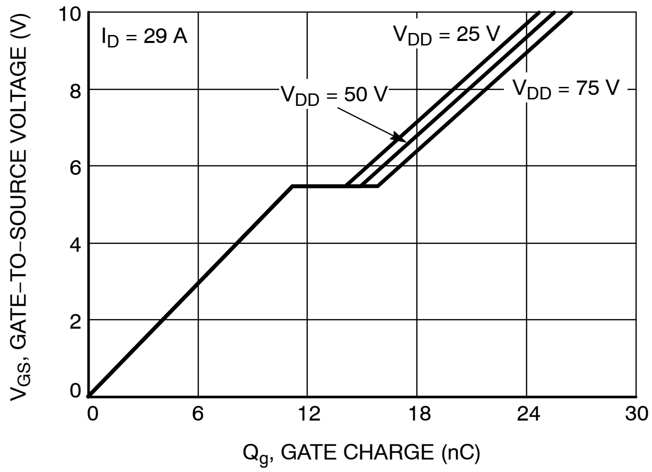


Figure 8. Gate Charge Characteristics

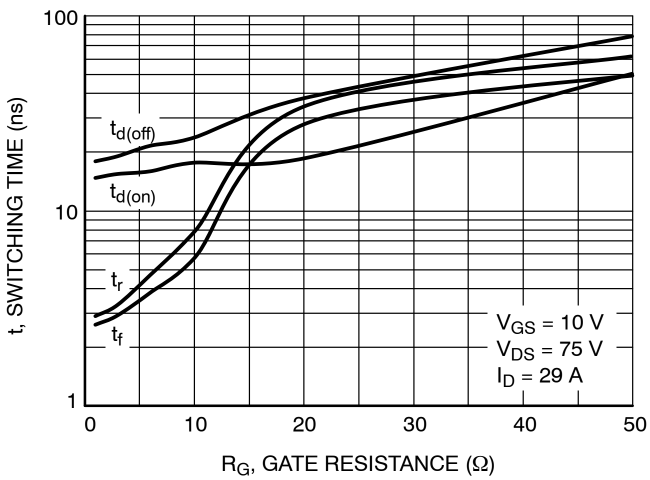


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

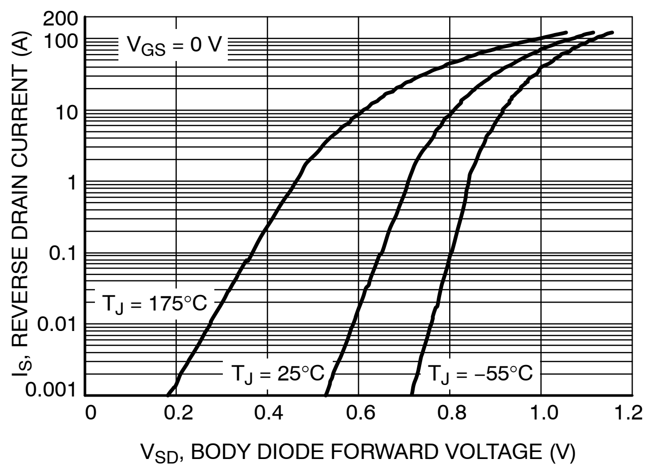


Figure 10. Source−to−Drain Diode Forward Voltage vs. Source Current

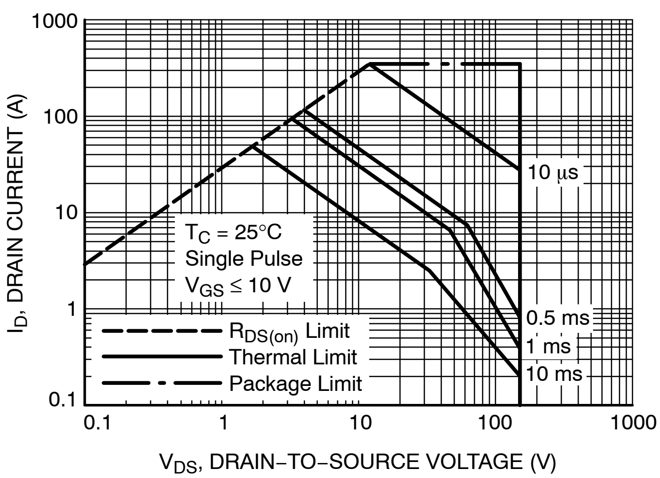


Figure 11. Forward Bias Safe Operating Area

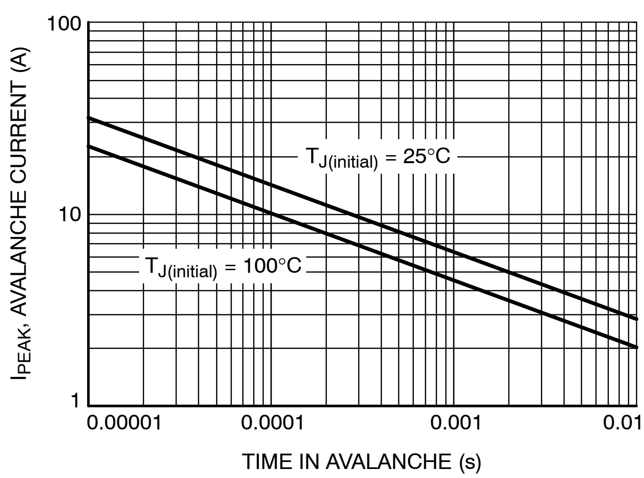


Figure 12. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS

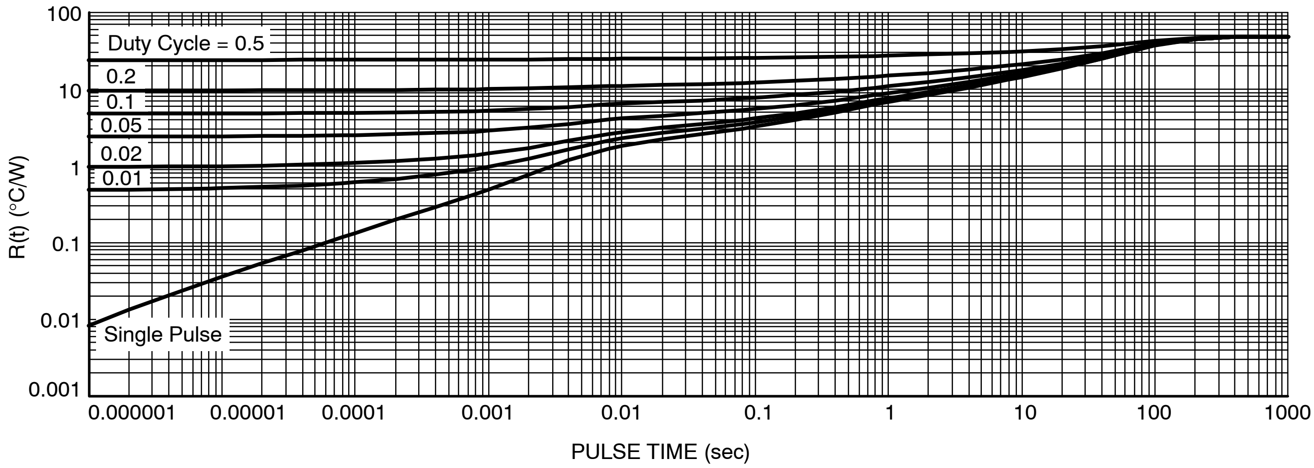
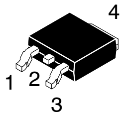


Figure 13. Transient Thermal Impedance

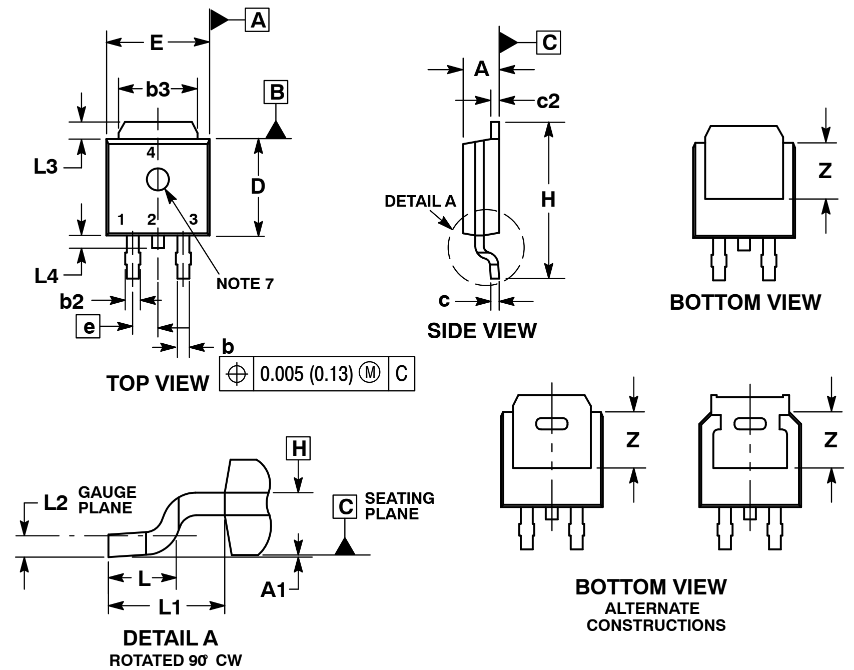


SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C
ISSUE F

DATE 21 JUL 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

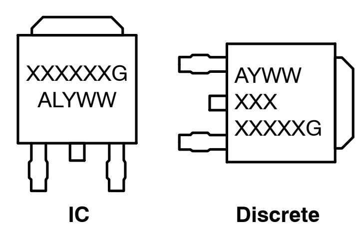
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

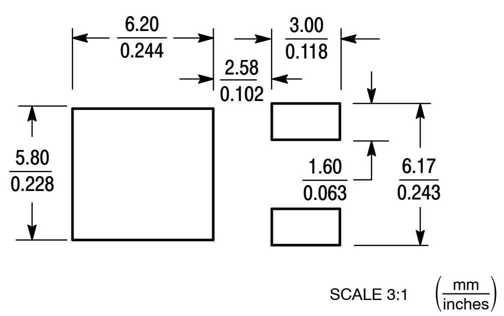
GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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TECHNICAL SUPPORT
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Phone: 011 421 33 790 2910

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