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MOSFET – Power, N-Channel, SUPERFET III, FRFET
650 V, 36 A, 95 mΩ

NVHL095N65S3F

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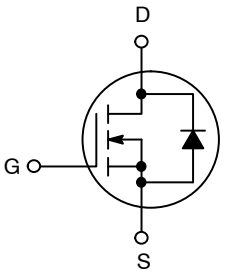
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	95 mΩ @ 10 V	36 A



Description

SUPERFET III MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

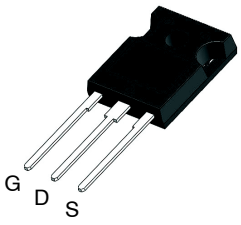
SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 78 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 65 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 597 pF)
- 100% Avalanche Tested
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS Compliant

Applications

- Automotive On Board Charger HEV−EV
- Automotive DC/DC Converter HEV−EV



TO−247 long leads
CASE 340CX

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
NVHL095N65S3F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25°C)	36	A
		– Continuous (T_C = 100°C)	22.8	
I_{DM}	Drain Current	– Pulsed (Note 1)	90	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		440	mJ
I_{AS}	Avalanche Current (Note 2)		4.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.72	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	272	W
		– Derate Above 25°C	2.176	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 4.6 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le$ 18 A, di/dt ≤ 200 A/μs, $V_{DD} \le$ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.46	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVHL095N65S3F	NVHL095N65S3F	TO−247	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D = 15 mA, Referenced to 25°C		640		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		12		
Gate to Body Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.86 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 0.86 mA		−7		mV/°C
Static Drain to Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		78	95	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 18 A		19		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		3020		pF
Output Capacitance	C_{oss}			61		
Reverse Transfer Capacitance	C_{rss}			7.0		
Effective Output Capacitance	$C_{oss(eff.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		597		pF
Energy Related Output Capacitance	$C_{oss(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		107		pF
Total Gate Charge at 10V	$Q_{g(tot)}$	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 18 A (Note 4)		66		nC
Threshold Gate Charge	$Q_{g(th)}$			13		
Gate to Source Gate Charge	Q_{gs}			22		
Gate to Drain “Miller” Charge	Q_{gd}			26		
Equivalent Series Resistance	ESR	f = 1 MHz		2.4		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 400 V, I_D = 18 A, R_g = 2.2 Ω (Note 4)		26		ns
Turn-On Rise Time	t_r			26		ns
Turn-Off Delay Time	$t_{d(off)}$			62		ns
Turn-Off Fall Time	t_f			4.0		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
Maximum Continuous Source to Drain Diode Forward Current	I_S	V_{GS} = 0 V			36	A
Maximum Pulsed Source to Drain Diode Forward Current	I_{SM}	V_{GS} = 0 V			90	A
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 18 A			1.3	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 100 A/μs, I_{SD} = 18 A		97		ns
Charge Time	t_a			78		
Discharge Time	t_b			19		
Reverse Recovery Charge	Q_{rr}			349		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

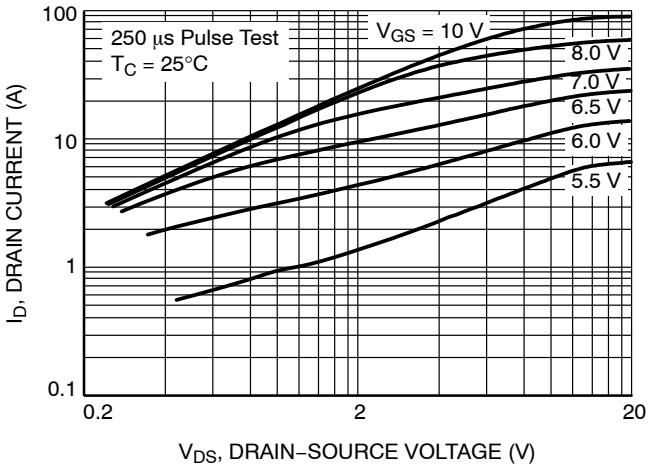


Figure 1. On−Region Characteristics 25°C

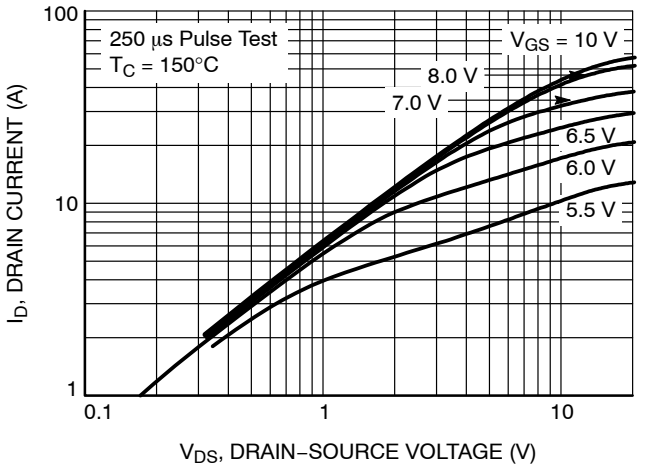


Figure 2. On−Region Characteristics 150°C

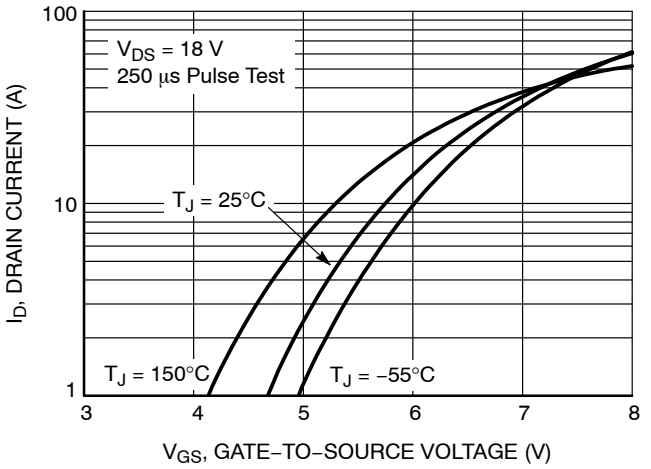


Figure 3. Transfer Characteristics

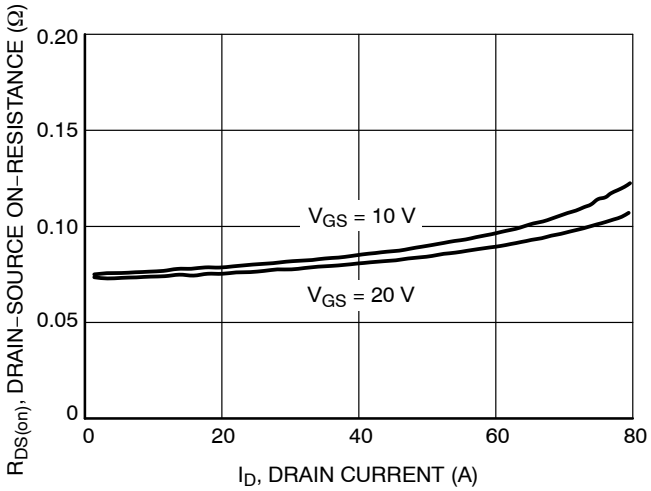


Figure 4. On−Resistance Variation vs. Drain Current and Gate Voltage

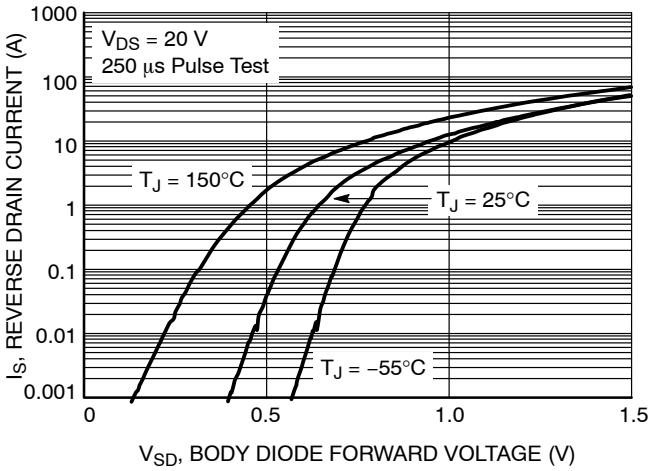


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

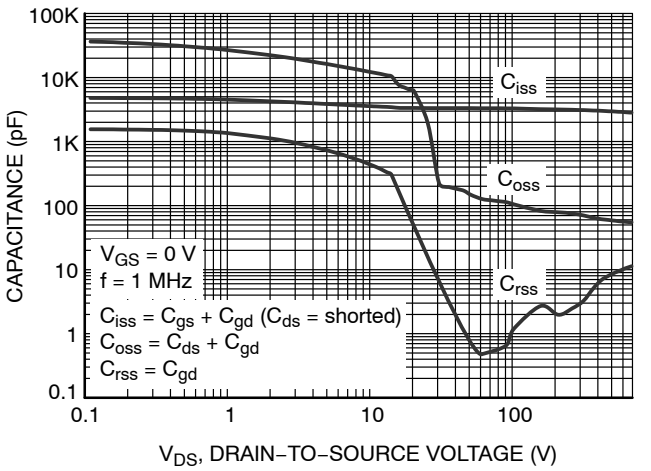


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

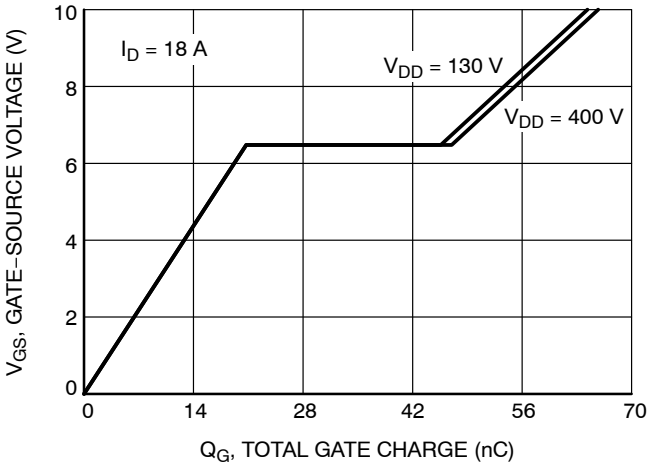


Figure 7. Gate Charge Characteristics

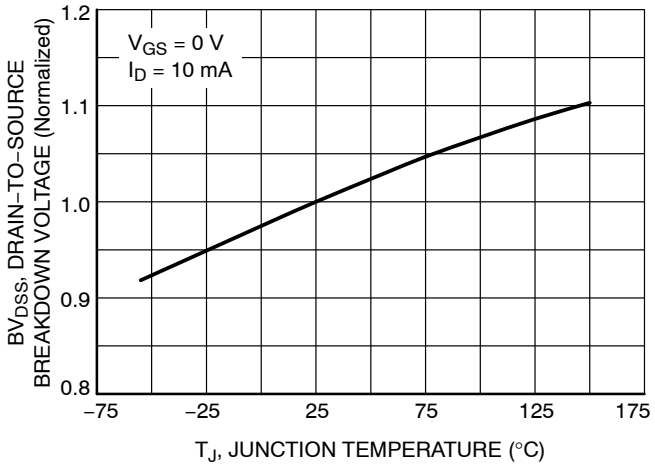


Figure 8. Breakdown Voltage Variation vs. Temperature

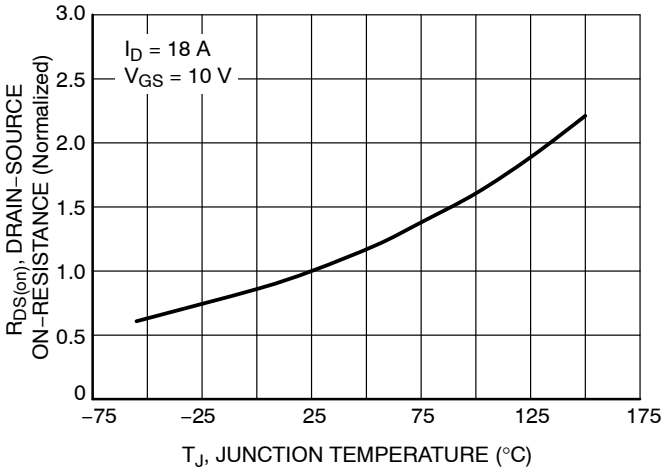


Figure 9. On−Resistance Variation vs. Temperature

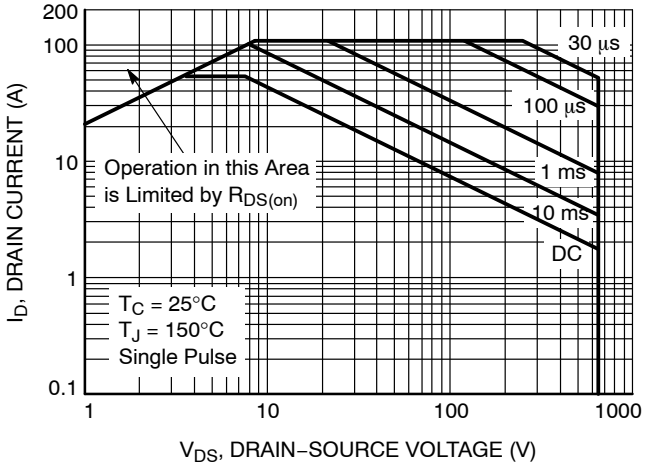


Figure 10. Maximum Safe Operating Area

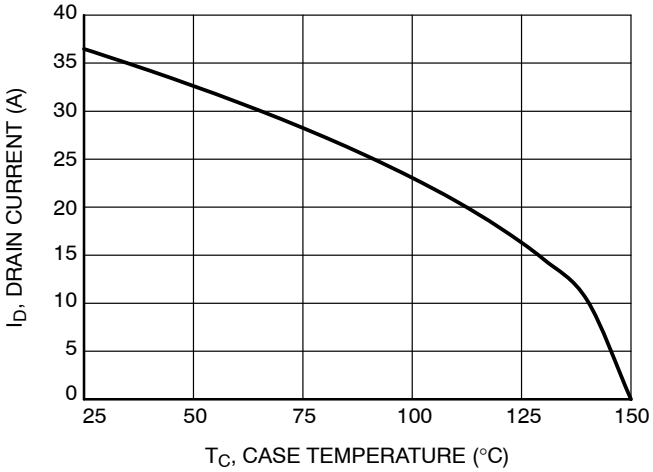


Figure 11. Maximum Drain Current vs. Case Temperature

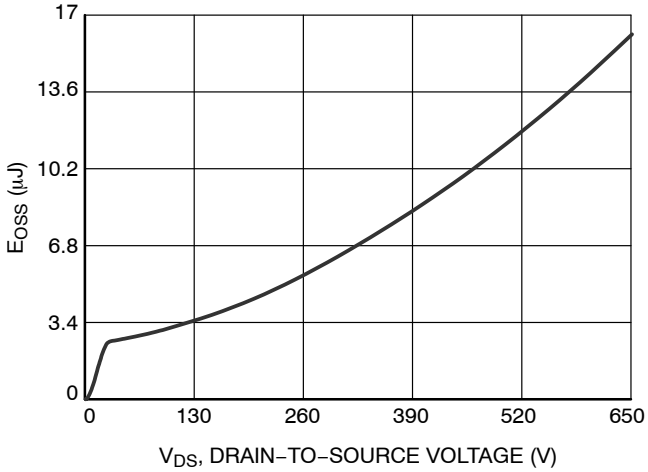


Figure 12. E_{OSS} vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

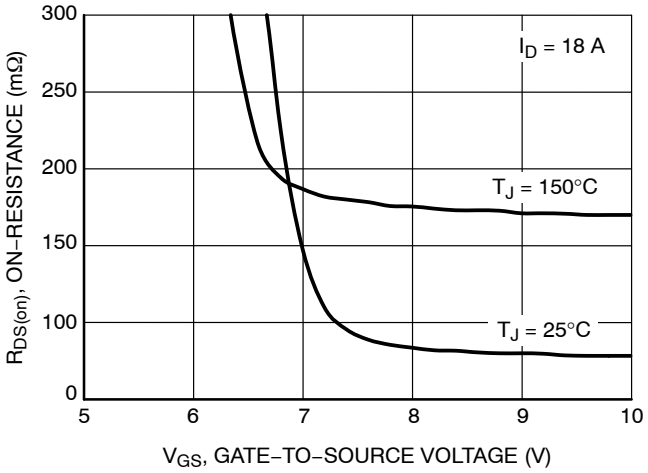


Figure 13. $R_{DS(on)}$ vs. Gate Voltage

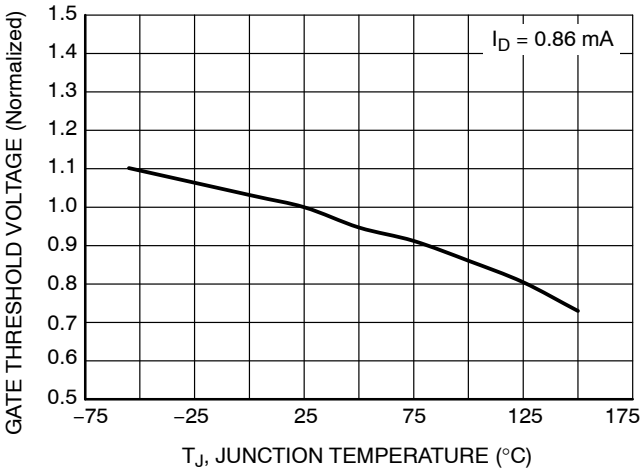
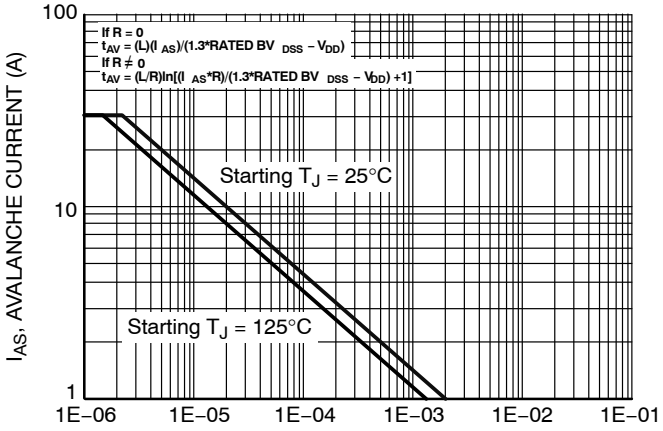


Figure 14. Normalized Gate Threshold Voltage vs. Temperature



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 15. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS

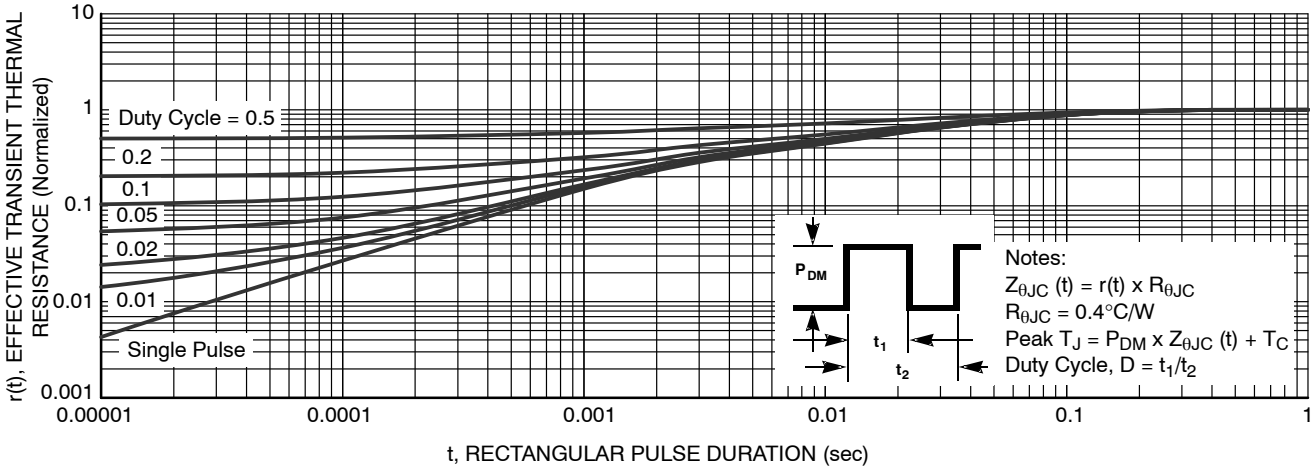


Figure 16. Transient Thermal Response

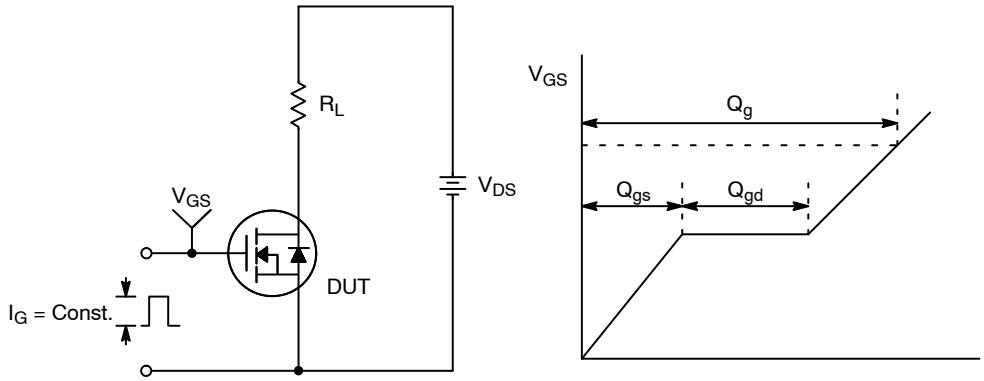


Figure 17. Gate Charge Test Circuit & Waveform

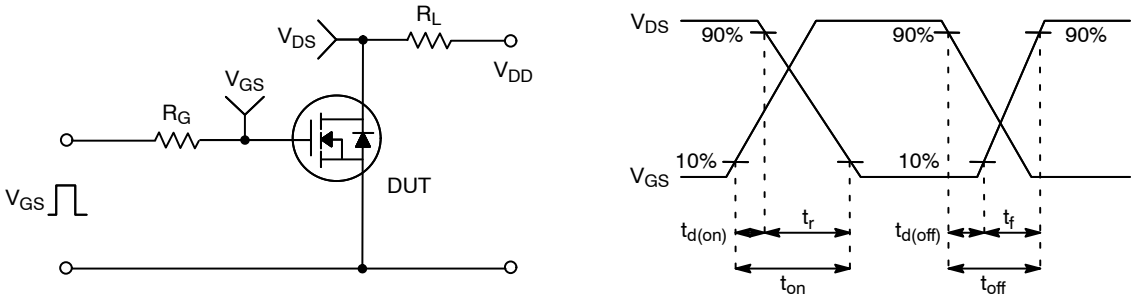


Figure 18. Resistive Switching Test Circuit & Waveforms

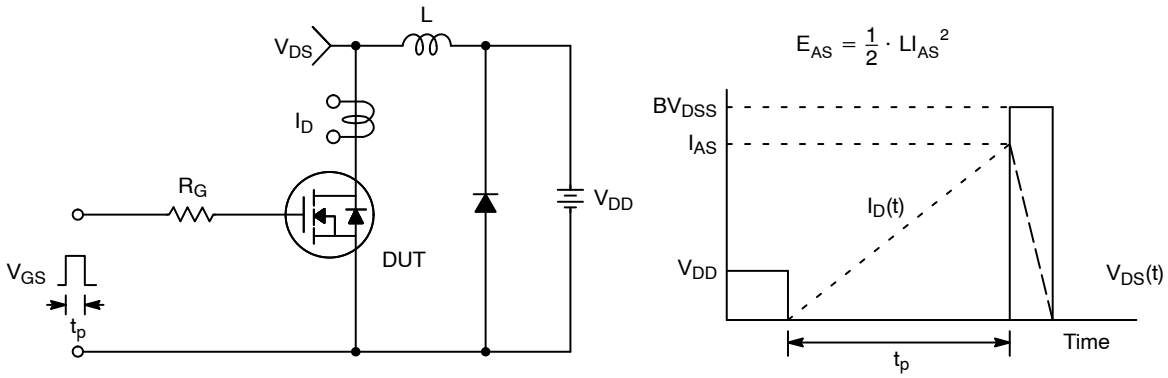


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

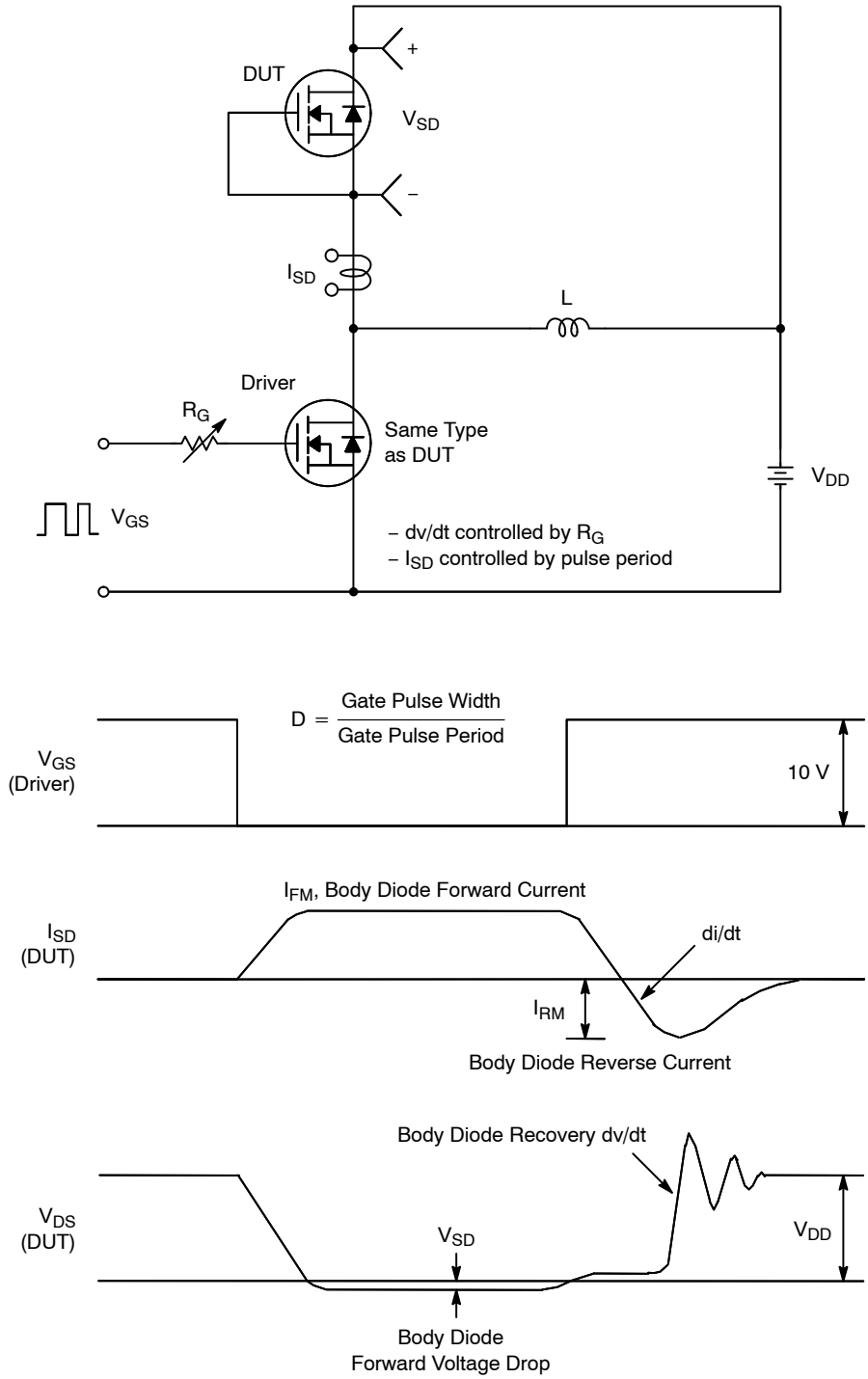
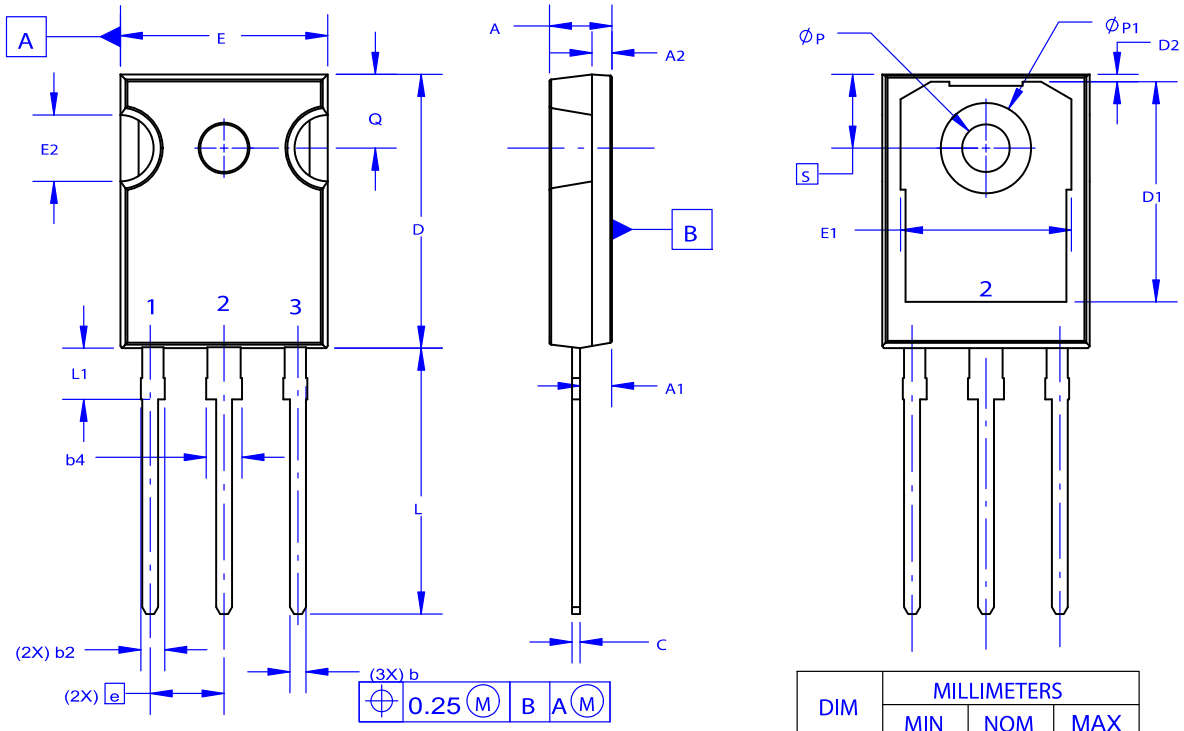


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE DIMENSIONS

TO−247−3LD
CASE 340CX
ISSUE A



NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

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