

NVLUS4C12N

MOSFET – Power, Single N-Channel, μ Cool, 2.0x2.0x0.55 mm UDFN6 30 V, 10.7 A



ON Semiconductor®

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Features

- Low Profile UDFN 2.0 x 2.0 x 0.55 mm for Board Space Saving with Exposed Drain Pads for Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Reduce Conduction Losses
- Optimized Gate Charge to Reduce Switching Losses
- Low Capacitance to Minimize Driver Losses
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- Synch DC-DC Converters
- Wireless Charging Circuit

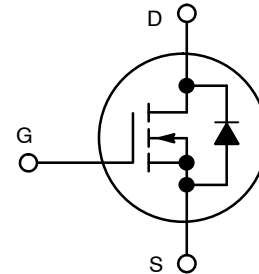
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	10.7	A
		$T_A = 85^\circ\text{C}$	7.7	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	15.1	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.54	W
		$t \leq 5$ s	$T_A = 25^\circ\text{C}$	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	6.8	A
		$T_A = 85^\circ\text{C}$	4.9	
Power Dissipation (Note 2)	$T_A = 25^\circ\text{C}$	P_D	0.63	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	43	A
MOSFET Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode) (Note 1)	I_S	1.55		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$

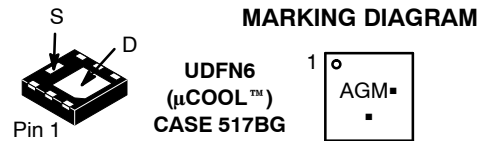
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

MOSFET		
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	9 m Ω @ 10 V	10.7 A
	12 m Ω @ 4.5 V	
	15 m Ω @ 3.7 V	
	19 m Ω @ 3.3 V	

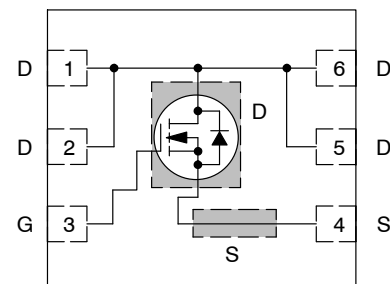


N-CHANNEL MOSFET



AG = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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2. Surface-mounted on FR4 board using the minimum recommended pad size,
2 oz. Cu.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	81	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40.5	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	200	

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size, 2 oz. Cu.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μ A	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250$ μ A, ref to 25°C		12		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$		1.0	μ A
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μ A	1.3		2.1	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			4.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 9.0$ A		7.2	9	m Ω
		$V_{GS} = 4.5$ V, $I_D = 8.0$ A		9.3	12	
		$V_{GS} = 3.7$ V, $I_D = 5.0$ A		10.9	15	
		$V_{GS} = 3.3$ V, $I_D = 5.0$ A		13	19	
Forward Transconductance	g_{FS}	$V_{DS} = 15$ V, $I_D = 9.0$ A		39		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 15$ V		1172		pF
Output Capacitance	C_{OSS}			546		
Reverse Transfer Capacitance	C_{RSS}			26		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V; $I_D = 8.0$ A		8.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	Q_{GS}			3.0		
Gate-to-Drain Charge	Q_{GD}			2.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10$ V, $V_{DS} = 15$ V; $I_D = 9.0$ A		18		nC

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DD} = 15$ V, $I_D = 8.0$ A, $R_G = 3$ Ω		9.4		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			14		
Fall Time	t_f			3.5		

SWITCHING CHARACTERISTICS, $V_{GS} = 10$ V (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10$ V, $V_{DD} = 15$ V, $I_D = 9.0$ A, $R_G = 3$ Ω		6.3		ns
Rise Time	t_r			14		
Turn-Off Delay Time	$t_{d(OFF)}$			18		
Fall Time	t_f			2.4		

- Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1.5\text{ A}$	$T_J = 25^\circ\text{C}$	0.72	1.1	V
			$T_J = 125^\circ\text{C}$	0.52		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 1.5\text{ A}$		29		ns
Charge Time	t_a			14.1		
Discharge Time	t_b			14.9		
Reverse Recovery Charge	Q_{RR}			20		

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

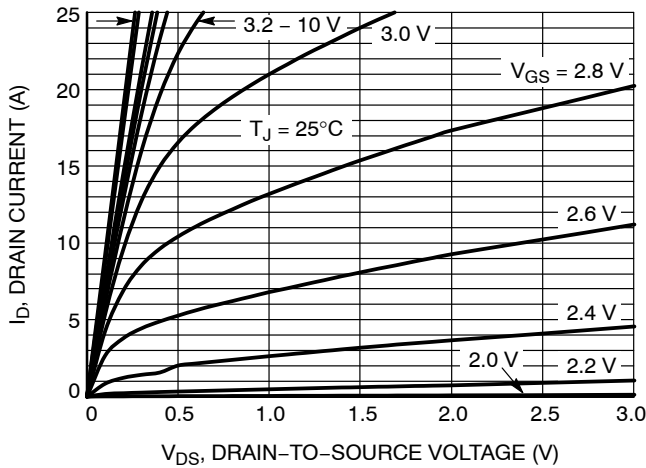


Figure 1. On-Region Characteristics

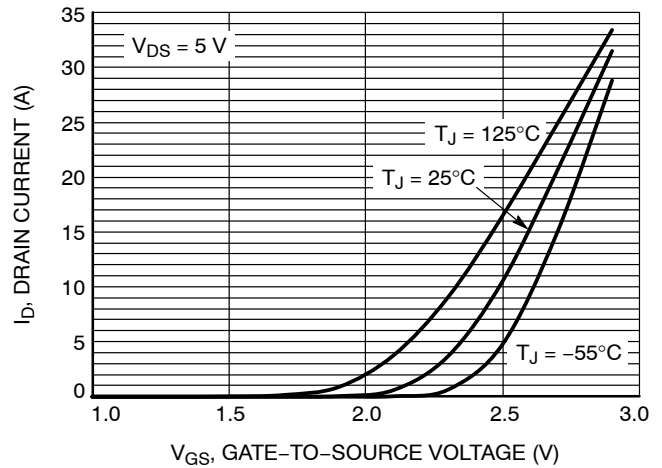


Figure 2. Transfer Characteristics

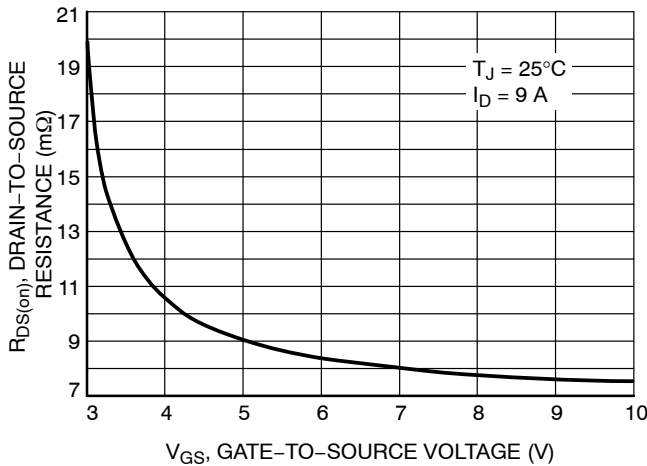


Figure 3. On-Resistance vs. Gate-to-Source Voltage

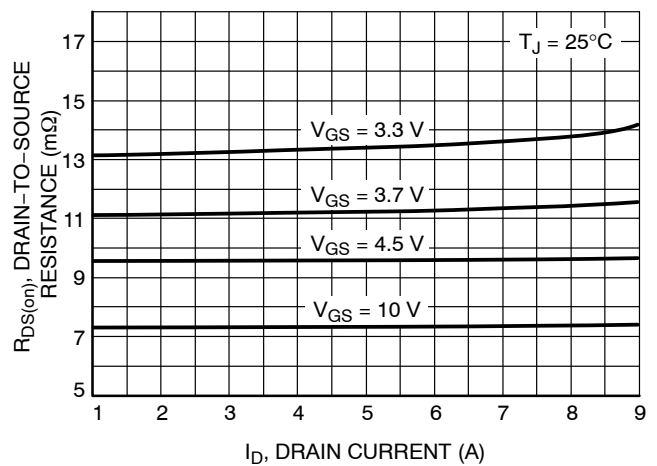


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS

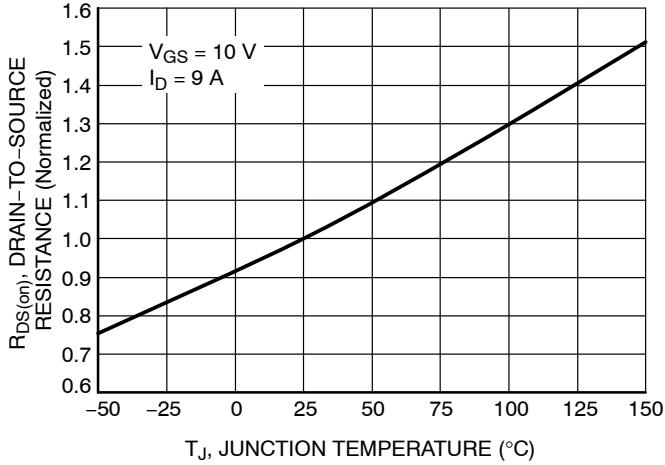


Figure 5. On-Resistance Variation with Temperature

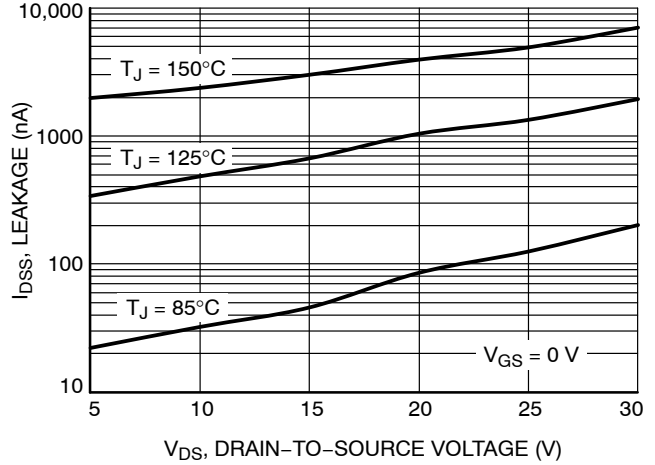


Figure 6. Drain-to-Source Leakage Current vs. Voltage

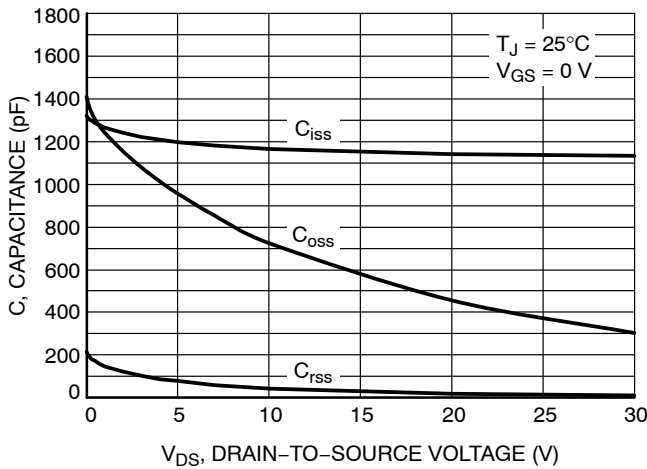


Figure 7. Capacitance Variation

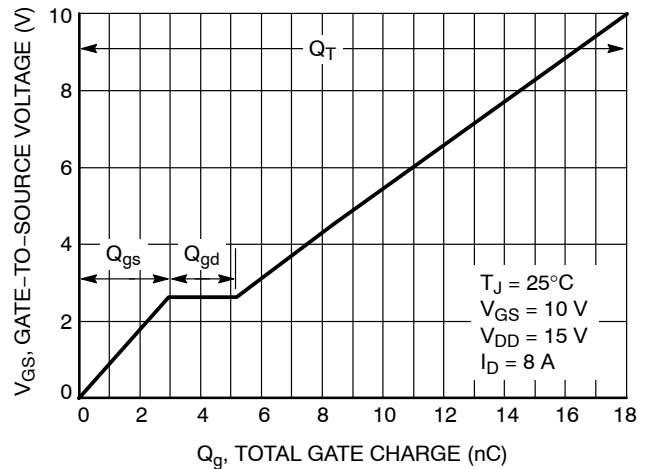


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

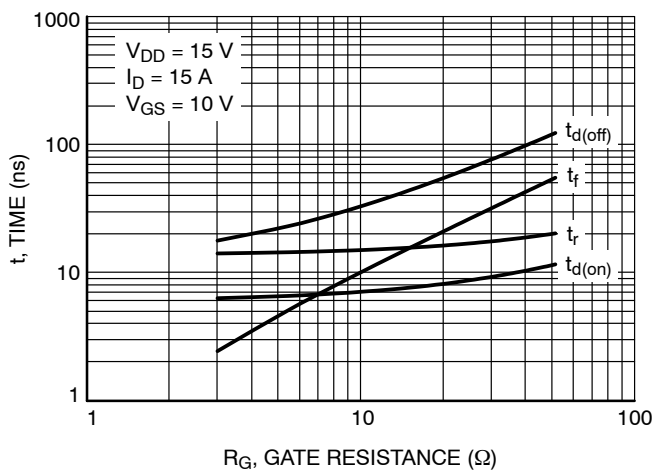


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

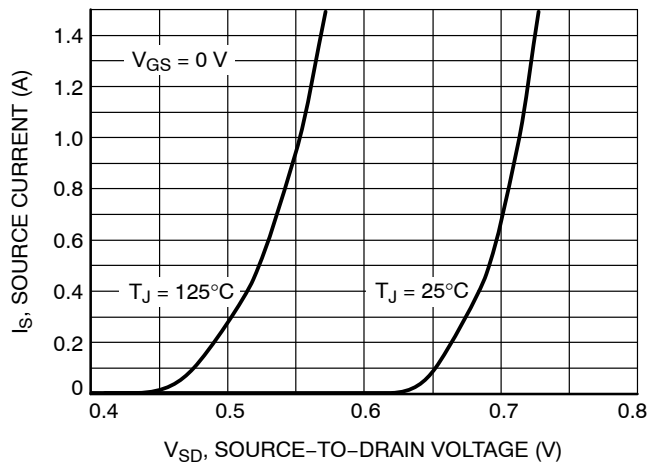


Figure 10. Diode Forward Voltage vs. Current

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TYPICAL CHARACTERISTICS

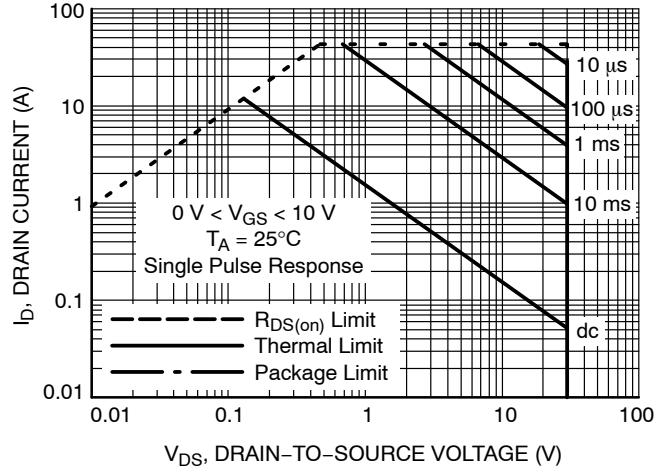


Figure 11. Maximum Rated Forward Biased Safe Operating Area

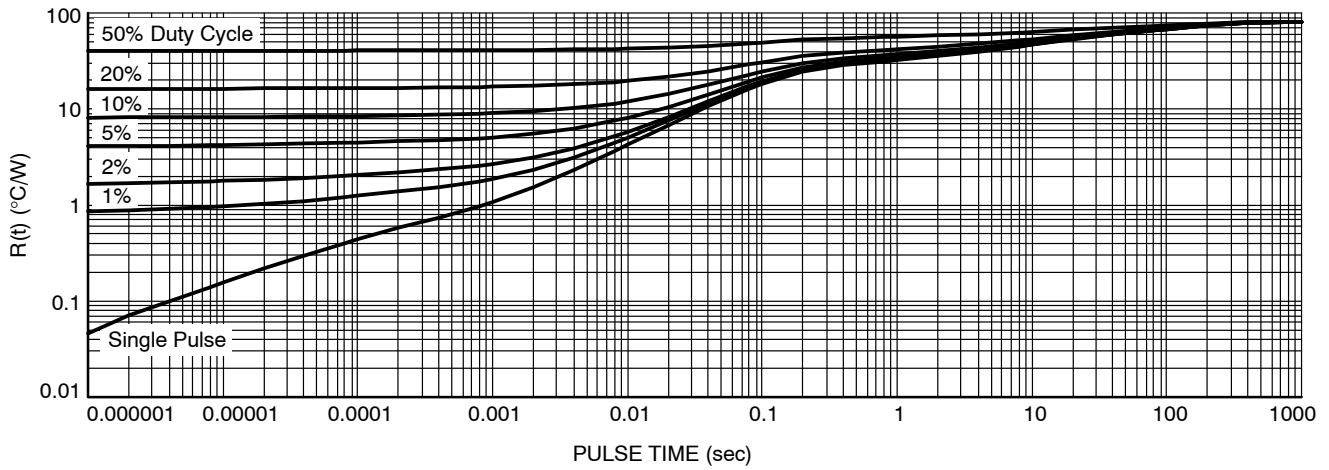


Figure 12. Thermal Response

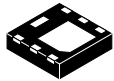
DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NVLUS4C12NTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

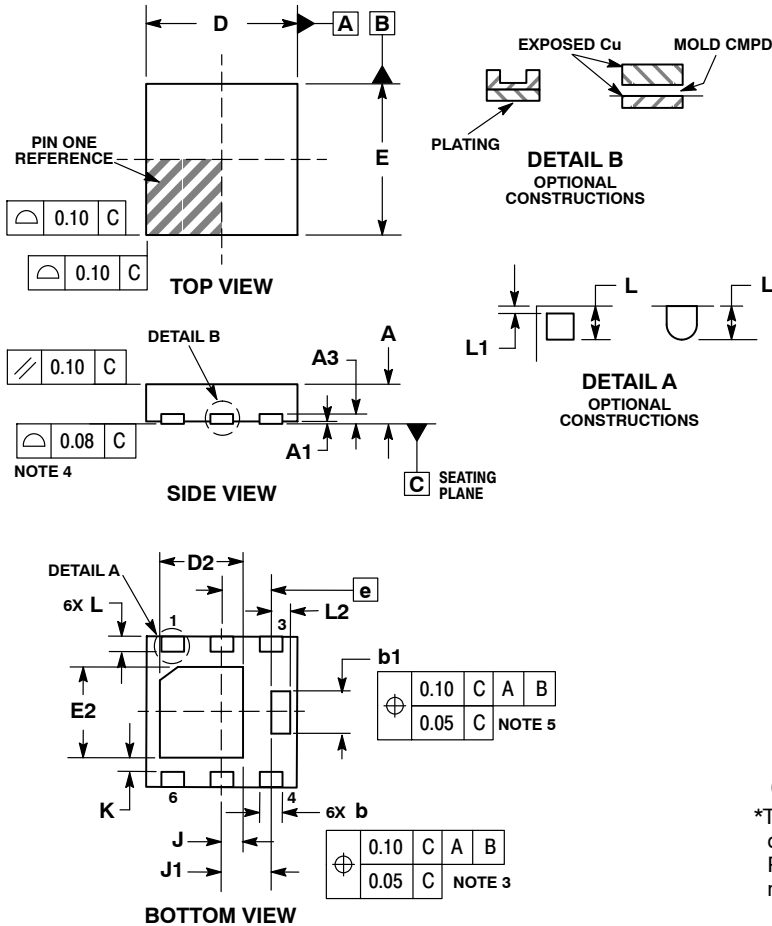
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SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517BG-01
ISSUE A

DATE 04 FEB 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. CENTER TERMINAL LEAD IS OPTIONAL. CENTER TERMINAL IS CONNECTED TO TERMINAL LEAD # 4.
2. LEADS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
J	0.27 BSC	
J1	0.65 BSC	
L	0.20	0.30
L1	---	0.10
L2	0.20	0.30

GENERIC MARKING DIAGRAM*

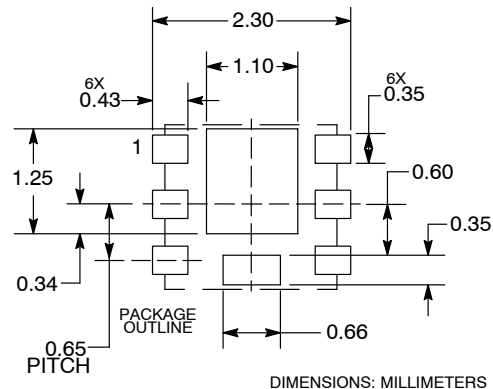


XX = Specific Device Code
M = Date Code

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



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DESCRIPTION:	UDFN6 2X2, 0.65P	PAGE 1 OF 1

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