NVMFD5853N, NVMFD5853NWF

MOSFET – Dual N-Channel, Dual SO-8FL

40 V, 10 mΩ, 53 A

ON Semiconductor®

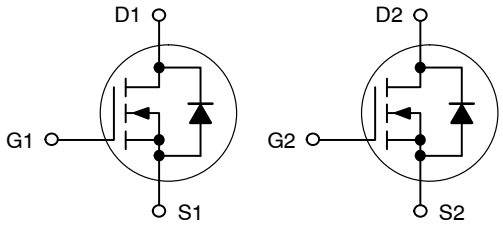
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	10 mΩ @ 10 V	53 A

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5853NWF – Wettable Flanks Product
- AEC–Q101 Qualified and PPAP Capable
- This is a Pb–Free and Halogen–Free Device

Dual N–Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	40	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	53	A
		T_C = 100°C		37	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	58	W
		T_C = 100°C		29	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	12	A
		T_A = 100°C		8.7	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	165	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	53	A
Single Pulse Drain–to–Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 28.3 A, L = 0.1 mH)			E_{AS}	40	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

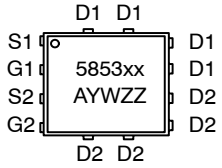
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State (Note 2)	$R_{\theta JC}$	2.6	°C/W
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



5853N = NVMFD5853N
5853WF = NVMFD5853NWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5853NT1G	DFN8 (Pb–Free)	1500 / Tape & Reel
NVMFD5853NWFT1G	DFN8 (Pb–Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				41.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A			8.4	10	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 15 A			44		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1225		pF
Output Capacitance	C_{oss}				150		
Reverse Transfer Capacitance	C_{rss}				100		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 15 A			24		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.5		
Gate−to−Source Charge	Q_{GS}				5.2		
Gate−to−Drain Charge	Q_{GD}				6.6		
Plateau Voltage	V_{GP}				4.1		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 15 A, R_G = 2.5 Ω			9		ns
Rise Time	t_r				20		
Turn−Off Delay Time	$t_{d(off)}$				21		
Fall Time	t_f				3		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A	T_J = 25°C		0.82	1.1	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 15 A			16		ns
Charge Time	t_a				10		
Discharge Time	t_b				6		
Reverse Recovery Charge	Q_{RR}				9		nC

4. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

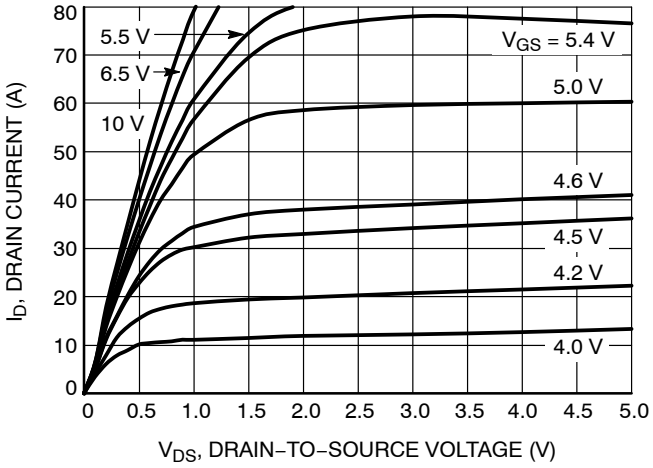


Figure 1. On−Region Characteristics

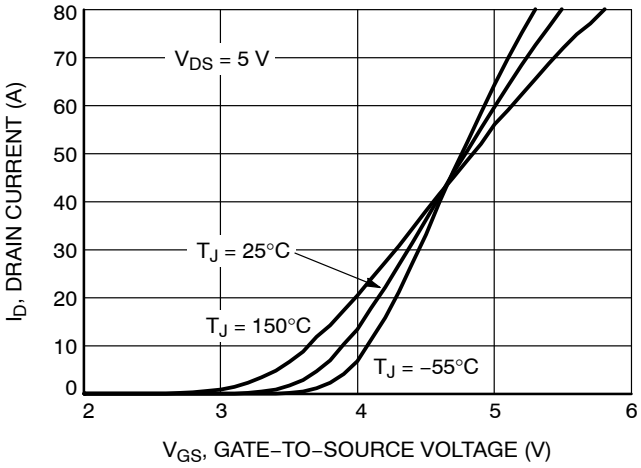


Figure 2. Transfer Characteristics

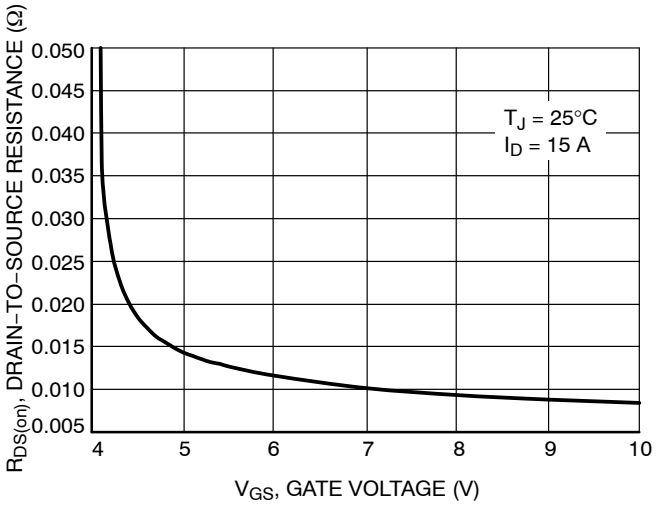


Figure 3. On−Resistance vs. Gate−to−Source Voltage

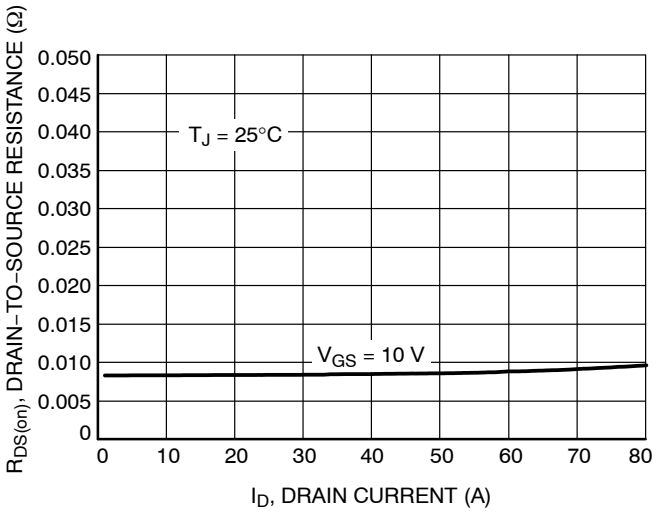


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

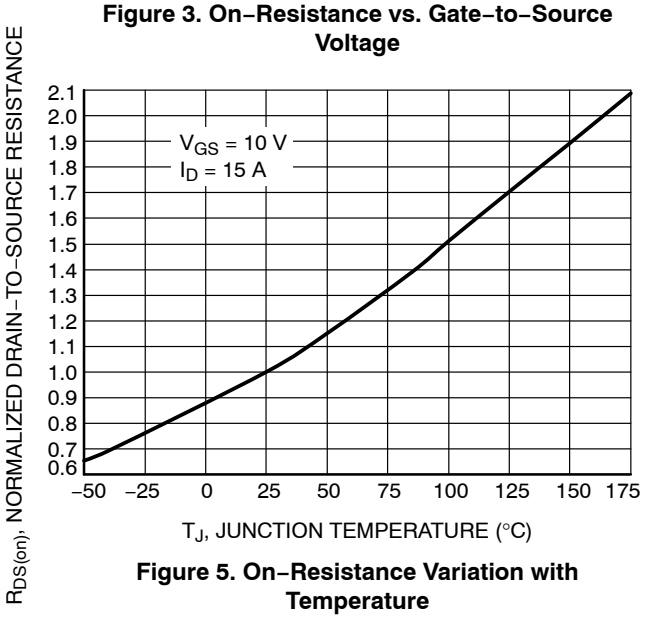


Figure 5. On−Resistance Variation with Temperature

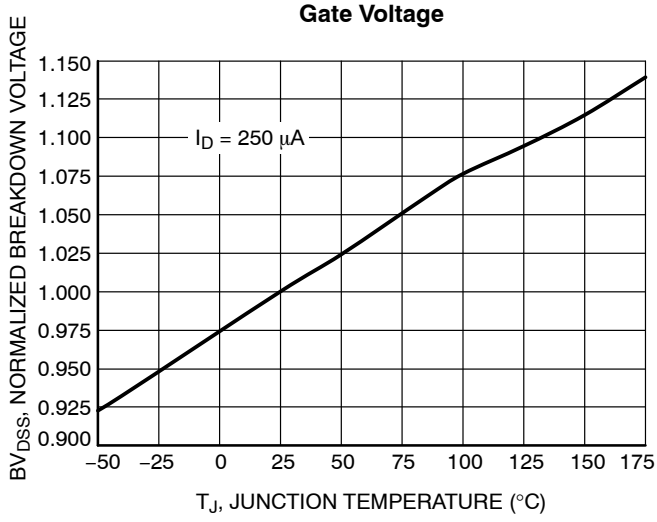


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

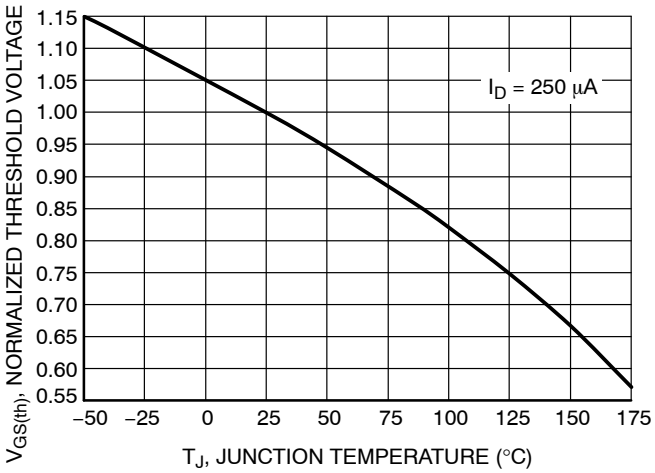


Figure 7. Threshold Voltage Variation with Temperature

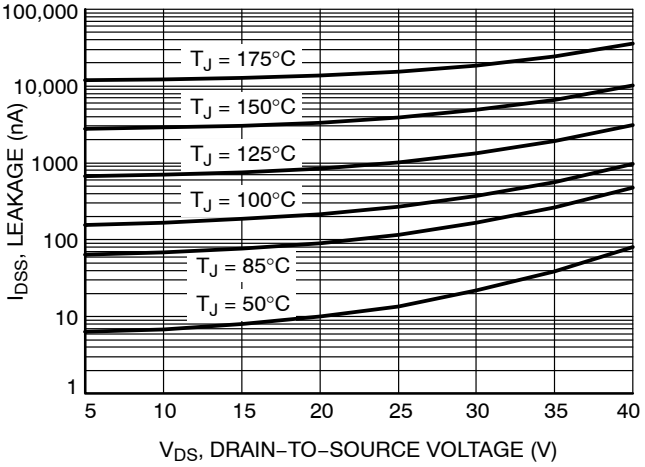


Figure 8. Drain−to−Source Leakage Current vs. Voltage

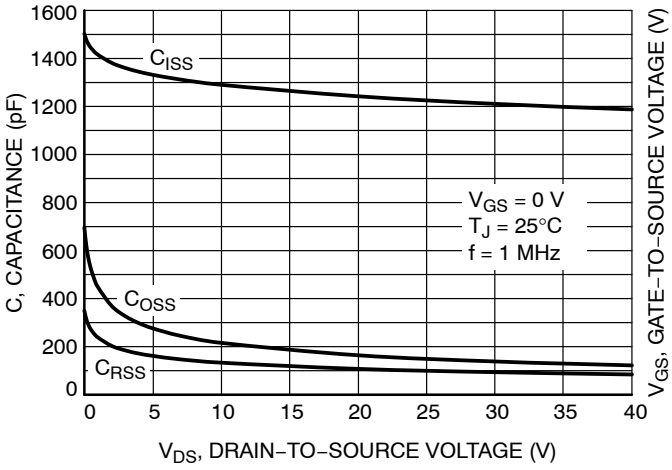


Figure 9. Capacitance Variation

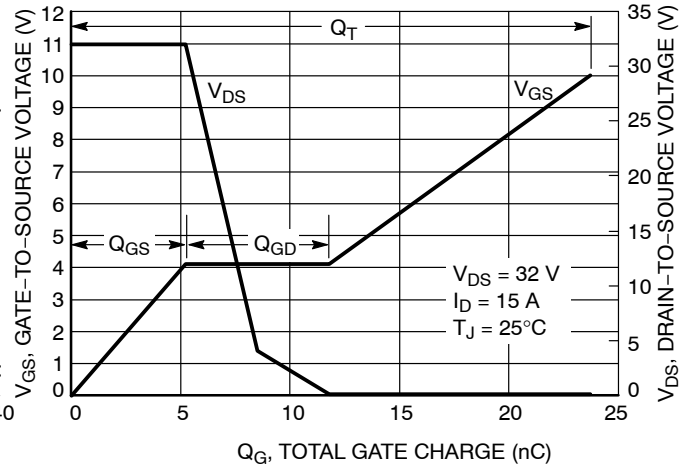


Figure 10. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

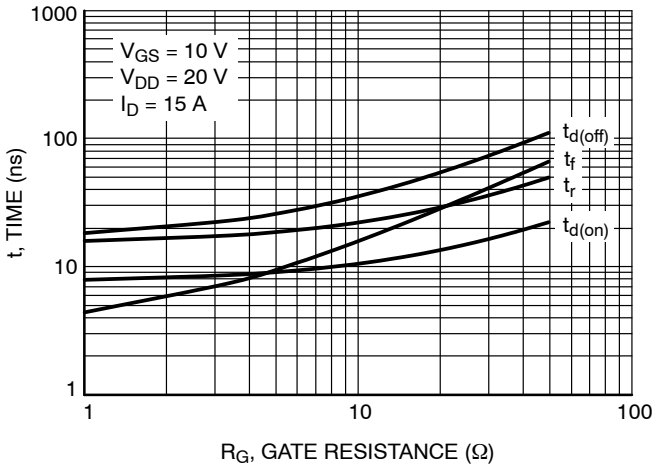


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

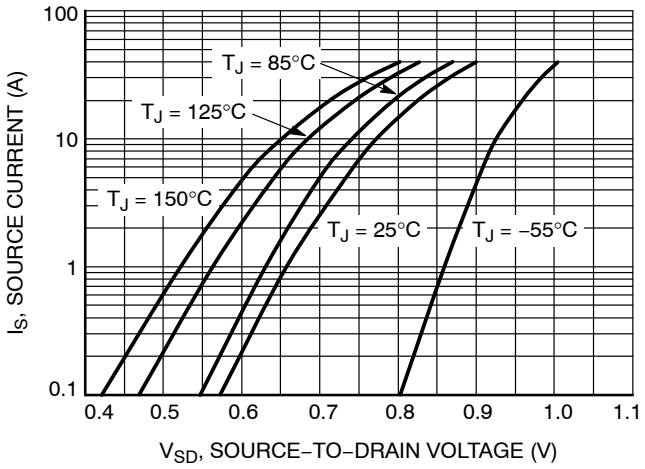


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

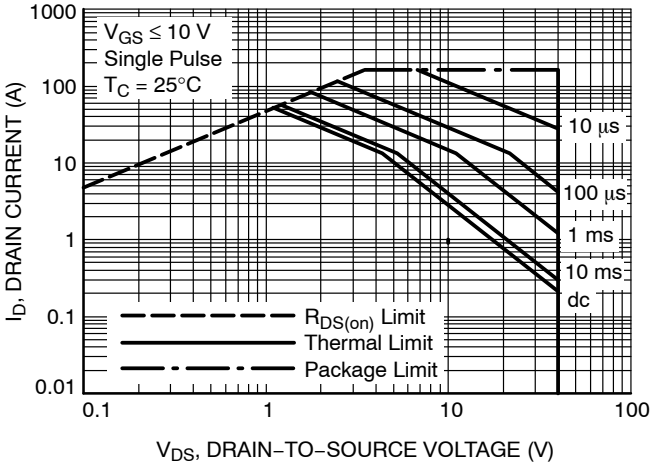


Figure 13. Maximum Rated Forward Biased Safe Operating Area

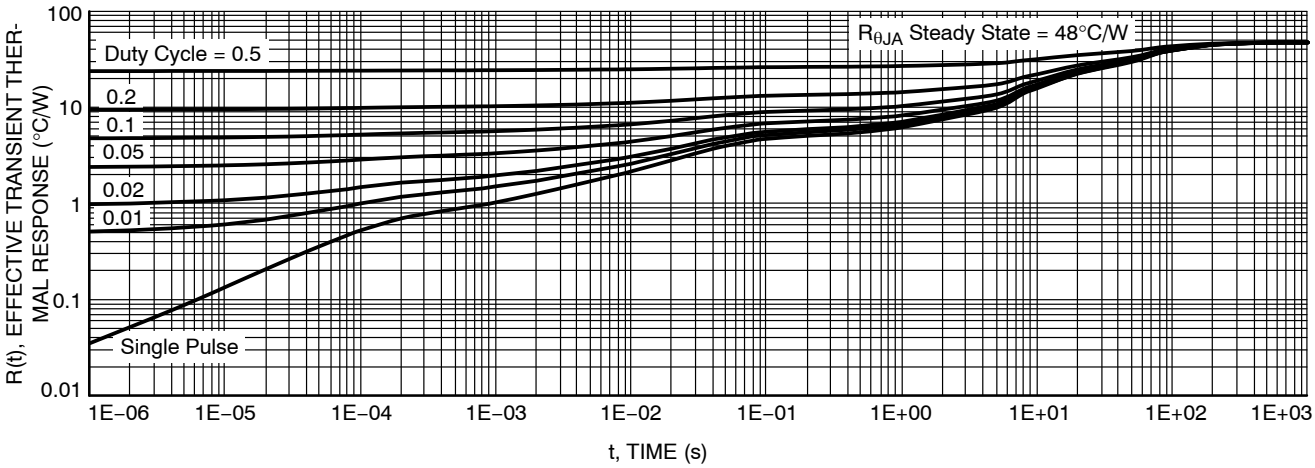


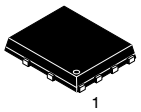
Figure 14. Thermal Impedance (Junction−to−Ambient)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

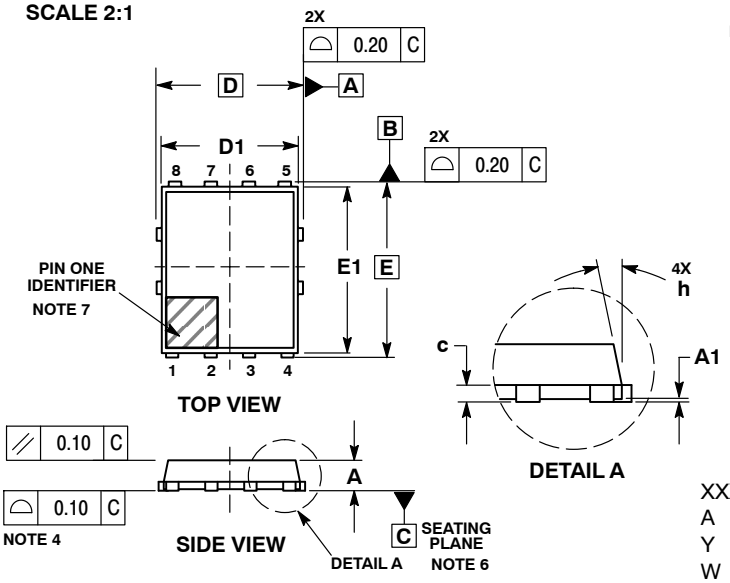
ON Semiconductor®

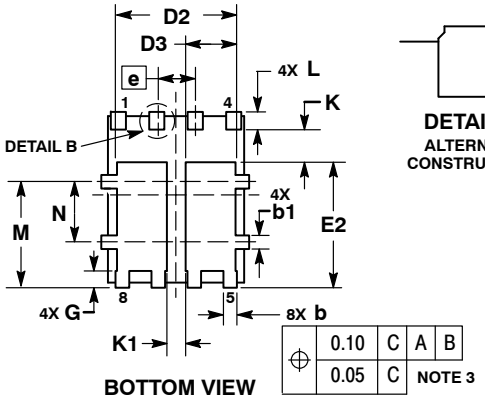
DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual)
CASE 506BT
ISSUE E

DATE 26 FEB 2013



SCALE 2:1



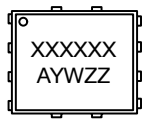


DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

DIM	MILLIMETERS		
	MIN	MAX	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

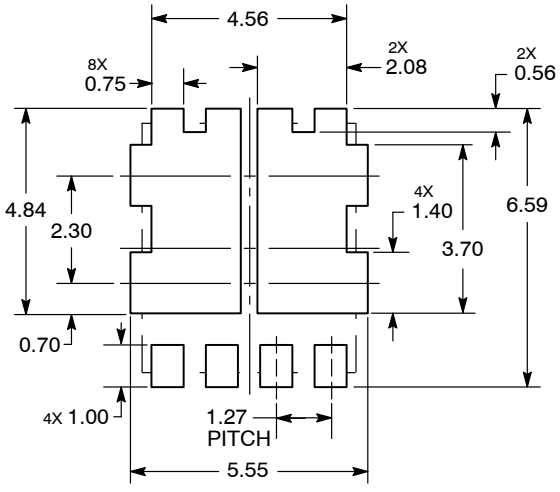
GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL)	PAGE 1 OF 1

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