

# NVMFS5C604NL

## MOSFET – Power, Single N-Channel 60 V, 1.2 mΩ, 287 A



ON Semiconductor®

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### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5C604NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---------------|------------------|-----------|
| 60 V          | 1.2 mΩ @ 10 V    | 287 A     |
|               | 1.7 mΩ @ 4.5 V   |           |

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

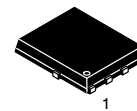
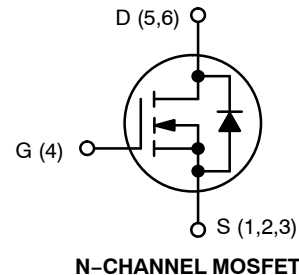
| Parameter  | Symbol   | Value                     | Unit             |                  |   |
|--|--|---------------------------|------------------|------------------|---|
| Drain-to-Source Voltage  | $V_{DSS}$                                      | 60                        | V                |                  |   |
| Gate-to-Source Voltage   | $V_{GS}$                                       | $\pm 20$                  | V                |                  |   |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)                        | Steady State                                   | $T_C = 25^\circ\text{C}$  | $I_D$            | 287              | A |
|  |  | $T_C = 100^\circ\text{C}$ |                  | 203              |   |
| Power Dissipation $R_{\theta JC}$ (Note 1)                                   | Steady State                                   | $T_C = 25^\circ\text{C}$  | $P_D$            | 200              | W |
|  |  | $T_C = 100^\circ\text{C}$ |                  | 100              |   |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)                     | Steady State                                   | $T_A = 25^\circ\text{C}$  | $I_D$            | 40               | A |
|  |  | $T_A = 100^\circ\text{C}$ |                  | 28               |   |
| Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)                              | Steady State                                   | $T_A = 25^\circ\text{C}$  | $P_D$            | 3.9              | W |
|  |  | $T_A = 100^\circ\text{C}$ |                  | 1.9              |   |
| Pulsed Drain Current   | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | $I_{DM}$                  | 900              | A                |   |
| Operating Junction and Storage Temperature                                   | $T_J, T_{stg}$                                 | -55 to +175               |                  | $^\circ\text{C}$ |   |
| Source Current (Body Diode)  | $I_S$  | 203                       | A                |                  |   |
| Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 22 \text{ A}$ ) | $E_{AS}$                                       | 776                       | mJ               |                  |   |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s)            | $T_L$  | 260                       | $^\circ\text{C}$ |                  |   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

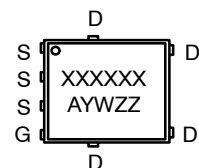
| Parameter                                   | Symbol          | Value | Unit                      |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State             | $R_{\theta JC}$ | 0.75  | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 39    |                           |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



XXXXXX = 5C604L  
(NVMFS5C604NL) or  
604LWF  
(NVMFS5C604NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFS5C604NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|   |                   |   |                           |      |           |               |
|---|-------------------|---|---------------------------|------|-----------|---------------|
| Drain-to-Source Breakdown Voltage                         | $V_{(BR)DSS}$     | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$   | 60                        |      |           | V             |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ |   |                           | 22.9 |           | mV/°C         |
| Zero Gate Voltage Drain Current                           | $I_{DSS}$         | $V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$     | $T_J = 25^\circ\text{C}$  |      | 10        | $\mu\text{A}$ |
|   |                   |   | $T_J = 125^\circ\text{C}$ |      | 250       |               |
| Gate-to-Source Leakage Current                            | $I_{GSS}$         | $V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$ |                           |      | $\pm 100$ | nA            |

### ON CHARACTERISTICS (Note 4)

|                                   |                  |  |     |      |     |            |
|-----------------------------------|------------------|--|-----|------|-----|------------|
| Gate Threshold Voltage            | $V_{GS(TH)}$     | $V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$  | 1.2 |      | 2.0 | V          |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ |  |     | -5.9 |     | mV/°C      |
| Drain-to-Source On Resistance     | $R_{DS(on)}$     | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$  |     | 0.93 | 1.2 | m $\Omega$ |
|                                   |                  | $V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$ |     | 1.25 | 1.7 |            |
| Forward Transconductance          | $g_{FS}$         | $V_{DS} = 15\text{ V}, I_D = 50\text{ A}$  |     | 180  |     | S          |

### CHARGES, CAPACITANCES & GATE RESISTANCE

|                              |              |  |  |      |  |    |
|------------------------------|--------------|--|--|------|--|----|
| Input Capacitance            | $C_{ISS}$    | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$    |  | 8900 |  | pF |
| Output Capacitance           | $C_{OSS}$    |  |  | 3750 |  |    |
| Reverse Transfer Capacitance | $C_{RSS}$    |  |  | 40   |  |    |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ |  | 52   |  | nC |
| Total Gate Charge            | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$  |  | 120  |  |    |
| Threshold Gate Charge        | $Q_{G(TH)}$  | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ |  | 6.4  |  |    |
| Gate-to-Source Charge        | $Q_{GS}$     |  |  | 21.4 |  |    |
| Gate-to-Drain Charge         | $Q_{GD}$     |  |  | 12.7 |  |    |
| Plateau Voltage              | $V_{GP}$     |  |  | 2.8  |  | V  |

### SWITCHING CHARACTERISTICS (Note 5)

|                     |              |   |  |      |  |    |
|---------------------|--------------|---|--|------|--|----|
| Turn-On Delay Time  | $t_{d(ON)}$  | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\ \Omega$ |  | 21.8 |  | ns |
| Rise Time           | $t_r$        |   |  | 79.1 |  |    |
| Turn-Off Delay Time | $t_{d(OFF)}$ |   |  | 57.8 |  |    |
| Fall Time           | $t_f$        |   |  | 81.3 |  |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |          |  |                           |     |      |     |    |
|-------------------------|----------|--|---------------------------|-----|------|-----|----|
| Forward Diode Voltage   | $V_{SD}$ | $V_{GS} = 0\text{ V}, I_S = 50\text{ A}$                                     | $T_J = 25^\circ\text{C}$  |     | 0.78 | 1.2 | V  |
|                         |          |  | $T_J = 125^\circ\text{C}$ |     | 0.64 |     |    |
| Reverse Recovery Time   | $t_{RR}$ | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$ |                           | 98  |      | ns  |    |
| Charge Time             | $t_a$    |  |                           | 45  |      |     |    |
| Discharge Time          | $t_b$    |  |                           | 53  |      |     |    |
| Reverse Recovery Charge | $Q_{RR}$ |  |                           | 190 |      |     | nC |

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NVMFS5C604NL

## TYPICAL CHARACTERISTICS

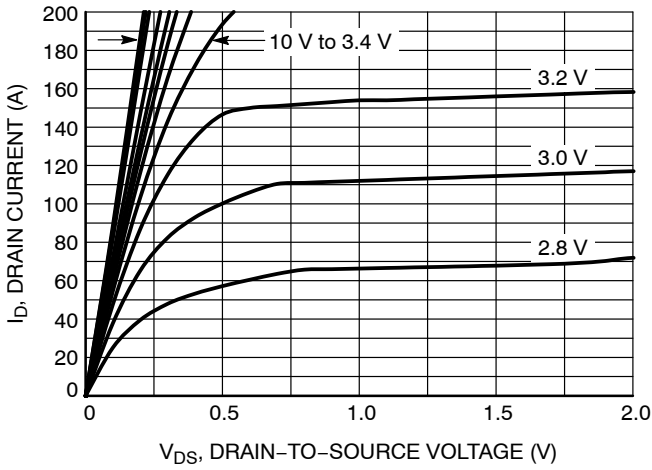


Figure 1. On-Region Characteristics

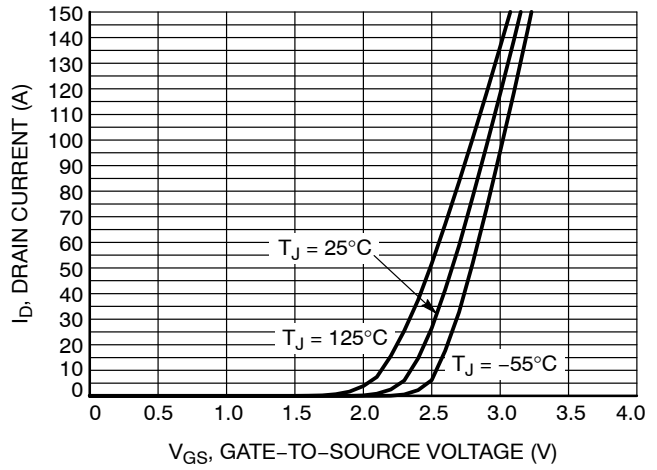


Figure 2. Transfer Characteristics

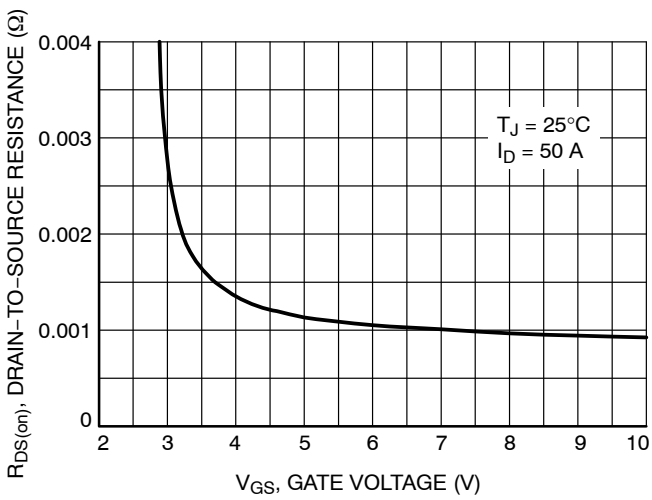


Figure 3. On-Resistance vs. Gate-to-Source Voltage

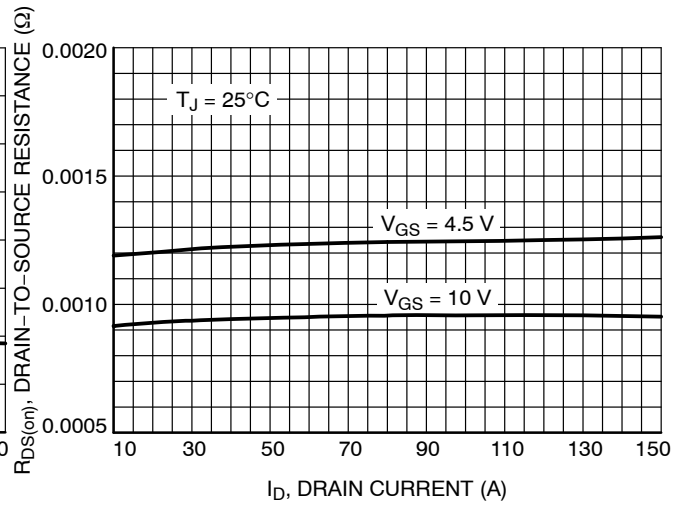


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

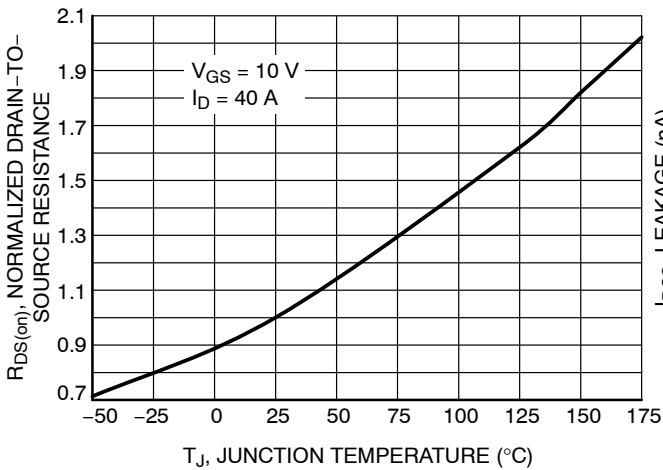


Figure 5. On-Resistance Variation with Temperature

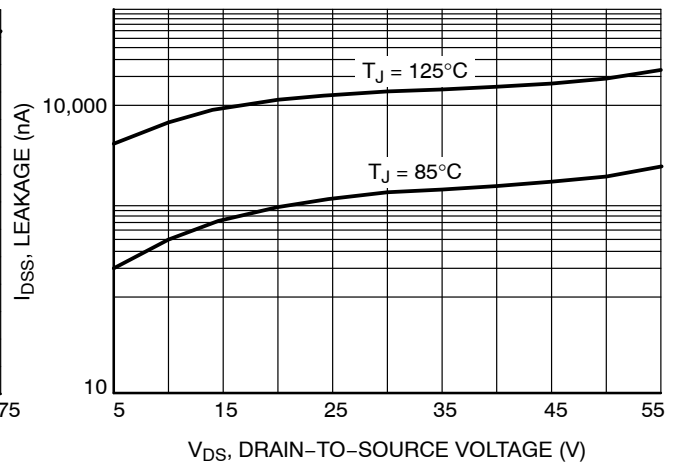


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

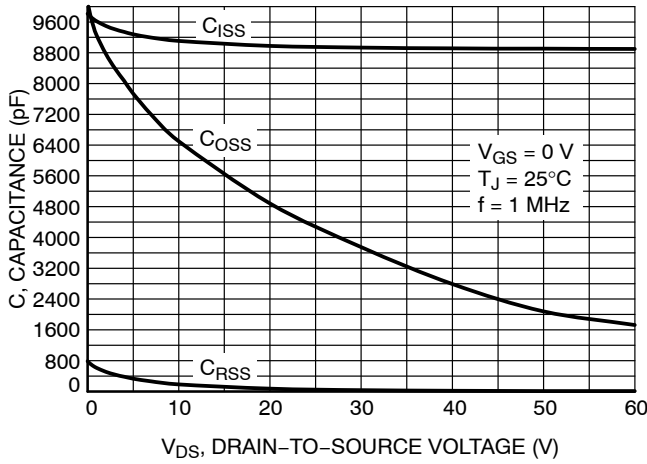


Figure 7. Capacitance Variation

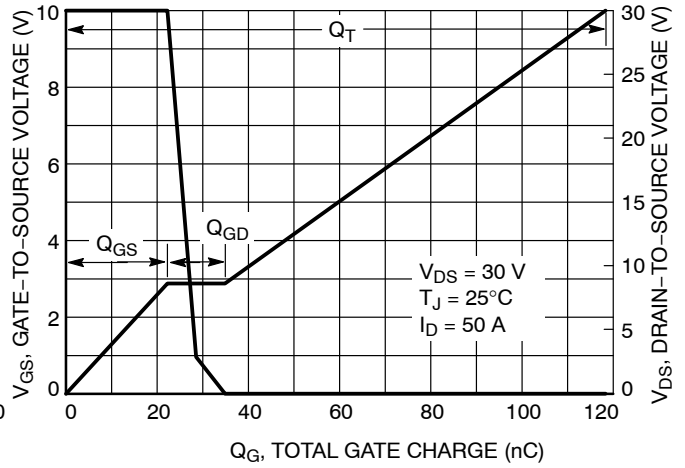


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

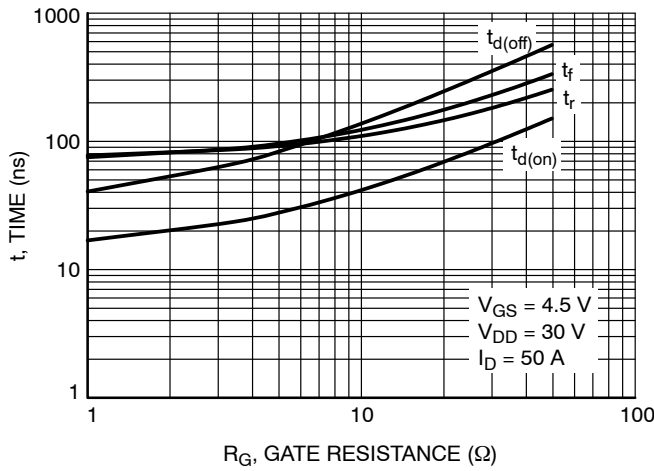


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

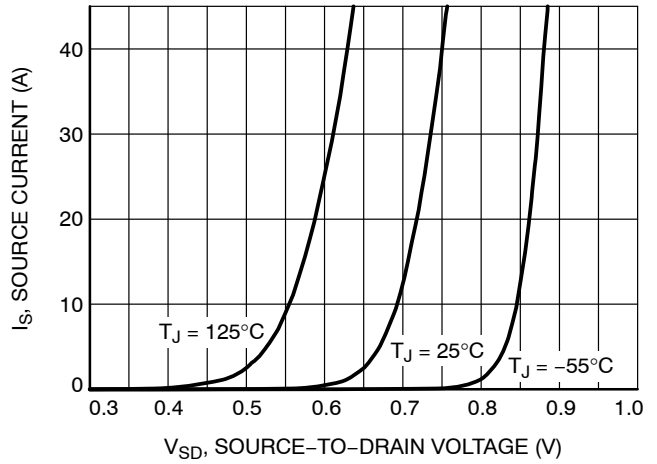


Figure 10. Diode Forward Voltage vs. Current

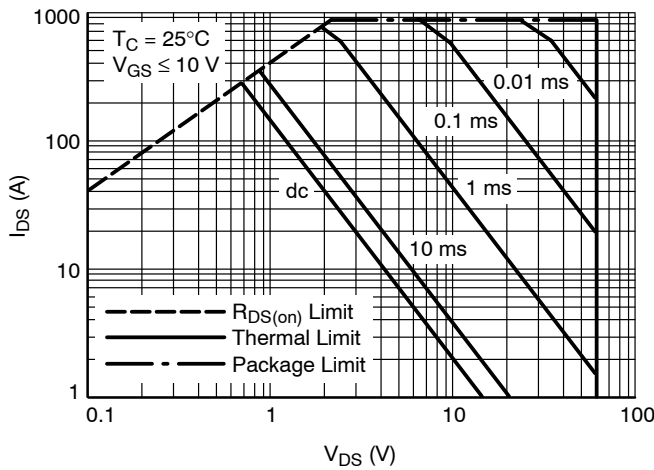


Figure 11. Safe Operating Area

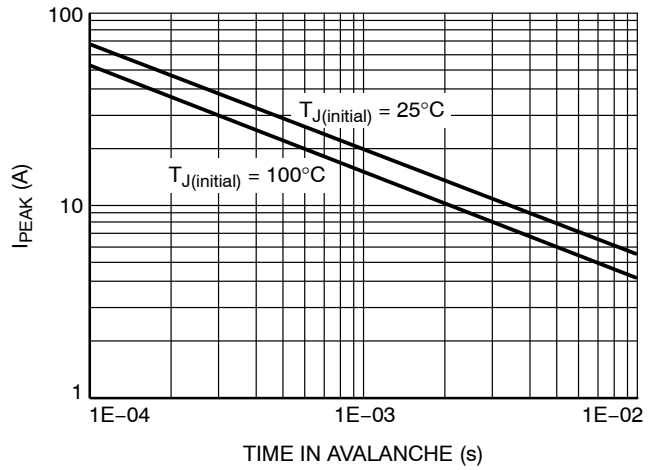
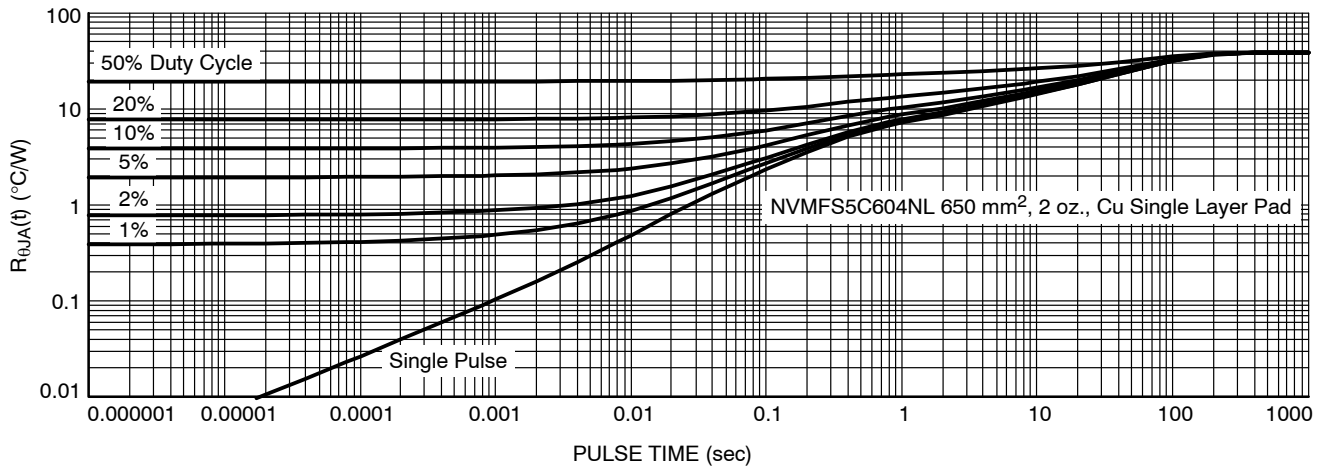


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFS5C604NL



**Figure 13. Thermal Characteristics**

## DEVICE ORDERING INFORMATION

| Device              | Marking | Package                            | Shipping <sup>†</sup> |
|---------------------|---------|------------------------------------|-----------------------|
| NVMFS5C604NLT1G     | 5C604L  | DFN5<br>(Pb-Free)                  | 1500 / Tape & Reel    |
| NVMFS5C604NLWFT1G   | 604LWF  | DFN5<br>(Pb-Free, Wettable Flanks) | 1500 / Tape & Reel    |
| NVMFS5C604NLT3G     | 5C604L  | DFN5<br>(Pb-Free)                  | 5000 / Tape & Reel    |
| NVMFS5C604NLWFT3G   | 604LWF  | DFN5<br>(Pb-Free, Wettable Flanks) | 5000 / Tape & Reel    |
| NVMFS5C604NLAFT1G   | 5C604L  | DFN5<br>(Pb-Free)                  | 1500 / Tape & Reel    |
| NVMFS5C604NLWFAFT1G | 604LWF  | DFN5<br>(Pb-Free, Wettable Flanks) | 1500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

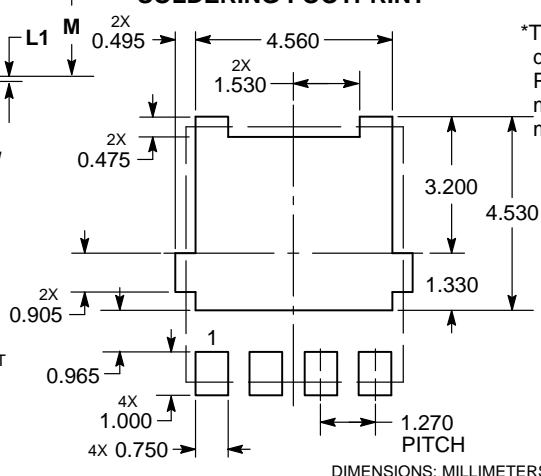
### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT\*



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                          |  |
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| DESCRIPTION:     | DFN5 5x6, 1.27P (SO-8FL) | PAGE 1 OF 1  |

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