## **Power MOSFET**

# 80 V, 5.5 m $\Omega$ , 89 A, Single N-Channel

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- NVMFSW6D1N08H Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

### **Typical Applications**

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

## **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	80	V
Gate-to-Source Voltage	Э		$V_{GS}$	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 1)	Steady	T <sub>C</sub> = 25°C	I <sub>D</sub>	89	А
Power Dissipation $R_{\theta JC}$ (Note 1)	State		P <sub>D</sub>	104	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	17	Α
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	State		P <sub>D</sub>	3.8	W
Pulsed Drain Current	$T_A = 25^{\circ}C$ , $t_p = 10 \mu s$		I <sub>DM</sub>	468	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	87	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>AV</sub> = 5.9 A)			E <sub>AS</sub>	465	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			TL	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{ heta JC}$	1.44	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	40	

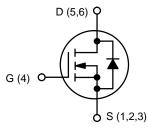
The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



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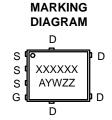
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	5.5 mΩ @ 10 V	89 A



**N-CHANNEL MOSFET** 



DFN5 (SO-8FL) CASE 488AA STYLE 1



XXXXXX = 6D1N08

(NVMFS6D1N08H) or

W6D1N8

(NVMFSW6D1N08H)

A = Assembly Location Y = Year

W = Work Week

ZZ = Lot Traceability

#### **ORDERING INFORMATION**

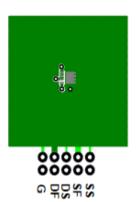
See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

<sup>2.</sup> Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 1 oz. Cu pad.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> / T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C			43.8		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	T <sub>J</sub> = 25°C			10	μΑ
		$V_{DS} = 80 \text{ V}$	T <sub>J</sub> = 125°C			100	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS}$	= 20 V			100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	= 120 μA	2.0		4.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref	to 25°C		-7.08		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub>	= 20 A		4.5	5.5	mΩ
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub>	= 20 A		80		S
Gate-Resistance	$R_{G}$	T <sub>A</sub> = 25°	С		1.0		Ω
CHARGES & CAPACITANCES							•
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz, V}_{DS} = 40 \text{ V}$			2085		pF
Output Capacitance	C <sub>OSS</sub>				300		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				10		1
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 6 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 30 A			10		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 30 A			32		nC
Gate-to-Source Charge	Q <sub>GS</sub>				10		1
Gate-to-Drain Charge	$Q_{GD}$				6		1
Plateau Voltage	$V_{GP}$				5		V
SWITCHING CHARACTERISTICS (Note 3	)						•
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 64 \text{ V},$			18		ns
Rise Time	t <sub>r</sub>	$I_D = 30 \text{ A}, R_G =$	= 2.5 Ω		50		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>				48		1
Fall Time	t <sub>f</sub>				39		1
DRAIN-SOURCE DIODE CHARACTERIS	TICS						•
Forward Diode Voltage	V <sub>SD</sub>	$V_{GS} = 0 \text{ V},$ $I_{S} = 20 \text{ A}$	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.7		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dI_{S}/dt =$			49		ns
Reverse Recovery Charge	Q <sub>RR</sub>	I <sub>S</sub> = 20 A			60		nC
Charge Time	ta	$V_{GS} = 0 \text{ V, dI}_{S}/dt = 100 \text{ A}/\mu\text{s,}$ $I_{S} = 20 \text{ A}$			30		ns
Discharge Time	t <sub>b</sub>				19		ns

<sup>Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Switching characteristics are independent of operating junction temperatures
4. R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR–4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.</sup> 



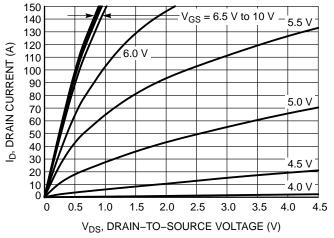
a) 53°C/W when mounted on a 1 in² pad of 2 oz copper.

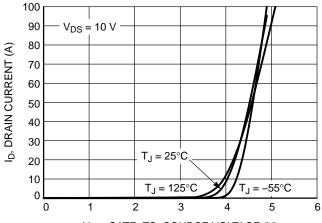


b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- 5. Pulse Test: pulse width < 300  $\mu$ s, duty cycle < 2%.
  6. E<sub>AS</sub> of 465 mJ is based on started T<sub>J</sub> = 25°C, I<sub>AS</sub> = 5.9 A, V<sub>DD</sub> = 80 V, V<sub>GS</sub> = 10 V. 100% test at I<sub>AS</sub> = 8.4 A.
  7. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

#### **TYPICAL CHARACTERISTICS**





V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

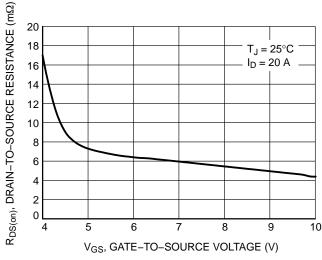


Figure 2. Transfer Characteristics

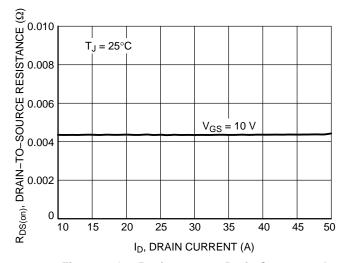


Figure 3. On-Resistance vs. Gate-to-Source Voltage

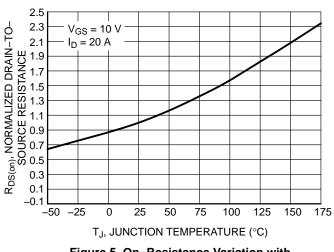


Figure 5. On-Resistance Variation with **Temperature** 

Figure 4. On-Resistance vs. Drain Current and **Gate Voltage** 

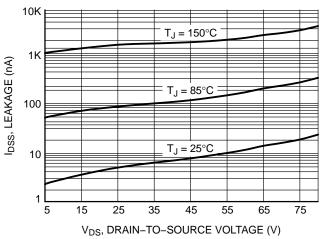


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**

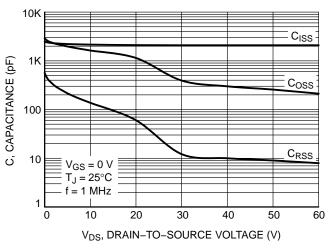


Figure 7. Capacitance Variation

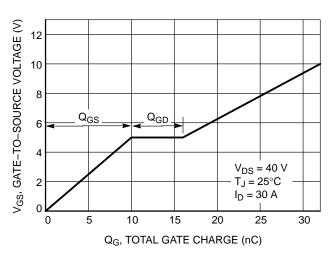


Figure 8. Gate-to-Source Voltage vs. Total Charge

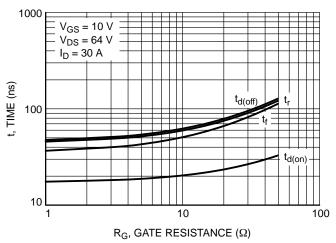


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

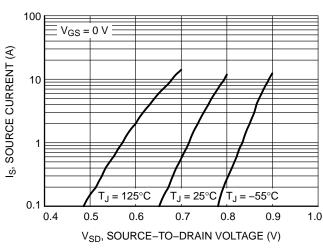


Figure 10. Diode Forward Voltage vs. Current

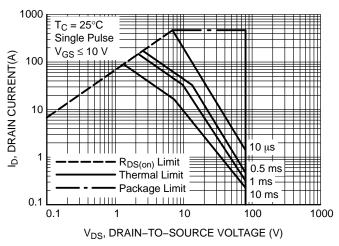


Figure 11. Maximum Rated Forward Biased Safe Operating Area

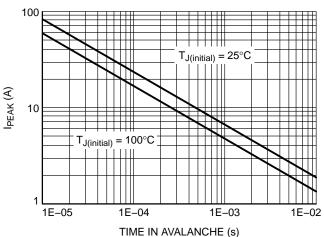


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

## **TYPICAL CHARACTERISTICS**

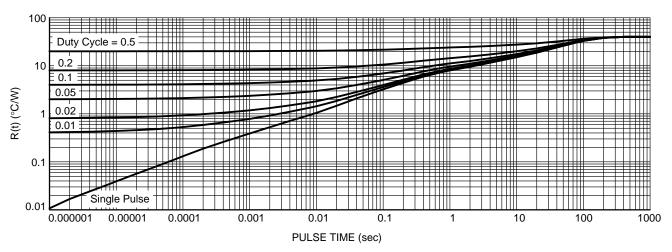


Figure 13. Thermal Characteristics

### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS6D1N08HT1G	6D1N08	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFSW6D1N08HT1G	W6D1N8	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SIDE VIEW



DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

**DATE 25 JUN 2018** 

#### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
  CONTROLLING DIMENSION: MILLIMETER.
  DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
M	3.00	3.40	3.80	
A	n o		12 °	

#### **GENERIC** MARKING DIAGRAM\*



XXXXXX = Specific Device Code

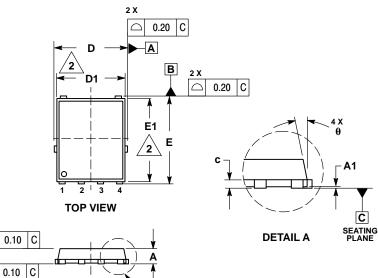
= Assembly Location Α

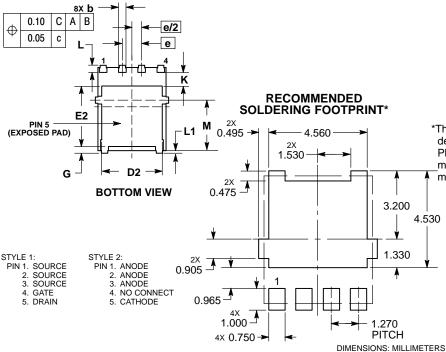
= Lot Traceability

Υ = Year W = Work Week

ZZ

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





**DETAIL A** 

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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