MOSFET - Power, Single

N-Channel

80 V, 4 mΩ, 110 A

NVMFS6H824NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS6H824NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	80	V
Gate-to-Source Voltage	Э		V _{GS}	±20	V
Continuous Drain		T _C = 25°C	I _D	110	Α
Current R _{θJC} (Notes 1, 3)	Steady	T _C = 100°C		78	
Power Dissipation	State	T _C = 25°C	P _D	116	W
R ₀ JC (Note 1)		T _C = 100°C	1	58	
Continuous Drain		T _A = 25°C	I _D	20	Α
Current R _{0JA} (Notes 1, 2, 3)	Steady	T _A = 100°C		14	
Power Dissipation	State	T _A = 25°C	P_{D}	3.8	W
R _{θJA} (Notes 1, 2)		T _A = 100°C		1.9	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	722	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			Is	96	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 7.0 A)			E _{AS}	1081	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.3	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	40	

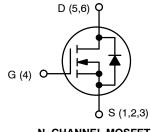
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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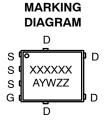
www.onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
80 V	4 mΩ @ 10 V	110 A
	5.2 mΩ @ 4.5 V	IIUA



N-CHANNEL MOSFET





XXXXXX = 6H824L

(NVMFS6H824NL) or

824LWF

(NVMFS6H824NLWF) = Assembly Location

W = Work Week

ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS					•		•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				34.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 \text{ V}, \qquad T_{J} = 25 ^{\circ}\text{C}$				10	1
		V _{DS} = 80 V	T _J = 125°C			100	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{G}$	_S = 20 V			100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 140 \mu A$		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A		3.3	4	mΩ
		V _{GS} = 4.5 V	I _D = 20 A		4.1	5.2	mΩ
Forward Transconductance	9 _F s	V _{DS} = 8 V, I _D	₀ = 50 A		178		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE				•		
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 40 V			2900		pF
Output Capacitance	Coss				366		
Reverse Transfer Capacitance	C _{RSS}				15		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 10 \text{ V}, V_{DS} = 40 \text{ V}; I_D = 50 \text{ A}$ $V_{GS} = 4.5 \text{ V}, V_{DS} = 40 \text{ V}; I_D = 50 \text{ A}$			52		nC
Threshold Gate Charge	Q _{G(TH)}				5		
Gate-to-Source Charge	Q _{GS}				8.7		
Gate-to-Drain Charge	Q_GD				9		
Plateau Voltage	V_{GP}				3		V
Total Gate Charge	Q _{G(TOT)}				25		nC
SWITCHING CHARACTERISTICS (Note:	5)				-		
Turn-On Delay Time	t _{d(ON)}				19		
Rise Time	t _r	$V_{GS} = 4.5 \text{ V, } V_{I}$	ns = 64 V,		111		ns
Turn-Off Delay Time	t _{d(OFF)}	$V_{GS} = 4.5 \text{ V, } V_{E}$ $I_{D} = 50 \text{ A, } R_{G}$	= 2.5 Ω		35		
Fall Time	t _f				11		1
DRAIN-SOURCE DIODE CHARACTERIS	STICS				-		
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V,	T _J = 25°C		0.79	1.2	
		I _S = 20 A	T _J = 125°C		0.65		-
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 50 \text{ A}$			52		
Charge Time	t _a				29		ns
Discharge Time	t _b				23		1
Reverse Recovery Charge	Q _{RR}				59		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

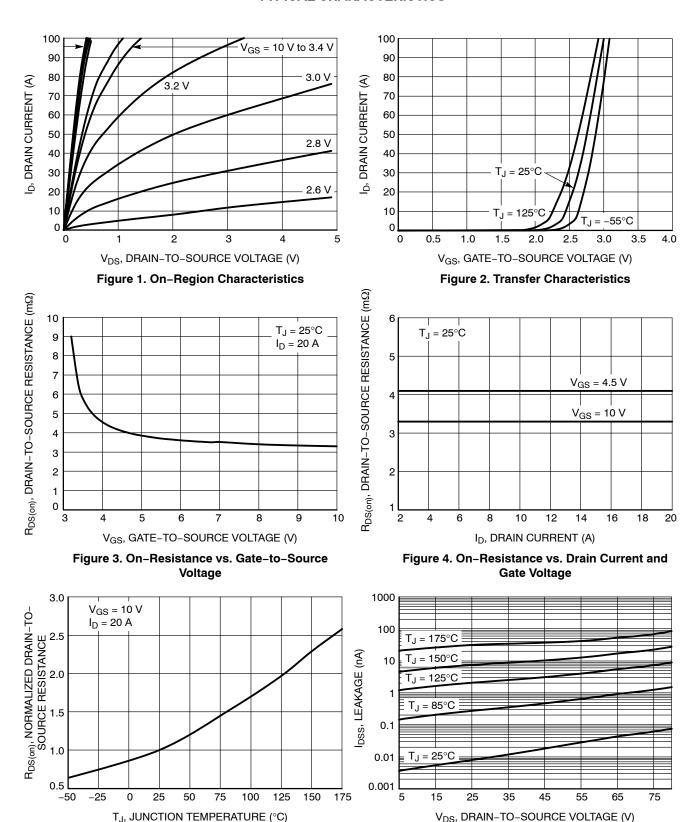


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

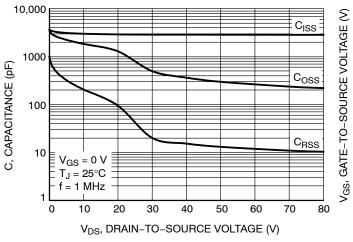


Figure 7. Capacitance Variation

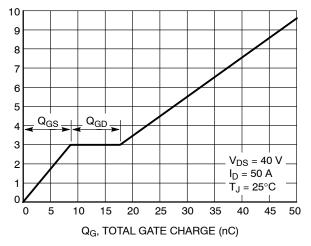


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

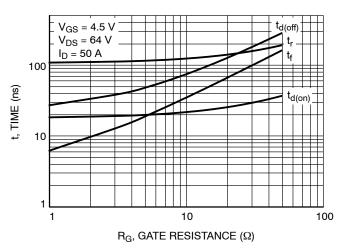


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

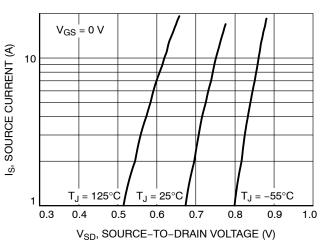


Figure 10. Diode Forward Voltage vs. Current

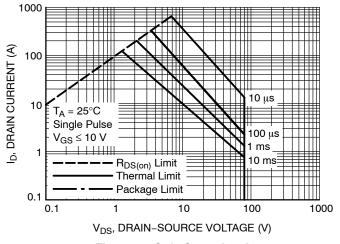


Figure 11. Safe Operating Area

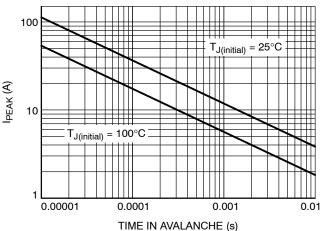


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

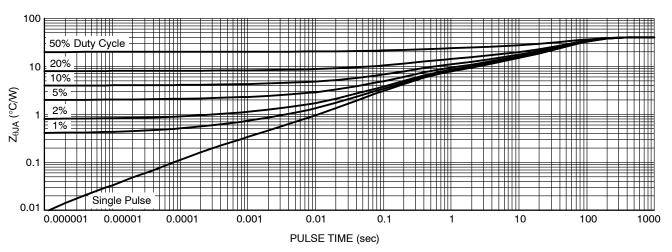


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS6H824NLT1G	6H824L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS6H824NLWFT1G	824LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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0.10

SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA ISSUE N

DATE 25 JUN 2018

NOTES:

BURRS

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
M	3.00	3.40	3.80	
A	0 0		12 °	

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

= Assembly Location Α

Υ = Year W = Work Week ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





DETAIL A

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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