# MOSFET – Power, Single N-Channel 40 V, 3.1 m $\Omega$ , 107 A

# **NVTFS5C453NL**

#### **Features**

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFS5C453NLWF Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parar	Symbol	Value	Unit		
Drain-to-Source Voltag	$V_{DSS}$	40	V		
Gate-to-Source Voltage	9		$V_{GS}$	±20	V
Continuous Drain		T <sub>C</sub> = 25°C	I <sub>D</sub>	107	Α
Current R <sub>θJC</sub> (Notes 1, 3)	Steady	T <sub>C</sub> = 100°C		75	
Power Dissipation	State $T_C = 25^{\circ}C$ $P_D$		$P_{D}$	68	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		34	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	23	Α
Current R <sub>0JA</sub> (Notes 1, 2, 3)	Steady State	T <sub>A</sub> = 100°C		16	
Power Dissipation		T <sub>A</sub> = 25°C	$P_{D}$	3.3	W
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C		1.6	
Pulsed Drain Current	$T_A = 25$	°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	740	Α
Operating Junction and	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		
Source Current (Body D	Is	76	Α		
Single Pulse Drain-to-S Energy (I <sub>L(pk)</sub> = 7 A)	E <sub>AS</sub>	215	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.2	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	46	

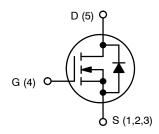
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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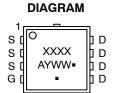
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX	
40 V	3.1 mΩ @ 10 V	107.4	
40 V	5.2 mΩ @ 4.5 V	107 A	



**N-CHANNEL MOSFET** 



WDFN8 (μ8FL) CASE 511AB



**MARKING** 

XXXX = Specific Device Code A = Assembly Location

Y = Year WW = Work Week ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS					•	•	•	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> =	= 250 μΑ	40			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				1.6		mV/°C	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	T <sub>J</sub> = 25 °C			10		
		$V_{DS} = 40 \text{ V}$	T <sub>J</sub> = 125°C			250	μΑ	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA	
ON CHARACTERISTICS (Note 4)					-		-	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D}$	) = 60 μΑ	1.2		2.0	V	
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.3		mV/°C	
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 40 A		2.6	3.1	mΩ	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 40 A		4.1	5.2		
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>I</sub>	<sub>D</sub> = 40 A		120		S	
CHARGES AND CAPACITANCES						•		
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V			2100			
Output Capacitance	Coss				1000		pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>				42			
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 40 A			35			
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 40 A			16		nC	
Threshold Gate Charge	Q <sub>G(TH)</sub>				4.0			
Gate-to-Source Charge	Q <sub>GS</sub>				7.0			
Gate-to-Drain Charge	$Q_{GD}$				5.0			
Plateau Voltage	$V_{GP}$				3.2		V	
SWITCHING CHARACTERISTICS (Note 5	5)				•	•	•	
Turn-On Delay Time	t <sub>d(ON)</sub>				11			
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.5 V, V <sub>E</sub>	ne = 20 V.		110		ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	I <sub>D</sub> = 40 A, R <sub>G</sub>	= 2.5 Ω		21			
Fall Time	t <sub>f</sub>				5		1	
DRAIN-SOURCE DIODE CHARACTERIS	TICS				•	•	•	
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.84	1.2	T	
		I <sub>S</sub> = 40 A	T <sub>J</sub> = 125°C		0.72		V	
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 40 \text{ A}$			41			
Charge Time	t <sub>a</sub>				19		ns	
Discharge Time	t <sub>b</sub>				22			
Reverse Recovery Charge	Q <sub>RR</sub>				30		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**

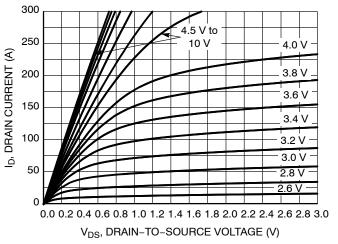


Figure 1. On-Region Characteristics

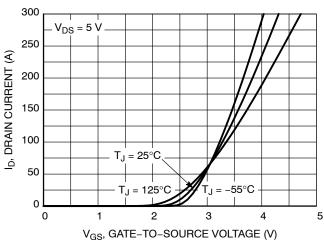


Figure 2. Transfer Characteristics

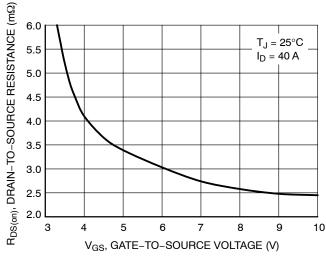


Figure 3. On-Resistance vs. Gate-to-Source Voltage

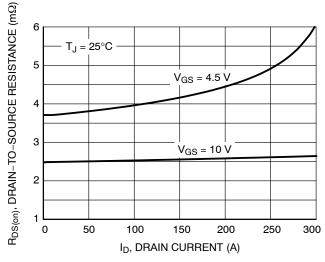


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

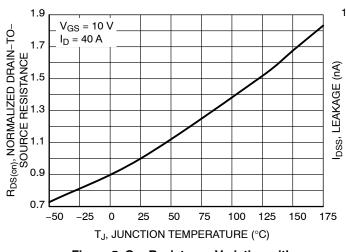


Figure 5. On–Resistance Variation with Temperature

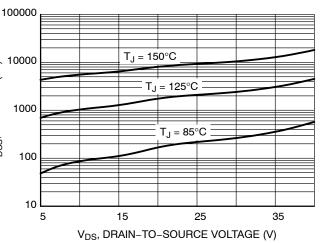
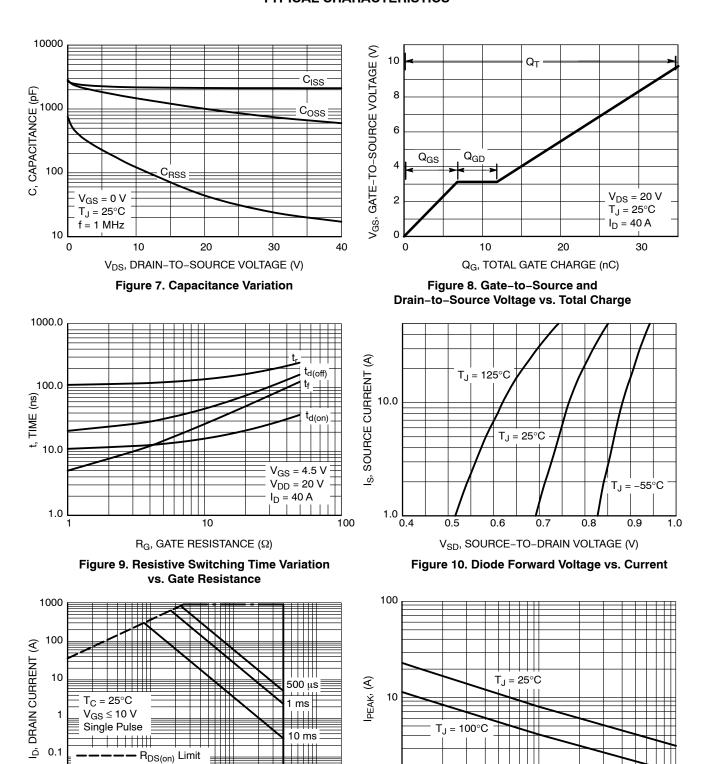


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**



 $V_{DS}\left(V\right)$  Figure 11. Safe Operating Area

10

Thermal Limit Package Limit

0.01

0.1

1E-3

10E-2

100

1 <u>–</u> 1E–4

## **TYPICAL CHARACTERISTICS**

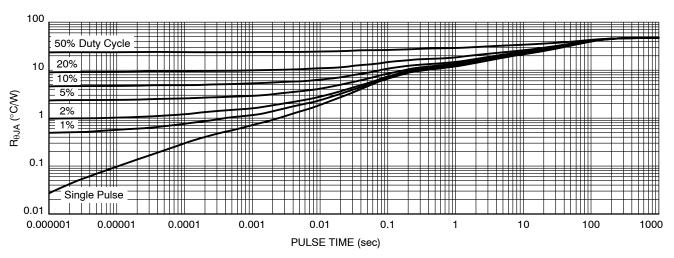


Figure 13. Thermal Characteristics

#### **DEVICE ORDERING INFORMATION**

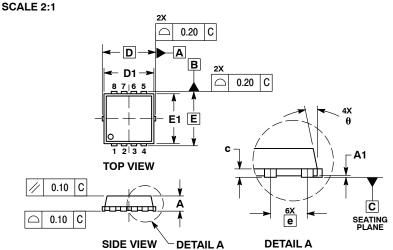
Device	Marking	Package	Shipping <sup>†</sup>
NVTFS5C453NLTAG	453L	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS5C453NLWFTAG	53LW	WDFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



#### WDFN8 3.3x3.3, 0.65P CASE 511AB ISSUE D

**DATE 23 APR 2012** 



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH
  PROTRUSIONS OR GATE BURRS.

	MILLIMETERS				INCHES	
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
С	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC		0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
е	0.65 BSC			(	0.026 BS	0
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
М	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °		12 °	0 °		12 °



#### **GENERIC MARKING DIAGRAM\***

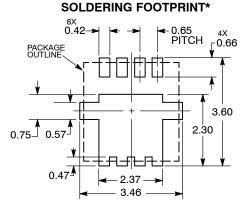


XXXXX = Specific Device Code = Assembly Location

= Year WW = Work Week = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot " ■", may or may not be present.



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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