NTR4503N, NVTR4503N

MOSFET – Power, Single, N-Channel, SOT-23

30 V, 2.5 A

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 4.5 V Rated for Low Voltage Gate Drive
- SOT−23 Surface Mount for Small Footprint (3 x 3 mm)
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- DC−DC Conversion
- Load/Power Switch for Portables
- Load/Power Switch for Computing

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	2.0	A
		T_A = 85°C		1.5	
	t ≤ 10 s	T_A = 25°C		2.5	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.73	W
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	1.5	A
		T_A = 85°C		1.1	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.42	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	10	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150	°C
Source Current (Body Diode)			I_S	2.0	A
Peak Source Current (Diode Forward)		t_p = 10 μs	I_{SM}	4.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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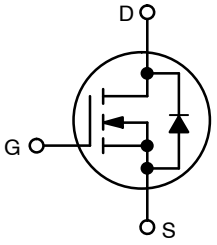
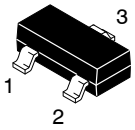
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	85 mΩ @ 10 V	2.5 A
	105 mΩ @ 4.5 V	

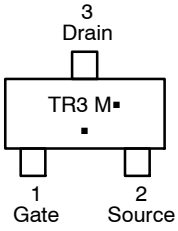
N−Channel





SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



TR3 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR4503NT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel
NVTR4503NT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	170	°C/W
Junction−to−Ambient − t < 10 s (Note 1)	$R_{\theta JA}$	100	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface−mounted on FR4 board using 1 in sq pad size.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	30	36		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V			1.0	μA
		V_{GS} = 0 V, V_{DS} = 24 V, T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.75	3.0	V
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A		85	110	mΩ
		V_{GS} = 4.5 V, I_D = 2.0 A		105	140	
Forward Transconductance	g_{FS}	V_{DS} = 4.5 V, I_D = 2.5 A		5.3		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V		135		pF
Output Capacitance	C_{oss}			52		
Reverse Transfer Capacitance	C_{rss}			15		
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 24 V		130	250	pF
Output Capacitance	C_{oss}			42	75	
Reverse Transfer Capacitance	C_{rss}			13	25	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 2.5 A		3.6	7.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate−to−Source Charge	Q_{GS}			0.6		
Gate−to−Drain Charge	Q_{GD}			0.7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 2.5 A		1.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate−to−Source Charge	Q_{GS}			0.6		
Gate−to−Drain Charge	Q_{GD}			0.9		
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 15 V, I_D = 1 A, R_G = 6 Ω		5.8	12	ns
Rise Time	t_r			5.8	10	
Turn−Off Delay Time	$t_{d(off)}$			14	25	
Fall Time	t_f			1.6	5.0	
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 24 V, I_D = 2.5 A, R_G = 2.5 Ω		4.8		ns
Rise Time	t_r			6.7		
Turn−Off Delay Time	$t_{d(off)}$			13.6		
Fall Time	t_f			1.8		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.0 A		0.85	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 2.0 A, dI_S/dt = 100 A/μs		9.2		ns
Reverse Recovery Charge	Q_{RR}			4.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

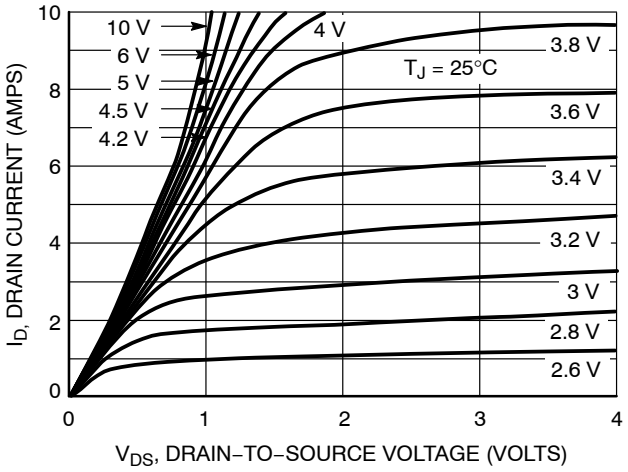


Figure 1. On−Region Characteristics

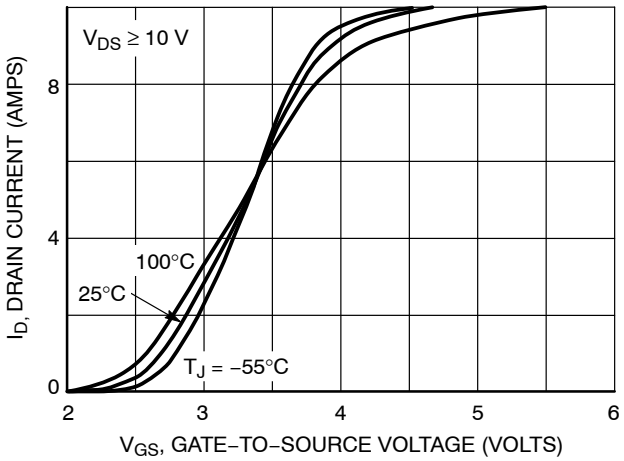


Figure 2. Transfer Characteristics

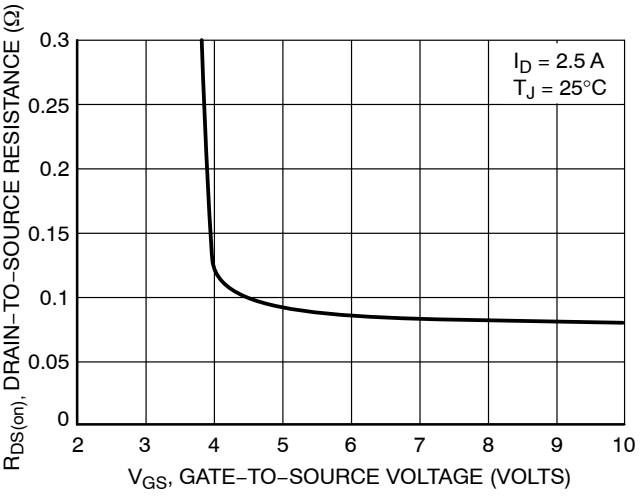


Figure 3. On−Resistance vs. Gate−to−Source Voltage

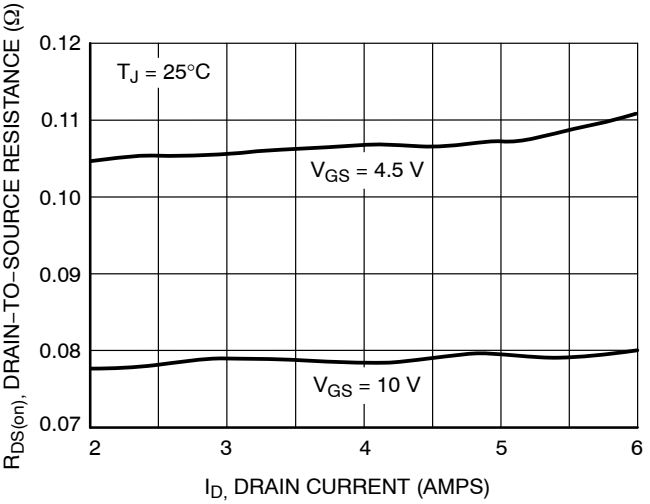


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

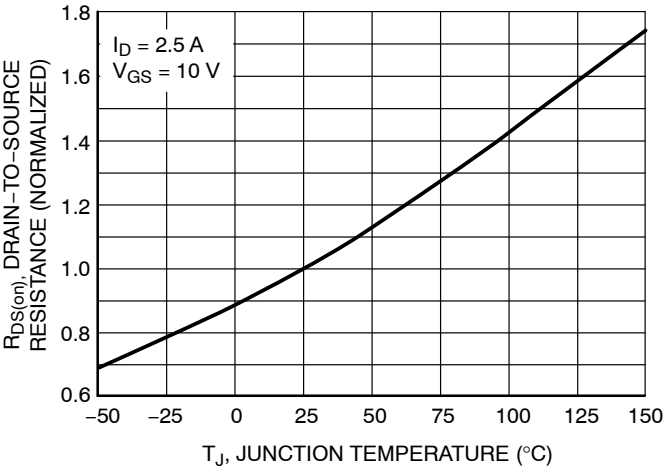


Figure 5. On−Resistance Variation with Temperature

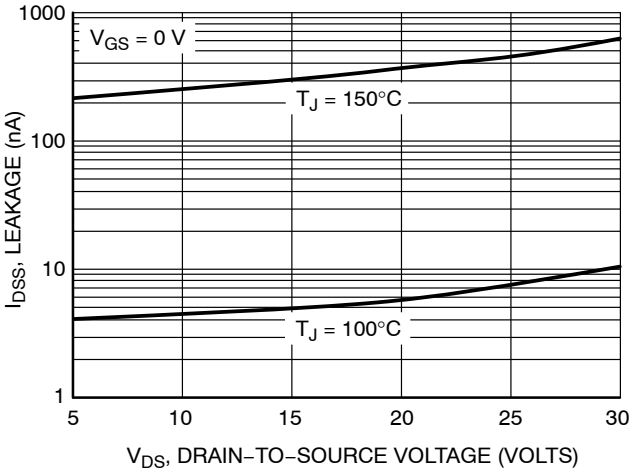


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

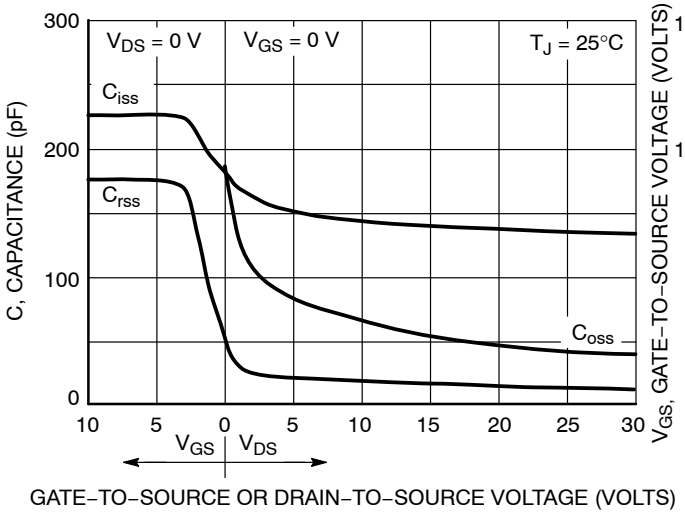


Figure 7. Capacitance Variation

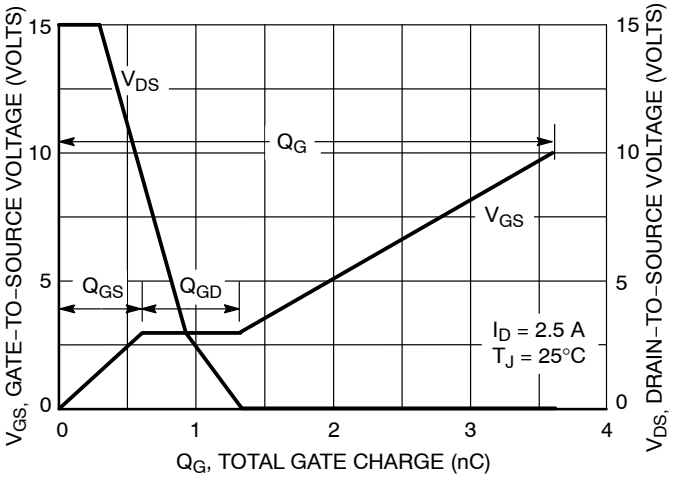


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

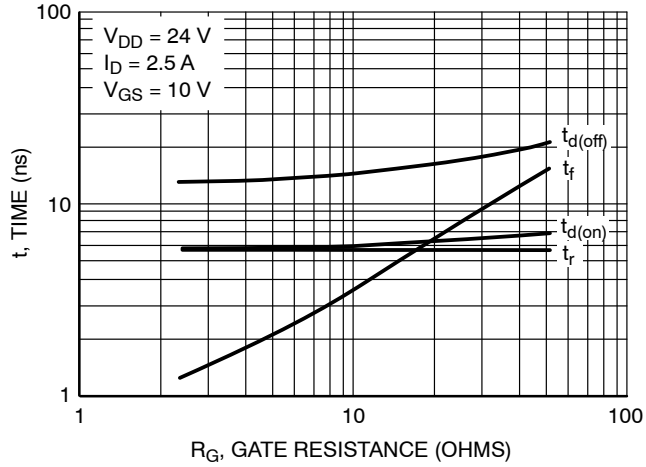


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

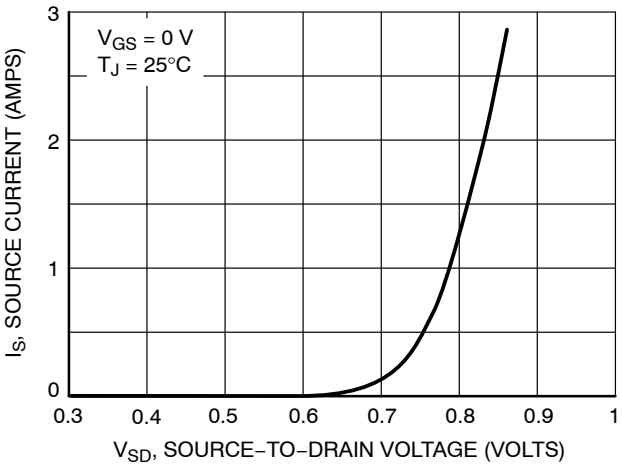
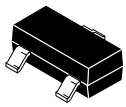


Figure 10. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

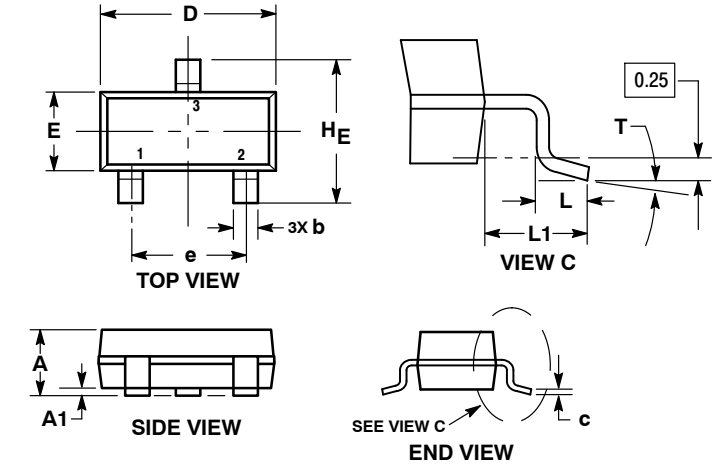
ON Semiconductor®



SOT−23 (TO−236)
CASE 318−08
ISSUE AS

DATE 30 JAN 2018

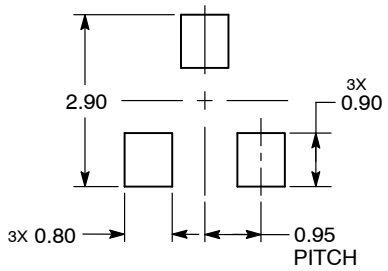
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

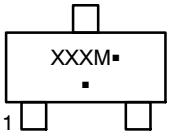
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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DESCRIPTION:	SOT−23 (TO−236)	PAGE 1 OF 1

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