PCS3P7303A

General Purpose Peak EMI Reduction IC

ON Semiconductor®

www.onsemi.com

Functional Description

PCS3P7303A is a versatile, 3.3 V / 2.5 V Peak EMI reduction IC based on TIMING SAFE™ technology. PCS3P7303A accepts an input clock either from a Crystal or from an external reference (AC or DC coupled to XIN / CLKIN) and locks on to it delivering a 1x modulated clock output. PCS3P7303A has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer to the *Frequency Selection* Table for details.

PCS3P7303A has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected between SSEXTR and GND. Modulation Rate (MR) control selects two different Modulation Rates.

PPCS3P7303A operates from a 3.3 V / 2.5 V supply and is available in an 8−pin TSSOP and 8L 2 mm x 2 mm WDFN packages.

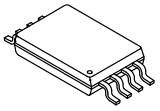
Application

PCS3P7303A is targeted for many applications including USB and SATA.

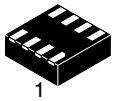
General Features

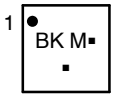
- 1x LVCMOS Peak EMI Reduction
- Input Frequency:
  - 10 MHz − 70 MHz @ 2.5 V
  - 10 MHz − 80 MHz @ 3.3 V
- Output Frequency:
  - 10 MHz − 70 MHz @ 2.5 V
  - 10 MHz − 80 MHz @ 3.3 V
- Analog Deviation Selection
- ModRate Selection Option
- Supply Voltage: 2.5 V ± 0.2 V
  3.3 V ± 0.3 V
- 8−pin TSSOP, 8L 2 mm x 2 mm WDFN (TDFN) Packages
- The First True Drop−in Solution
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS



TSSOP8 4.4x3
CASE 948AL



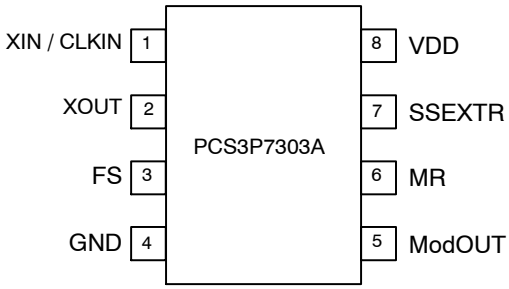


WDFN8 2x2, 0.5P
CASE 511AQ

XX	= Specific Device Code
M	= Date Code
YY, Y	= Year
WW, W	= Work Week
A	= Assembly Location
▪	= Pb−Free Device

(Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

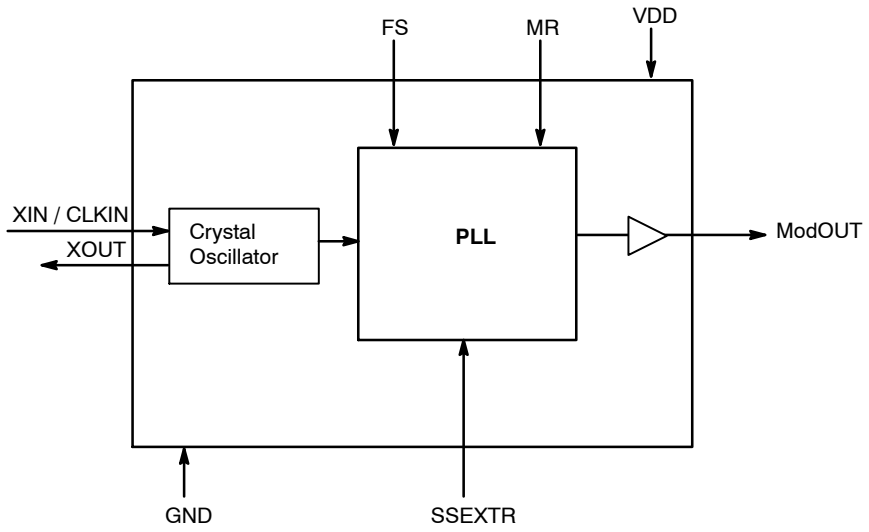


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	XIN / CLKIN	Input	Crystal connection or External reference clock input.
2	XOUT	Output	Crystal connection. If using an external reference, this pin should be left open.
3	FS	Input	Frequency Select. Pull LOW to select Low Frequency range. Selects High Frequency range when pulled HIGH. Has an internal pull−up resistor. (See *Frequency Selection table* for details.)
4	GND	Power	Ground.
5	ModOUT	Output	Buffered Modulated clock output.
6	MR	input	Modulation Rate Select. When LOW selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull−down resistor.
7	SSEXTR	Input	Analog Deviation Selection through external resistor to GND.
8	VDD	Power	2.5 V / 3.3 V supply Voltage.

Table 2. FREQUENCY SELECTION TABLE

VDD (V)	FS	Frequency (MHz)
2.5	0	10 – 35
	1	30 – 70
3.3	0	10 – 40
	1	30 – 80

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	2.3	3.6	V
T_A	Operating Temperature (Ambient Temperature)	−25	+85	°C
C_L	Load Capacitance		10	pF
C_{IN}	Input Capacitance		7	pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS FOR 2.5 V

Parameter	Description	Test Conditions		Min	Typ	Max	Units
VDD	Supply Voltage			2.3	2.5	2.7	V
V_{IL}	Input LOW Voltage					0.7	V
V_{IH}	Input HIGH Voltage			1.7			V
I_{IL}	Input LOW Current	V_{IN} = 0 V				−50	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	μA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA				0.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA		1.8			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled low				500	μA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS = 0; @ 10 MHz			5	mA
			FS = 1; @ 70 MHz			12	
Z_O	Output Impedance				45		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. SWITCHING CHARACTERISTICS FOR 2.5 V

Parameter	Test Conditions			Min	Typ	Max	Units
Input Frequency (Note 1) / ModOUT	FS = 0			10		35	MHz
	FS = 1			30		70	
Duty Cycle (Notes 2, 3)	Measured at V_{DD}/2			45	50	55	%
Output Rise Time (Notes 2, 3)	Measured between 20% to 80%				1.75	2.5	nS
Output Fall Time (Notes 2, 3)	Measured between 80% to 20%				1.0	1.6	nS
Cycle−to−Cycle Jitter (Note 3)	Unloaded output	FS = 0	10 MHz		±450	±600	pS
			35 MHz		±125	±250	
		FS = 1	30 MHz		±225	±350	
			70 MHz		±150	±300	
PLL Lock Time (Note 3)	Stable power supply, valid clock presented on XIN / CLKIN					3	mS

1. Functionality with Crystal is guaranteed by design and characterization. Not 100% tested in production.
2. All parameters are specified with 10 pF loaded outputs.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V

Parameter	Description	Test Conditions		Min	Typ	Max	Units
VDD	Supply Voltage			3.0	3.3	3.6	V
V_{IL}	Input LOW Voltage					0.8	V
V_{IH}	Input HIGH Voltage			2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0 V				−50	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	μA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA				0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA		2.4			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled low				700	μA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS = 0; @ 10 MHz			7	mA
			FS = 1; @ 80 MHz			20	
Z_O	Output Impedance				35		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. SWITCHING CHARACTERISTICS FOR 3.3 V

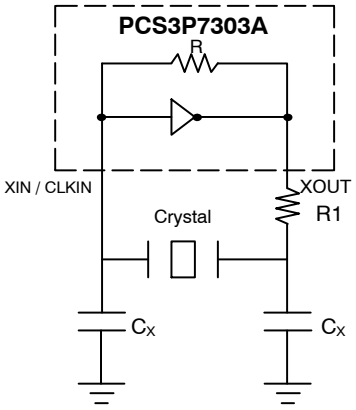
Parameter	Test Conditions			Min	Typ	Max	Units
Input Frequency (Note 1) / ModOUT	FS = 0			10		40	MHz
	FS = 1			30		80	
Duty Cycle (Notes 2, 3)	Measured at V_{DD}/2			45	50	55	%
Output Rise Time (Notes 2, 3)	Measured between 20% to 80%				1.3	2	nS
Output Fall Time (Notes 2, 3)	Measured between 80% to 20%				0.9	1.3	nS
Cycle−to−Cycle Jitter (Note 3)	Unloaded output	FS = 0	10 MHz		±450	±600	pS
			40 MHz		±125	±250	
		FS = 1	30 MHz		±225	±350	
			80 MHz		±125	±250	
PLL Lock Time (Note 3)	Stable power supply, valid clock presented on XIN / CLKIN					3	mS

4. Functionality with Crystal is guaranteed by design and characterization. Not 100% tested in production.
5. All parameters are specified with 10 pF loaded outputs.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 9. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal frequency	25 MHz
Frequency tolerance	±50 ppm or better at 25°C
Operating temperature range	−25°C to +85°C
Storage temperature	−40°C to +85°C
Load capacitance (C_P)	18 pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

NOTE: C_L is the Load Capacitance and R1 is used to prevent oscillations at overtone frequency of the Fundamental frequency.



$C_X = 2*(C_P - C_S)$,
Where C_P = Load capacitance of crystal from crystal vendor datasheet.
C_S = Stray capacitance due to C_{IN}, PCB, Trace, etc.

Figure 2. Typical Crystal Interface Circuit

Switching Waveforms

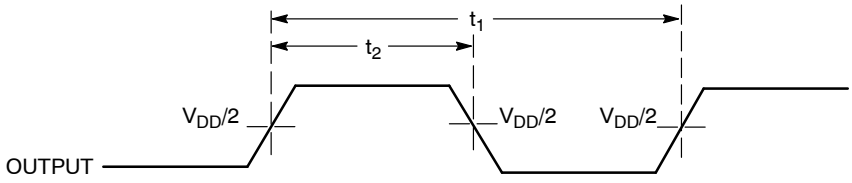


Figure 3. Duty Cycle Timing

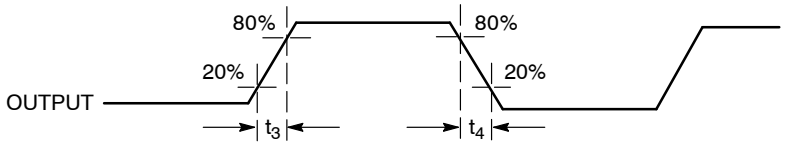
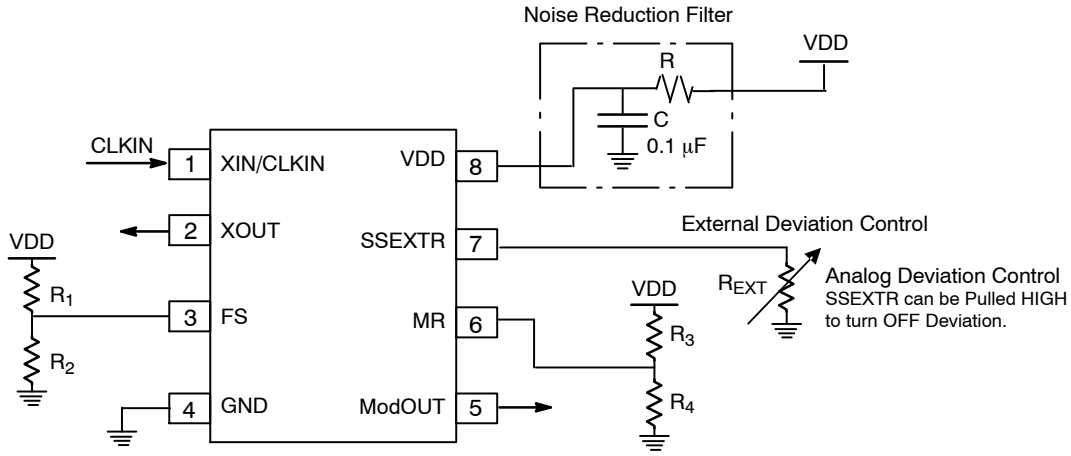


Figure 4. Output Rise/Fall Time

Application Schematic



Note: FS (Pin#3) MR (Pin#6): Connect to VDD or GND
Refer to Pin Description table for Functionality details.
Use 0 Ω resistor at either R_1 or R_2 to configure FS.
Use 0 Ω resistor at either R_3 or R_4 to configure MR.

Figure 5. Application Schematic

Charts

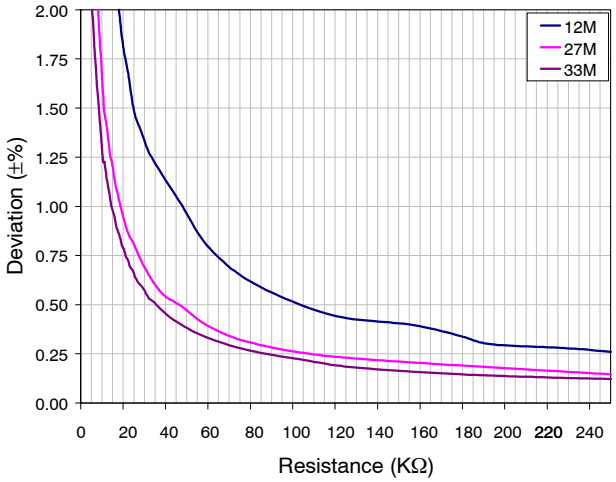


Figure 6. Deviation vs. Resistance (FS = 0, MR = 0)

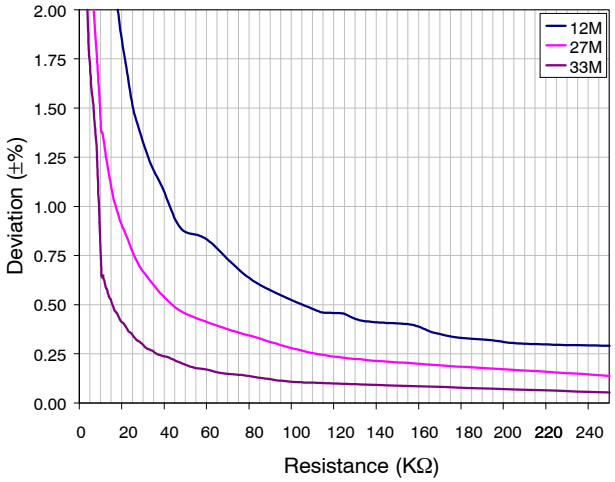


Figure 7. Deviation vs. Resistance (FS = 0, MR = 1)

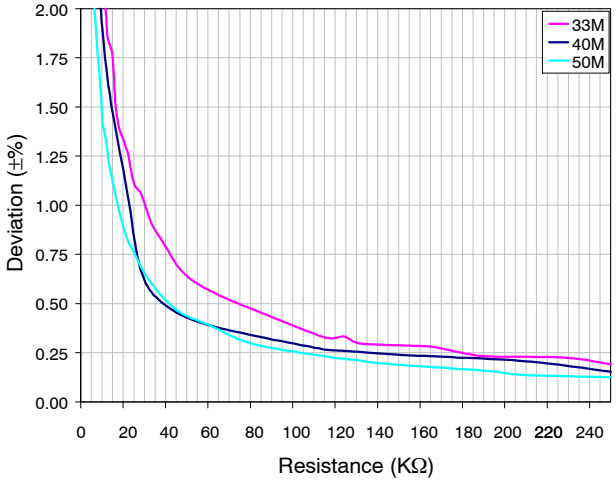


Figure 8. Deviation vs. Resistance (FS = 1, MR = 0)

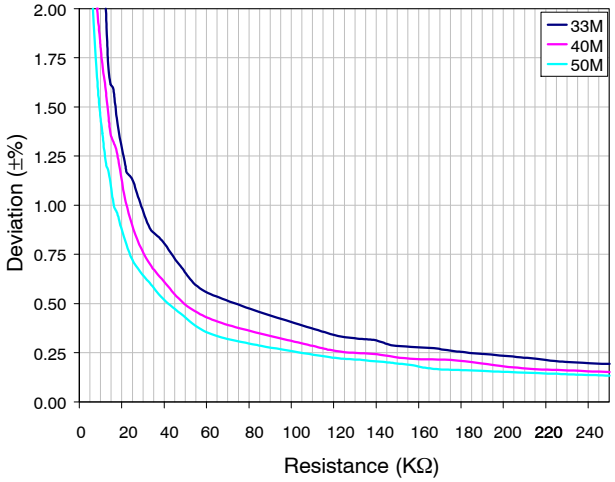


Figure 9. Deviation vs. Resistance (FS = 1, MR = 1)

NOTE: Device to Device variation of Deviation is ±10% (0°C to 70°C) and ±25% (−25°C to +85°C)

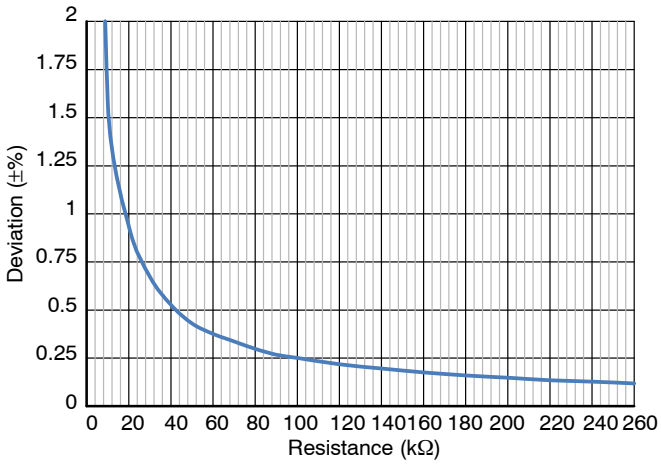


Figure 10. Deviation vs. Resistance (FS = 1, MR = 0) V_{DD} = 3.3 V

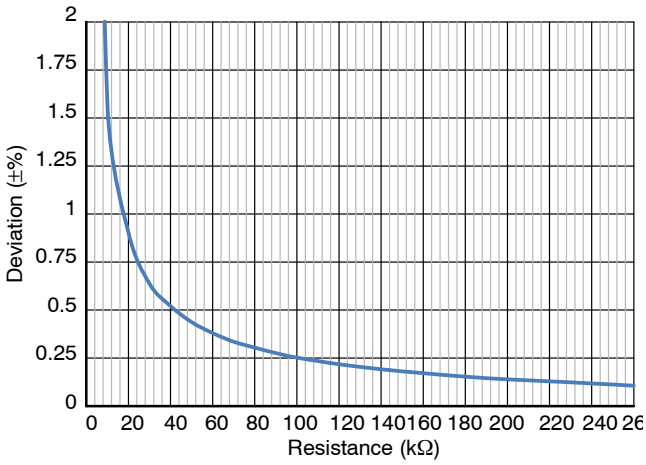


Figure 11. Deviation vs. Resistance (FS = 1, MR = 1) V_{DD} = 3.3 V

Table 10. ORDERING INFORMATION

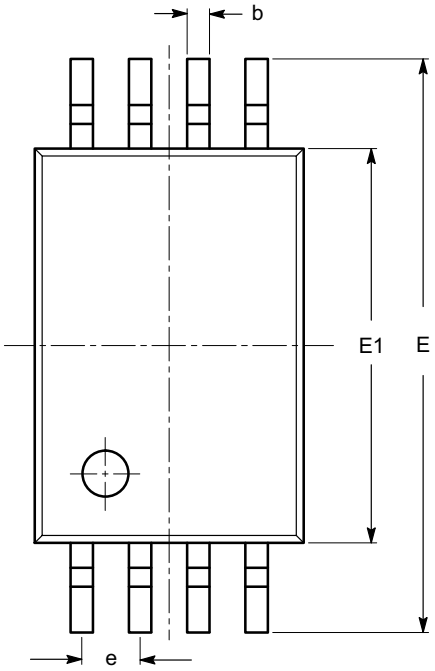
Part Number	Marking	Temperature	Package	Shipping†
PCS3P7303AG−08TR	BKL	−25°C to +85°C	8−pin TSSOP (Pb−Free)	Tape & Reel
PCS3P7303AG−08TT	BKL	−25°C to +85°C	8−pin TSSOP (Pb−Free)	Tube
PCS3P7303AG−08CR	BK	−25°C to +85°C	8L WDFN (2 mm x 2 mm) (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

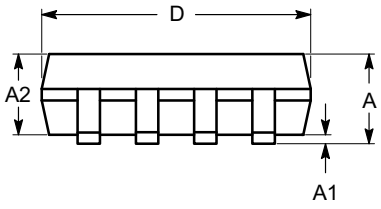
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

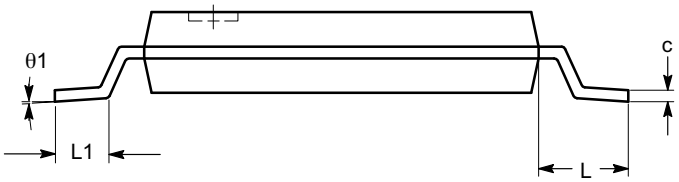


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

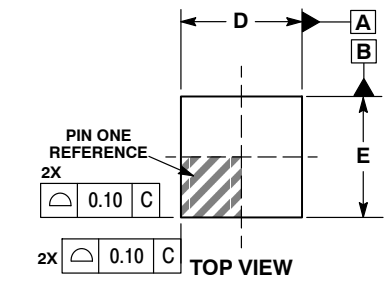


END VIEW

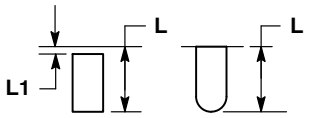
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PACKAGE DIMENSIONS

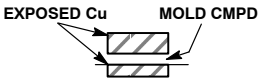
WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A



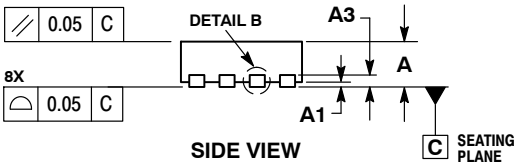
TOP VIEW



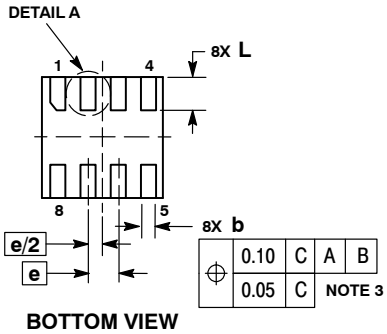
DETAIL A
OPTIONAL
CONSTRUCTIONS



DETAIL B
OPTIONAL
CONSTRUCTION



SIDE VIEW

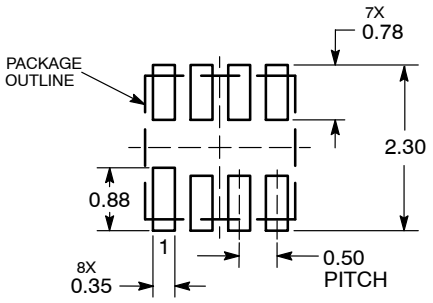


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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