Programmable Precision References

NCP431A, SC431A, NCP431B, SC431B, NCP432B, SC432B Series

The NCP431/NCP432 integrated circuits are three−terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from Vref to 36 V using two external resistors. These devices exhibit a wide operating current range of 40 μA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the NCP431/NCP432 operates as a shunt regulator, it can be used as either a positive or negative voltage reference. Low minimum operating current makes this device an ideal choice for secondary regulators in SMPS adapters with extremely low no−load consumption.

Features

- Programmable Output Voltage to 36 V
- Low Minimum Operating Current: 40 μA, Typ @ 25°C
- Voltage Reference Tolerance: ±0.5%, Typ @ 25°C (NCP431B/NCP432B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 40 μA to 100 mA
- Equivalent Full−Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- SC Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Voltage Adapters
- Switching Power Supply
- Precision Voltage Reference
- Charger
- Instrumentation

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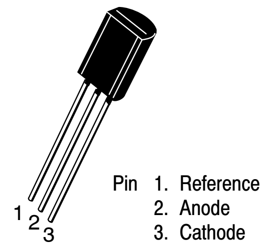
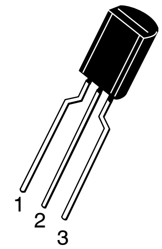


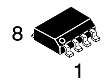
STRAIGHT LEAD
BULK PACK



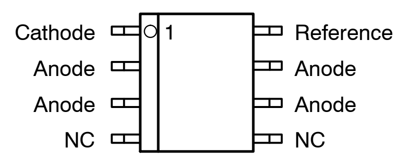
BENT LEAD
TAPE & REEL
AMMO PACK

TO−92
LP SUFFIX
CASE 29−10

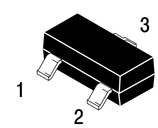
TO−92
LPRA SUFFIX
CASE 29−10



SOIC−8 NB
D SUFFIX
CASE 751



(Top View)



SOT−23
SN SUFFIX
CASE 318

NCP431/SC431	NCP432/SC432
Pin 1. Reference	Pin 1. Cathode
2. Cathode	2. Reference
3. Anode	3. Anode

ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

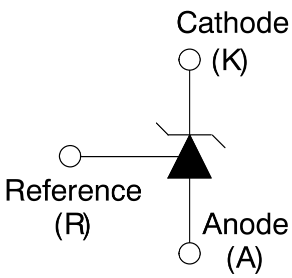


Figure 1. Symbol

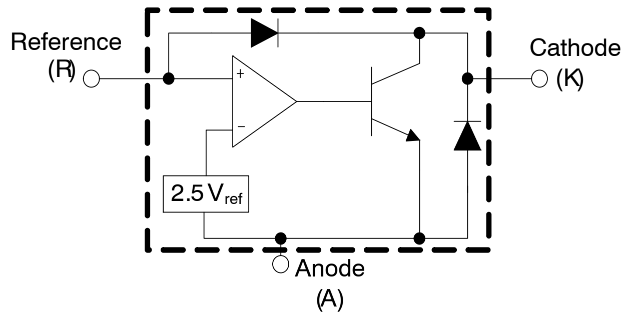


Figure 2. Representative Block diagram

This device contains 20 active transistors

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

Symbol	Rating	Value	Unit
V_{KA}	Cathode to Anode Voltage	37	V
I_K	Cathode Current Range, Continuous	−100 to +150	mA
I_{ref}	Reference Input Current Range, Continuous	−5 to +10	mA
T_J	Operating Junction Temperature	150	°C
T_A	Operating Ambient Temperature Range	−40 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package SN1 Suffix Plastic Package	 0.70 0.52	W
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package	1.5	W
 HBM CDM	ESD Rating (Note 1) Human Body Model per JEDEC JESD22−A114F Charged Device Model per JEDEC JESD22−C101E	 >2000 >1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds ±100 mA per JEDEC standard JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Condition	Min	Max	Unit
V_{KA}	Cathode to Anode Voltage	V_{ref}	36	V
I_K	Cathode Current	0.04	100	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

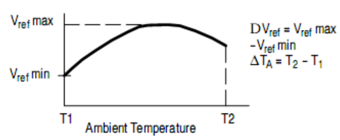
Symbol	Characteristic	LP Suffix Package (50 mm^2 x 35 μm Cu)	D Suffix Package (50 mm^2 x 35 μm Cu)	SN Suffix Package (10 mm^2 x 35 μm Cu)	Unit
$R_{\Theta JA}$	Thermal Resistance, Junction−to−Ambient	176	210	255	°C/W
$R_{\Theta JL}$	Thermal Resistance, Junction−to−Lead (Lead 3)	75	68	80	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	NCP431AC			NCP431AI			NCP431AV/ SC431AV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, I_K = 1 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Figure 3, Note 2)	 2.475 2.475	 2.500 2.500	 2.525 2.525	 2.475 2.465	 2.500 2.500	 2.525 2.525	 2.475 2.460	 2.500 2.500	 2.525 2.525	V
ΔV_{refT}	Reference Input Voltage Deviation Over Temperature Range (Figure 3, Notes 3, 4) $V_{KA} = V_{ref}$, I_K = 1 mA	–	–	–	–	5.0	10	–	10	15	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 1 mA (Figure 4), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	 – –	 −1.85 −0.80	 −3.1 −1.8	 – –	 −1.85 −0.80	 −3.1 −1.8	 – –	 −1.85 −0.80	 −3.1 −1.8	mV/V
I_{ref}	Reference Input Current (Figure 4) I_K = 1 mA, R1 = 220 k, R2 = ∞ T_A = −40°C to +125°C	–	81	190	–	81	190	–	81	190	nA
ΔI_{refT}	Reference Input Current Deviation Over Temperature Range (Figure 4, Note 3) I_K = 1 mA, R1 = 10 k, R2 = ∞	–	22	55	–	22	55	–	22	55	nA
I_{min}	Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 3)	–	40	60	–	40	60	–	40	60	μA
I_{off}	Off−State Cathode Current (Figure 5) V_{KA} = 36 V, V_{ref} = 0 V	–	180	1000	–	180	1000	–	180	1000	nA
$\lvert Z_{KA}\rvert$	Dynamic Impedance (Figure 3, Note 5) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	–	0.22	0.5	–	0.22	0.5	–	0.22	0.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. T_{low} = −40°C for NCP431AI, NCP431AV, SC431AV
   = 0°C for NCP431AC
   T_{high} = 70°C for NCP431AC
   = 85°C for NCP431AI
   = 125°C for NCP431AV, SC431AV
3. Guaranteed by design
4. The deviation parameter ΔV_{refT} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, Vref is defined as:

$$V_{ref}\frac{ppm}{^\circ C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref@25^\circ C}}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\left(V_{ref@25^\circ C}\right)}$$

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature.

Example: ΔV_{refT} = 17 mV and slope is positive
V_{ref} = 2.5 V, ΔT_A = 165°C (from −40°C to +125°C)

$$\alpha V_{ref} = \frac{0.017 \cdot 10^6}{165 \cdot 2.5} = 41.2\ ppm/^\circ C$$

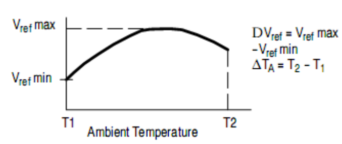
5. The dynamic impedance Z_{KA} is defined as: ($|Z_{KA}| = (\Delta V_{KA}/\Delta I_K)$. When the device is programmed with two external resistors, R1 and R2, the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}|$ (1 + (R1/R2)).
6. SC431AVSNT1G – T_{low} = −40°C, T_{high} = 125°C. Guaranteed by design. SC Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	NCP431BC NCP432BC			NCP431BI NCP432BI			NCP/SC431BV NCP/SC432BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, I_K = 1 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Figure 3, Note 7)	 2.4875 2.4875	 2.500 2.500	 2.5125 2.5125	 2.4875 2.4775	 2.500 2.500	 2.5125 2.5125	 2.4875 2.4725	 2.500 2.500	 2.5125 2.5125	V
ΔV_{refT}	Reference Input Voltage Deviation Over Temperature Range (Figure 3, Notes 8, 9) $V_{KA} = V_{ref}$, I_K = 1 mA	– –	–	– –	– –	5.0	10 1–	– –	10	15 15	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 1 mA (Figure 4), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	– –	−1.85 −0.80	−3.1 −1.8	– –	−1.85 −0.80	−3.1 −1.8	– –	−1.85 −0.80	−3.1 −1.8	mV/V
I_{ref}	Reference Input Current (Figure 4) I_K = 1 mA, R1 = 220 k, R2 = ∞ T_A = −40°C to +125°C	–	81	190	–	81	190	–	81	190	nA
ΔI_{refT}	Reference Input Current Deviation Over Temperature Range (Figure 4, Note 8) I_K = 1 mA, R1 = 10 k, R2 = ∞	–	22	55	–	22	55	–	22	55	nA
I_{min}	Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 3)	–	40	60	–	40	60	–	40	60	μA
I_{off}	Off−State Cathode Current (Figure 5) V_{KA} = 36 V, V_{ref} = 0 V	–	180	1000	–	180	1000	–	180	1000	nA
$\|Z_{KA}\|$	Dynamic Impedance (Figure 3, Note 10) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	–	0.22	0.5	–	0.22	0.5	–	0.22	0.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. T_{low} = −40°C for NCP431BI, NCP431BV, NCP432BI, NCP432BV, SC431B, SC432B
   = 0°C for NCP431BC, NCP432BC
   T_{high} = 70°C for NCP431BC, NCP432BC
   = 85°C for NCP431BI, NCP432BI
   = 125°C for NCP431BV, NCP432BV, SC431BV, SC432BV
8. Guaranteed by design
9. The deviation parameter ΔV_{refT} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, Vref is defined as:

$$V_{ref}\frac{ppm}{^\circ C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref@25^\circ C}}\right)\times 10^6}{\Delta T_A} = \frac{\Delta V_{ref}\times 10^6}{\Delta T_A\left(V_{ref@25^\circ C}\right)}$$

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature.

Example: ΔV_{refT} = 17 mV and slope is positive
V_{ref} = 2.5 V, ΔT_A = 165°C (from −40°C to +125°C)

$$\alpha V_{ref} = \frac{0.017\cdot 10^6}{165\cdot 2.5} = 41.2\ ppm/^\circ C$$

10. The dynamic impedance Z_{KA} is defined as: ($|Z_{KA}| = (\Delta V_{KA}/\Delta I_K)$. When the device is programmed with two external resistors, R1 and R2, the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}|$ (1 + (R1/R2))
11. SC431BVSNT1G, SC432BVSNT1G − T_{low} = −40°C, T_{high} = 125°C. Guaranteed by design. SC Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

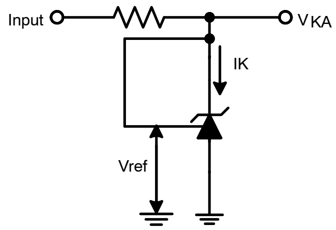


Figure 3. Test Circuit for $V_{KA} = V_{ref}$

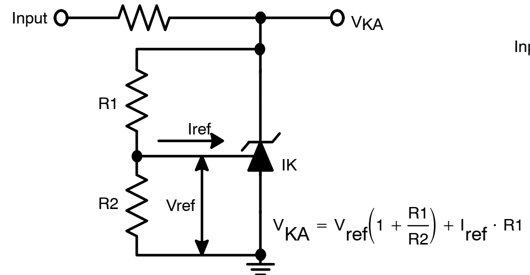


Figure 4. Test Circuit for $V_{KA} > V_{ref}$

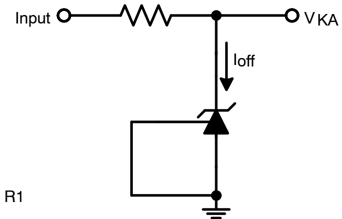


Figure 5. Test Circuit for I_{off}

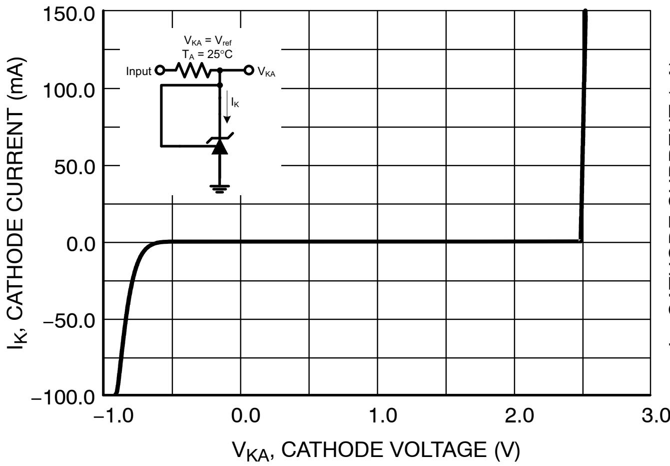


Figure 6. Cathode Current versus Cathode Voltage

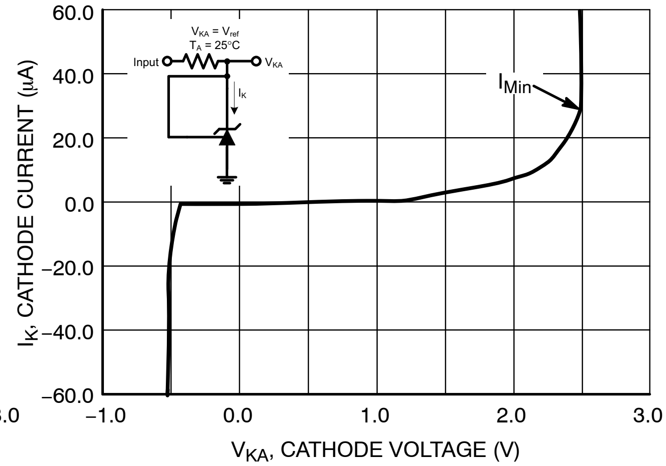


Figure 7. Cathode Current versus Cathode Voltage

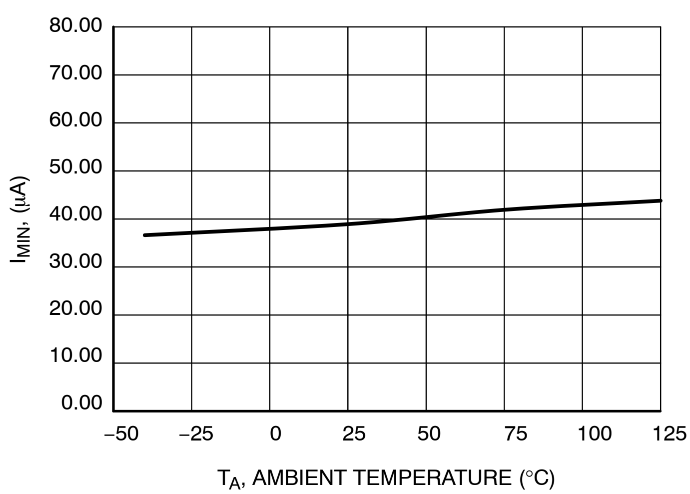


Figure 8. Minimum Cathode Current Regulation versus Ambient Temperature

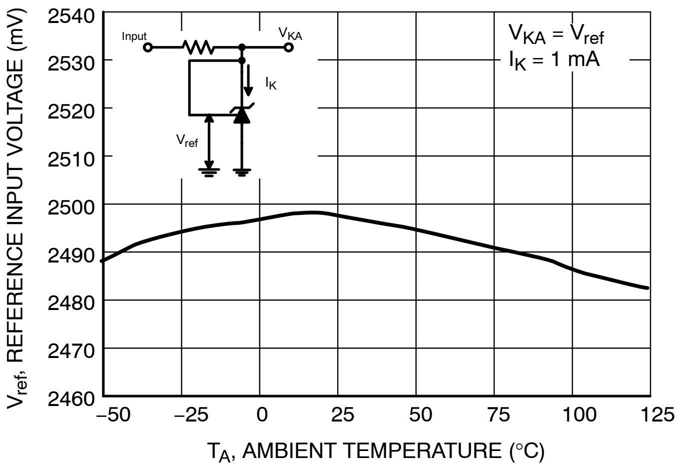


Figure 9. Reference Input Voltage versus Ambient temperature

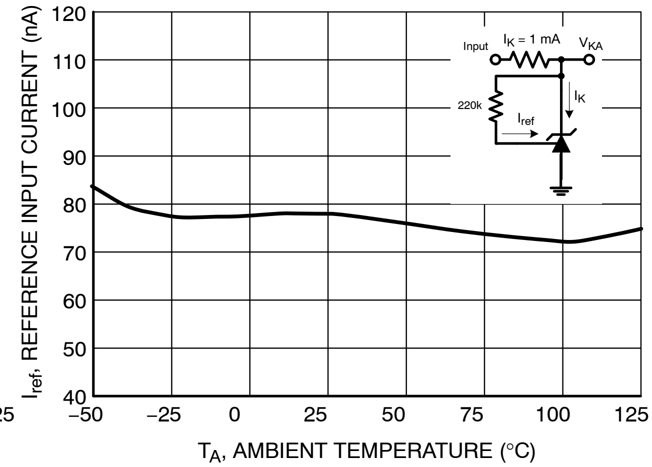


Figure 10. Reference Input Current versus Ambient temperature

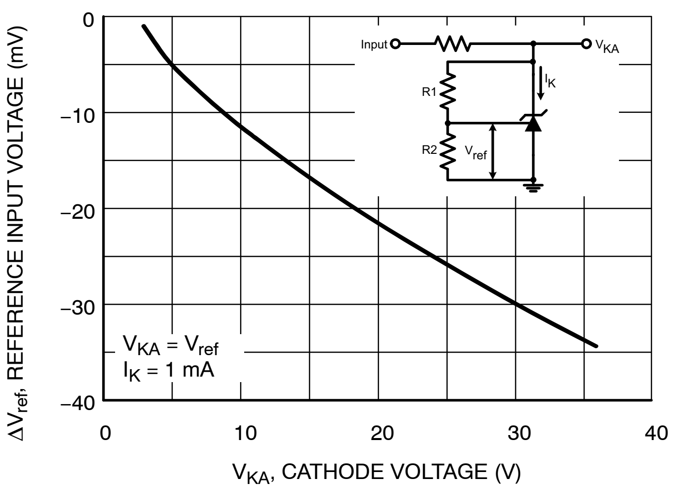


Figure 11. Change in Reference Input Voltage versus Cathode Voltage

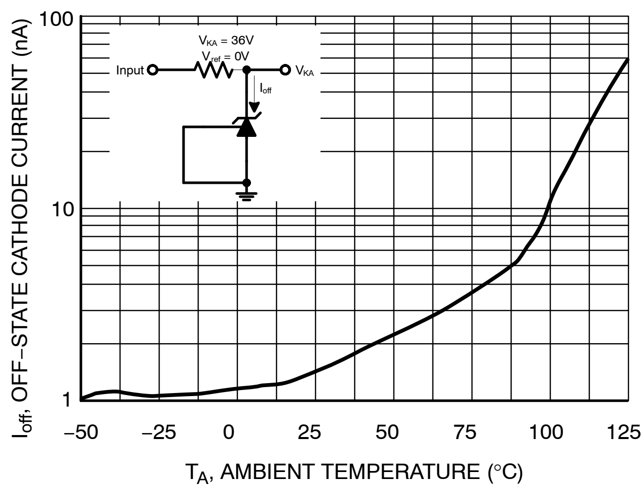


Figure 12. Off−State Cathode Current versus Ambient Temperature

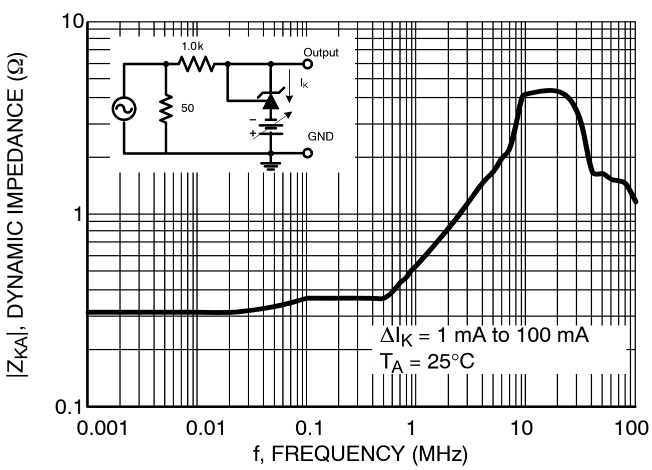


Figure 13. Dynamic Impedance versus Frequency

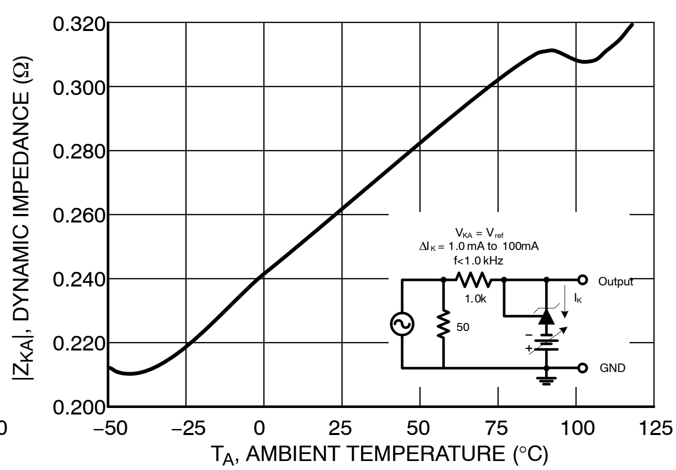


Figure 14. Dynamic Impedance versus Ambient Temperature

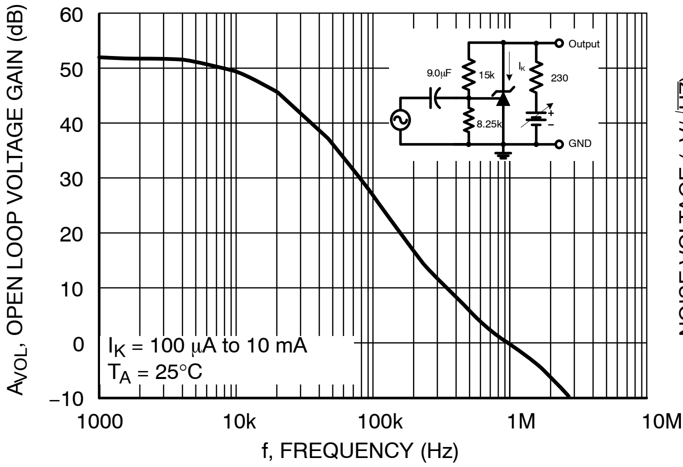


Figure 15. Open−Loop Voltage Gain versus Frequency

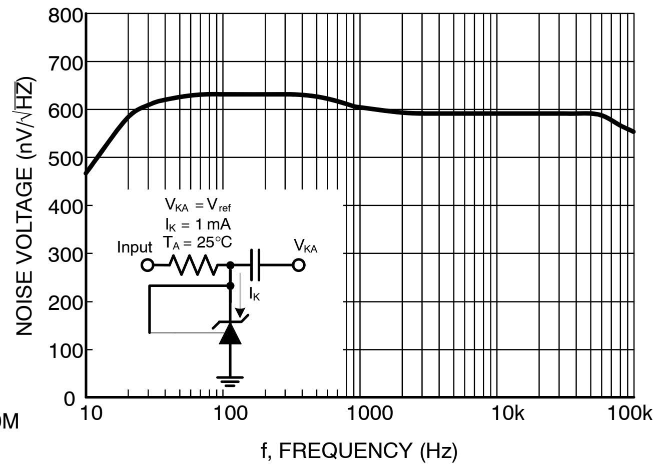


Figure 16. Spectral Noise Density

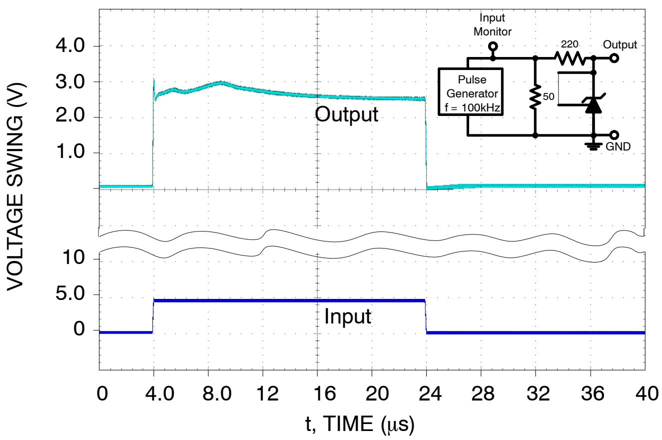


Figure 17. Pulse Response

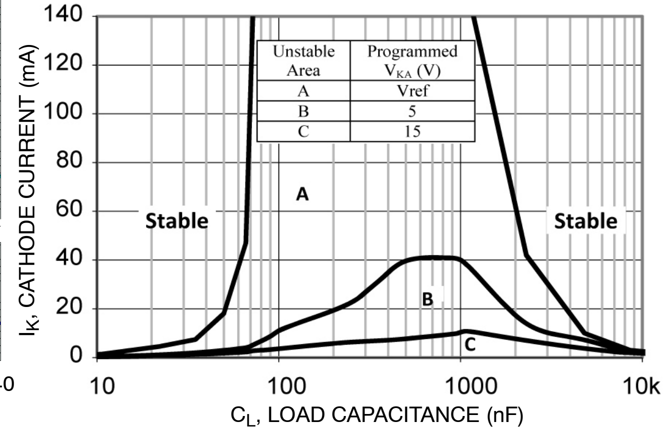


Figure 18. Stability Boundary Conditions

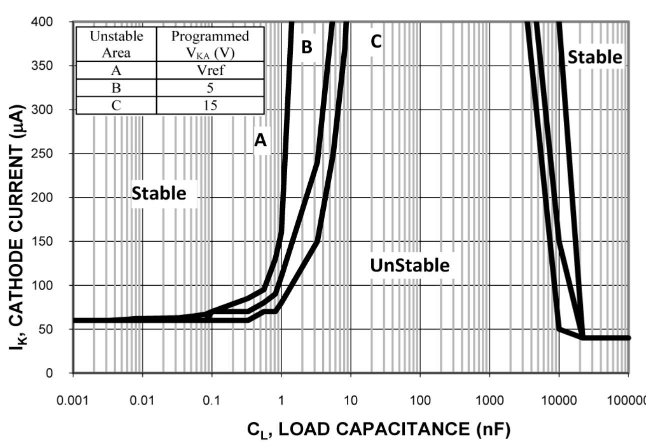


Figure 19. Stability Boundary Conditions for Small Cathode Current

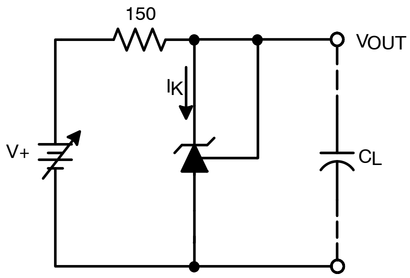


Figure 20. Test Circuit For Curve A of Stability Boundary Conditions

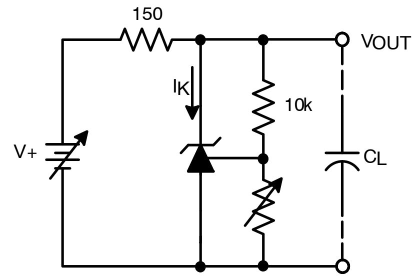
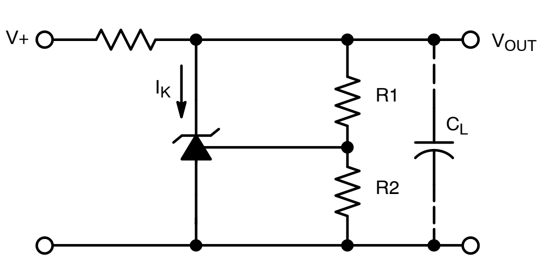


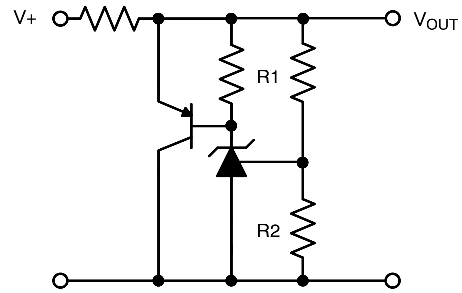
Figure 21. Test Circuit For Curve B And C of Stability Boundary Conditions

TYPICAL APPLICATIONS



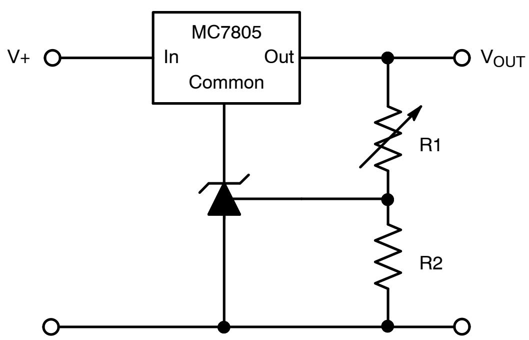
$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 22. Shunt Regulator



$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

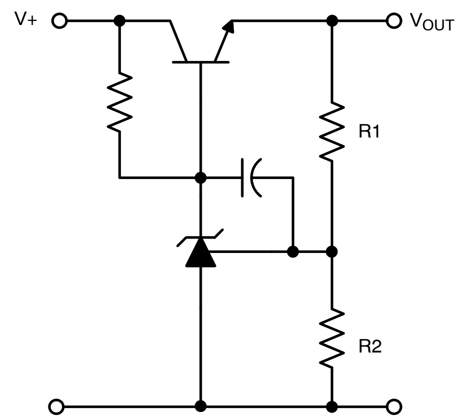
Figure 23. High Current Shunt Regulator



$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{OUT(min)} = V_{ref} + 5.0\ V$$

Figure 24. Output Control for a Tree−Terminal Fixed Regulator

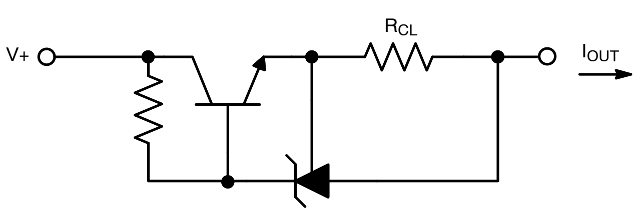


$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{IN(min)} = V_{OUT} + V_{be}$$

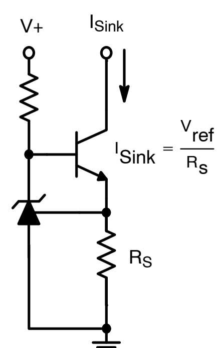
$$V_{OUT(min)} = V_{ref}$$

Figure 25. Series Pass Regulator



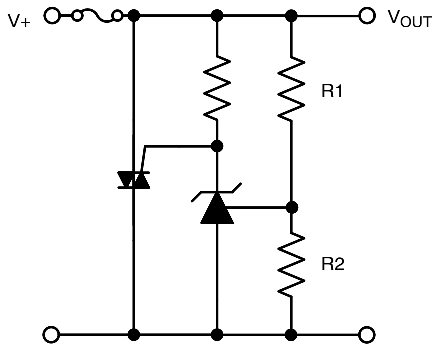
$$I_{OUT} = \frac{V_{ref}}{R_{CL}}$$

Figure 26. Constant Current Source



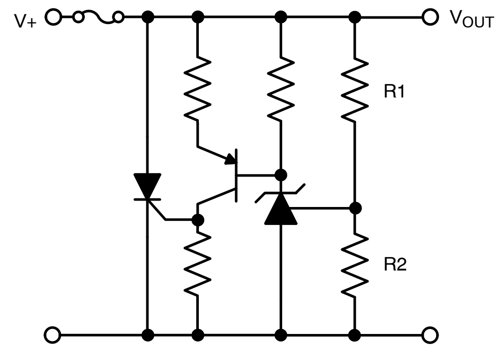
$$I_{Sink} = \frac{V_{ref}}{R_S}$$

Figure 27. Constant Current Sink



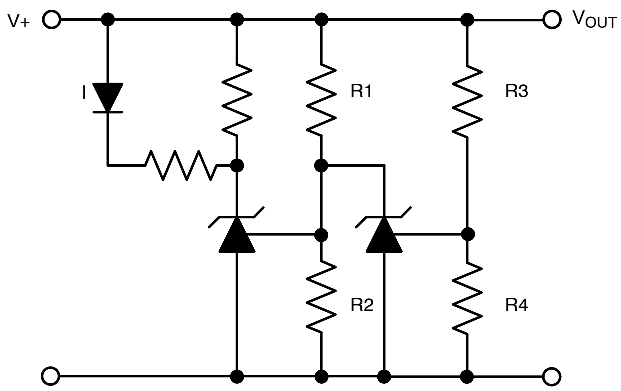
$V_{OUT(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$

Figure 28. Triac Crowbar



$V_{OUT(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$

Figure 29. SRC Crowbar

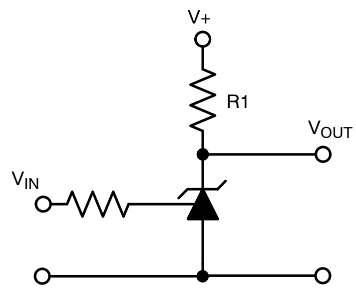


L.E.D. indicator is 'on' when V+ is between the uppper and lower limits.

$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$

$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$

Figure 30. Voltage Monitoring



V_{IN}	V_{OUT}
< V_{ref}	V+
> V_{ref}	≈2.0 V

$V_{th} = V_{ref}$

Figure 31. Single-Supply Comparator with Temperature-Compensated Threshold

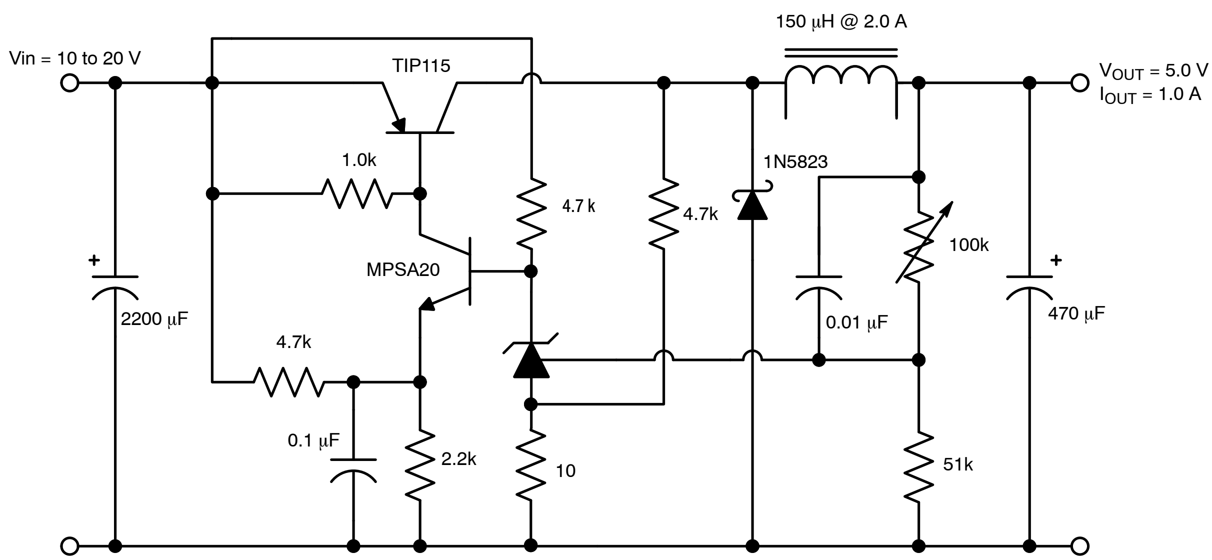


Figure 32. Step-Down Switching Converter

APPLICATIONS INFORMATION

The NCP431/NCP432 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non−standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 18. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the NCP431/NCP432 is shown in Figure 33. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, CP2. The voltage across CP2 drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:
Vref = 1.78 V
Gm = 0.3 + 2.7 exp (−IC/26 mA)
where IC is the device cathode current and Gm is in mhos
Go = 1.25 (Vcp2) µmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi \cdot 1.0M \cdot 20\ pF} = 7.96\ kHz$$

$$P2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi \cdot 10M \cdot 0.265\ pF} = 60\ kHz$$

$$Z1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi \cdot 15.9k \cdot 20\ pF} = 500\ kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the NCP431 is:

$$G = G_M R_{GM} G_o R_L$$

Example 1:
I_C=10 mA, R_L= 230 Ω,C_L= 0. Define the transfer gain.
The DC gain is:

$$G = G_M R_{GM} G_o R_L = (2.138)(1.0M)(1.25\mu)(230) = 615 = 56\ dB$$

$$\text{Loop gain} = G \frac{8.25k}{8.25k + 15k} = 218 = 47\ dB$$

The resulting transfer function Bode plot is shown in Figure 34. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9°. This model matches the Open−Loop Bode Plot of Figure 15. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44°.

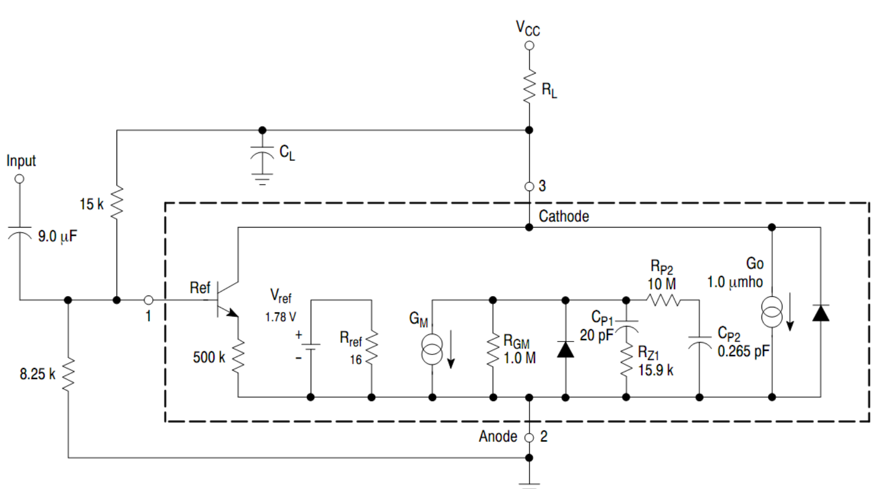


Figure 33. Simplified NCP431/NCP432 Device Model

NCP431/NCP432 OPEN−LOOP VOLTAGE GAIN VERSUS FREQUENCY

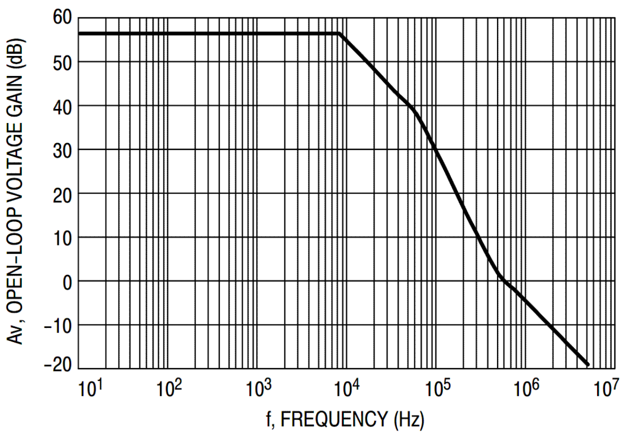


Figure 34. Example 1 Circuit Open Loop Gain Plot

NCP431/NCP432 OPEN−LOOP BODE PLOT WITH LOAD CAP

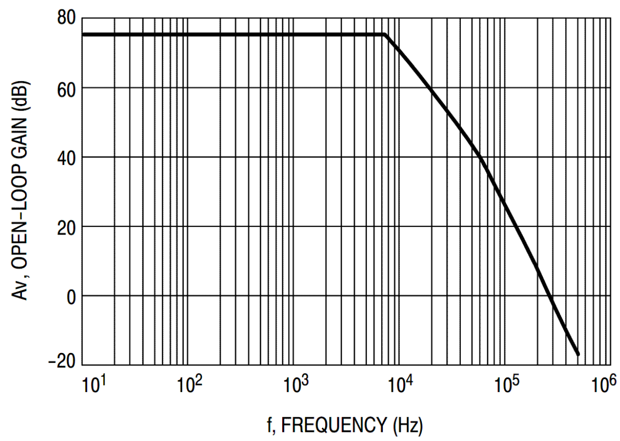


Figure 35. Example 2 Circuit Open Loop Gain Plot

Example 2.
I_C = 7.5 mA, R_L = 2.2 kΩ, C_L = 0.01 μF. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 18) shows that this value of load capacitance and cathode current is on the boundary.

Define the transfer gain.
The DC gain is:

$$G = G_M R_{GM} GoR_L = (2.138)(1.0M)(1.25\mu)(230) = 6389 = 76\text{ dB}$$

The resulting open loop Bode plot is shown in Figure 35. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{\left(1 + \frac{jf}{500\text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0\text{ kHz}}\right)\left(1 + \frac{jf}{60\text{ kHz}}\right)\left(1 + \frac{jf}{7.2\text{ kHz}}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about −46°. Therefore, instability of this circuit is likely.

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

The NCP431/NCP432 is often used as a regulator in secondary side of a switch mode power supply (SMPS).

The benefit of this reference is high and stable gain under low bias currents. Figure 36 shows dependence of the gain (dynamic impedance) on the bias current. Value of minimum cathode current that is needed to assure stable gain is 80 μA maximum.

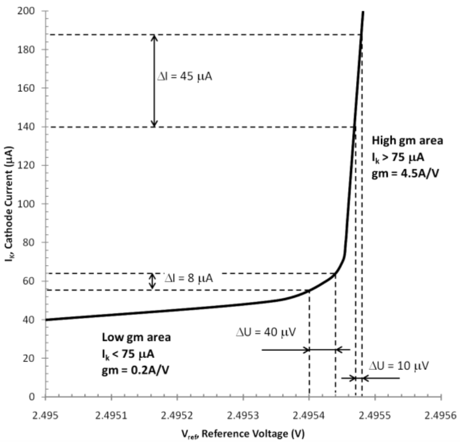


Figure 36. Knee of Reference

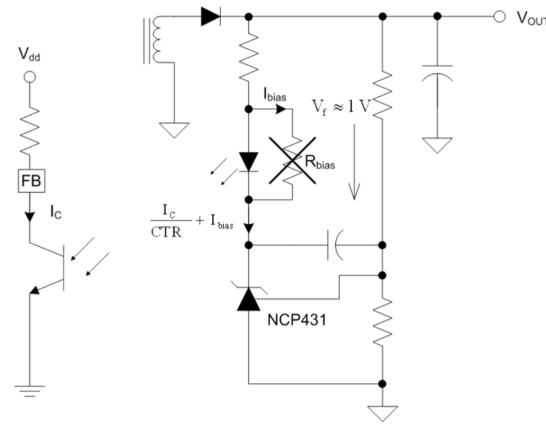


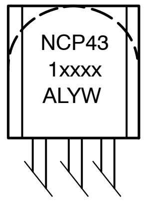
Figure 37. SMPS Secondary Side and Feedback Connection on Primary Side

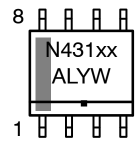
Regulator with TL431 or other references in secondary side of a SMPS needs bias resistor to increase cathode current to reach high and stable gain (refer to Figure 37). This bias resistor does not have to be used in regulator with NCP431/NCP432 thanks to its low minimum cathode current.

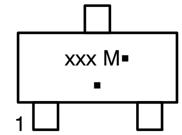
The NCP431/NCP432 operates with very low leakage and reference input current. Sum of these currents is lower than 100 nA. Regulator with the NCP431/NCP432 minimizes parasitic power consumption.

The best way to achieve extremely low no−load consumption in SMPS applications is to use NCP431/NCP432 as regulator on the secondary side. The consumption is reduced by minimum parasitic consumption and very low bias current of NCP431/NCP432.

MARKING DIAGRAMS







xx, xxx, xxx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
M = Date Code
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Marking	Tolerance	Operating Temperature Range	Package	Shipping†
NCP431ACDR2G	AC	1%		SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431ACSNT1G	VRF	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431BCSNT1G	VRJ	0.5%	0°C to 70°C	SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BCSNT1G	VRM	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431ACLPRAG	ACLP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AIDR2G	AI	1%		SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431AISNT1G	VRG	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431BISNT1G	VRK	0.5%	−40°C to 85°C	SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BISNT1G	VRN	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431AILPRAG	AILP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AVDR2G	AV	1%		SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431AVSNT1G / SC431AVSNT1G*	VRH	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431AVLPRAG	AVLP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AVLPG	AVLP	1%	−40°C to 125°C	TO−92 (TO−226) (Pb−Free)	2000 Units / Bag
NCP431BVSNT1G / SC431BVSNT1G*	VRL	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BVSNT1G / SC432BVSNT1G*	VRP	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*SC Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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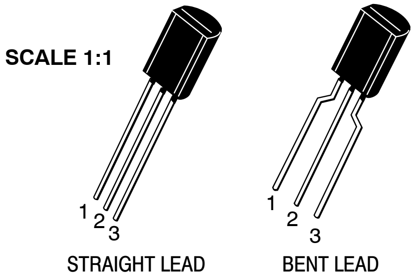
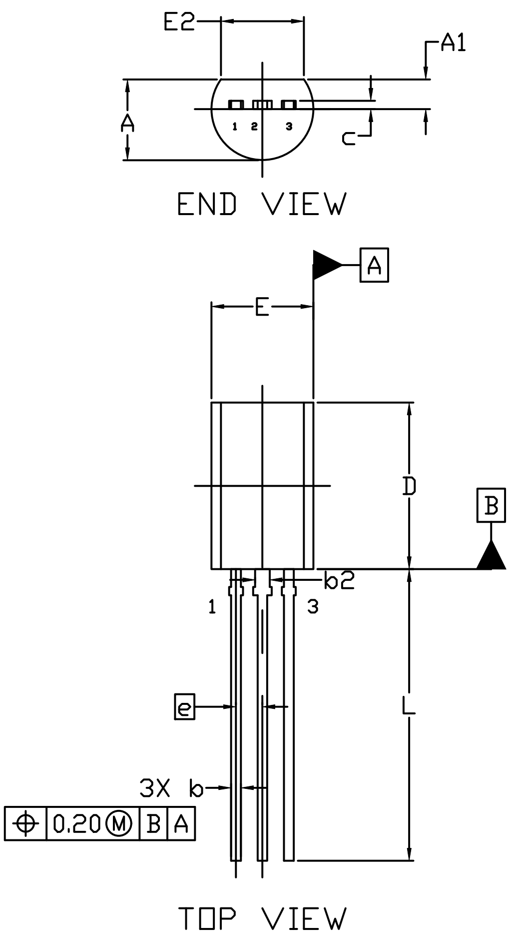


TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

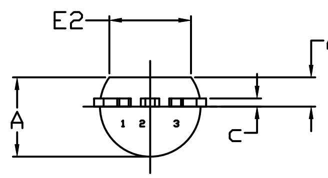
STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 3**

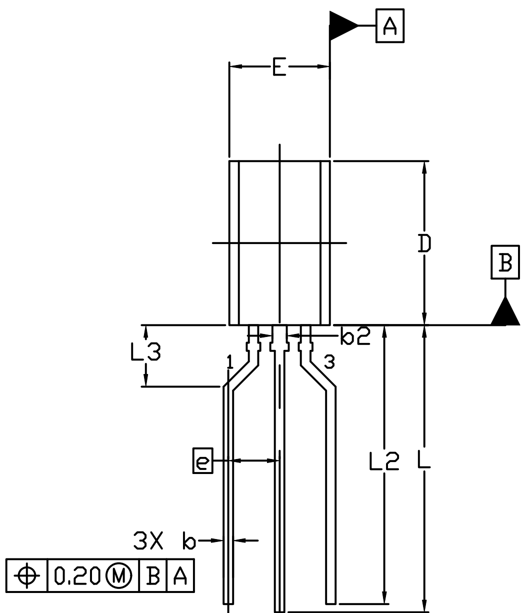
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 2 OF 3**

TO−92 (TO−226) 1 WATT

CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

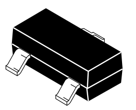
GENERIC MARKING DIAGRAM*

XXXXX
XXXXX
ALYW▪
▪

XXXX	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

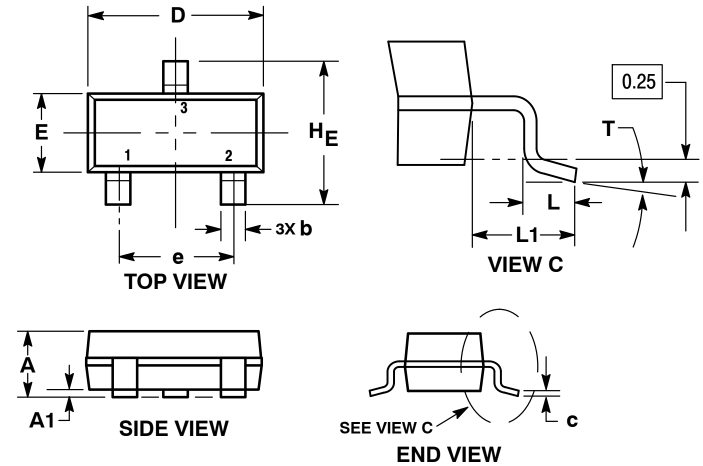
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



SCALE 4:1

SOT−23 (TO−236)
CASE 318−08
ISSUE AS

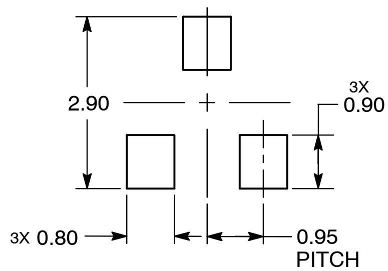
DATE 30 JAN 2018



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

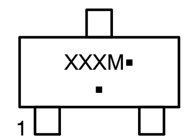
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

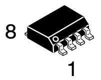
STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

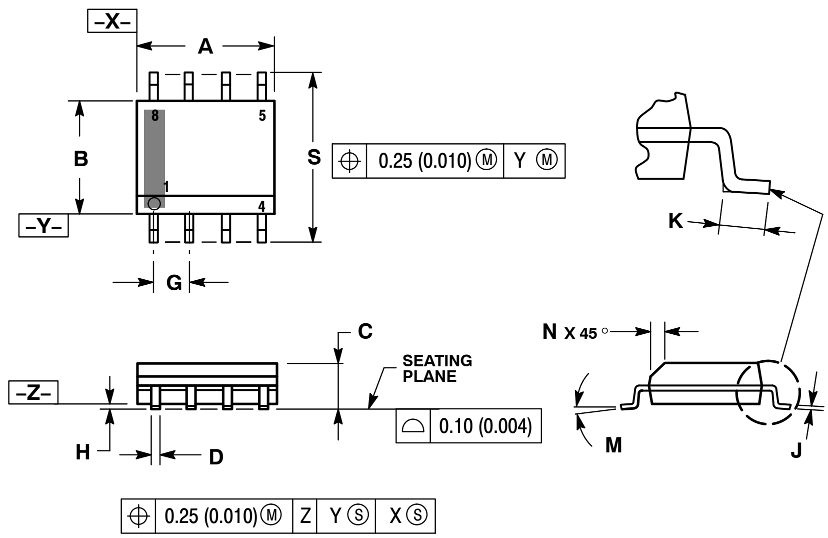
DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−23 (TO−236)**	**PAGE 1 OF 1**



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

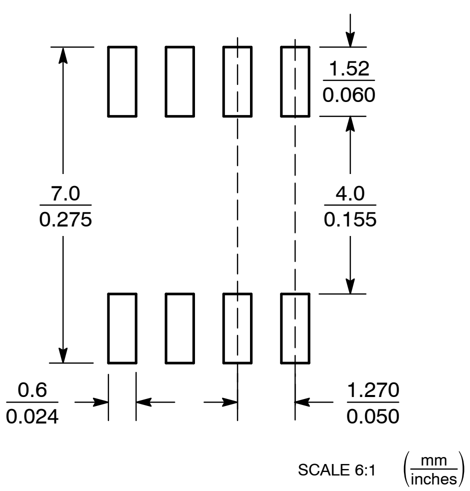
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

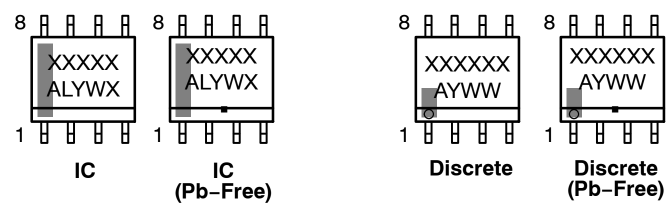
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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