ON Semiconductor®

SCY1751

10 W Charge Pump Converter with Bypass Mode

The SCY1751 integrated circuit is a 10 W charge pump converter that can automatically switch between a pass−through and a divide−by−2 mode of operation. It provides a narrowed 4 V to 12 V output voltage from a wide input voltage range of 4 V to 24 V. Together with the adjustable input overvoltage protection this allows supplying medium voltage devices from a varying higher voltage source such as a wireless charging interface. The charge pump can run on an internal or external clock while two devices can be put in parallel to increase the power capability. The input voltage, system current and die temperature are converted by an 8−bit ADC for full control by the host which can program or read out the device through the One−Wire / I^2C interface.

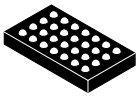
Features

- Wide Input Voltage Range from 4.0 V to 24 V
- Charge Pump Converter:
  - Pass−through Efficiency 99% at 8 V Input
  - Divide−by−2 Efficiency 96% at 12 V Input
  - Programmable Divide−by−2 Threshold
  - Minimum 2 A Output Current Capability
- Control
  - I^2C 400 kHz / 3.4 MHz Control Interface
  - OWI One Wire Interface (QUALCOMM®)
  - Communication Bus Selection with SEL Pin
- 8−bit ADC
  - Input Voltage Sensing
  - Remote Current Sensing
  - On−chip Temperature Monitor
- Charge Pump Clocking:
  - Internal Clock Generation
  - Synchronization to External Clock
  - Inverted Clock Output
- Low Dropout Regulator
- Over Voltage Detection with High Speed Gate Driver
- Open Drain Output for Charge ok Signaling
- Small Footprint
  - Package WLCSP28, 2.9x1.9 mm^2
  - 0.4 mm Pitch
- This is a Pb−Free Device

Typical Applications

- Wireless Charging Devices
- Tablets and Smartphones
- Portable Gaming Equipment

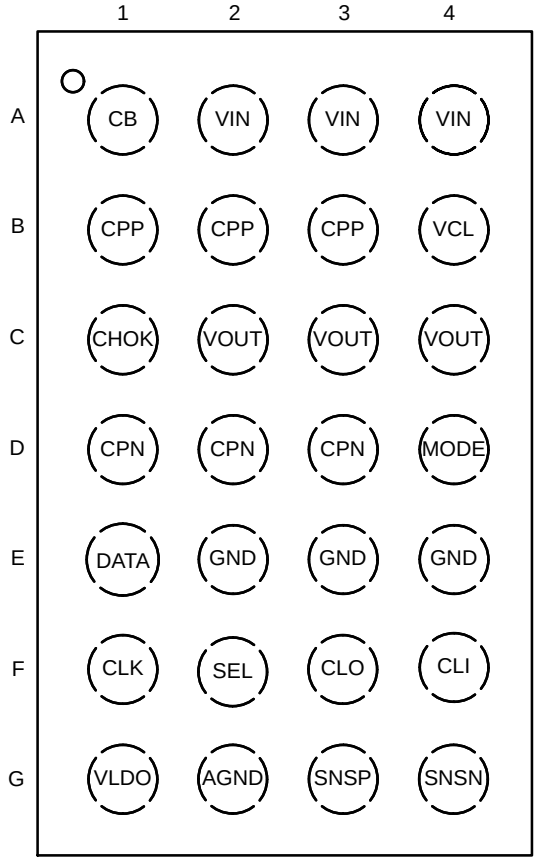
MARKING DIAGRAM



WLCSP28
CASE 567JJ

1751= Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 32 of this data sheet.

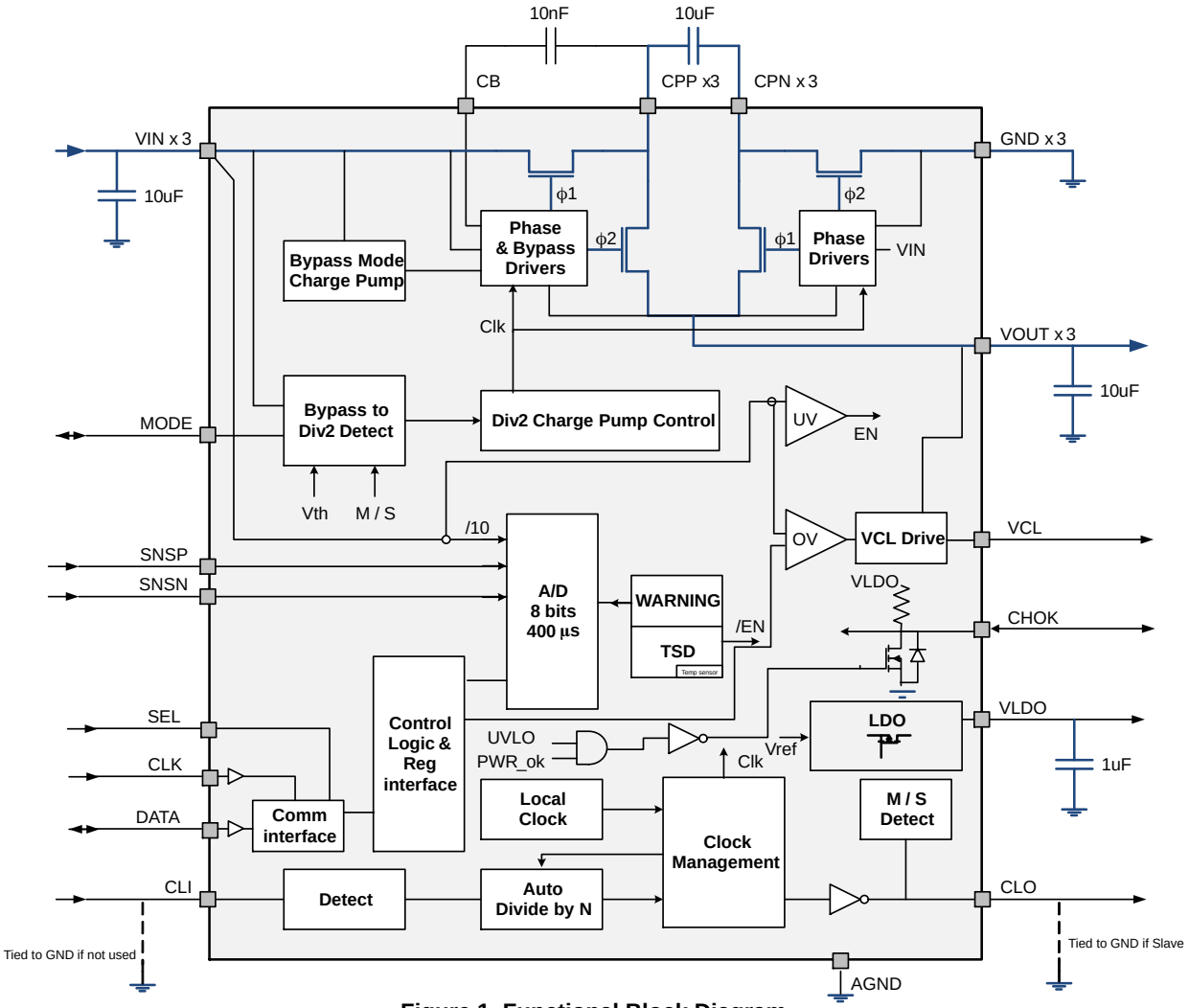


Figure 1. Functional Block Diagram

Table 1. PIN OUT DESCRIPTION

Pin	Name	Type	Description
POWER			
A2 A3 A4	VIN	Power Input	Positive Power Supply. These pins must be connected together. A 10μF low ESR ceramic capacitor must be connected between VIN and GND, and placed as close as possible to the device.
B1 B2 B3	CPP	Analog Input	Flying Capacitor Positive Node. These pins must be connected together. A 10μF low ESR ceramic capacitor must be connected between CPP and CPN, and placed as close as possible to the device.
D1 D2 D3	CPN	Analog Input	Flying Capacitor Negative Node. These pins must be connected together. A 10μF low ESR ceramic capacitor must be connected between CPP and CPN, and placed as close as possible to the device.
C2 C3 C4	VOUT	Power Output	Charge Pump Output. These pins must be connected together. A 10μF low ESR ceramic capacitor must be connected between VOUT and GND, and placed as close as possible to the device.
A1	CB	Analog Input	Bootstrap Capacitor Connection. A 10nF low ESR ceramic capacitor must be connected between CB and CPP, and placed as close as possible to the device.
E2 E3 E4	GND	Power Ground	Charge Pump Power Ground. These pins must be connected together. They carry the high switching currents and high quality ground must be provided to prevent noise spikes. A local ground plane is recommended.
CONTROL AND SERIAL INTERFACE			
F2	SEL	Digital Input	Bus Select. Connect SEL to GND for OWI communication bus selection. Connect SEL to VLDO for I^2C communication bus selection.
F1	CLK	Digital Input	Clock. OWI interface clock or I^2C interface clock.
E1	DATA	Digital I/O	DATA. OWI interface data line or I^2C data line.
OTHERS			
B4	VCL	Analog Output	Voltage Clamp. Open drain pull up. This pin is pulled up to VOUT if Vin voltage exceeds the overvoltage level and left floating when released.
C1	CHOK	Digital I/O	Charger OK Input/Output. When internally pulled high to VLDO it indicates charging is allowed and when externally forced low that charging has ended.
D4	MODE	Digital I/O	Mode Input/Output. Output signal in single tile or in master mode configuration, input signal in slave mode. Low level indicates pass through mode, high level divide−by−2 mode.
G2	AGND	Analog Ground	Analog Ground. Ground for analog core and digital modules. Must be connected to the system ground.
F3	CLO	Digital Output	Clock Ouput. This pin is the buffered output of the charge pump switching frequency. If grounded at start up the IC enters in slave mode.
F4	CLI	Digital Input	External Clock Input. An external clock can be applied here. The charge pump will synchronize to a divided by version of this clock. If not used connect to GND.
G1	VLDO	Power Output	Output of The Internal LDO. A 1 μF low ESR ceramic capacitor must be connected between VLDO and GND, and placed as close as possible to the device.
G4	SNSN	Analog Input	Negative Sense Input. Current sensing negative input to the ADC.
G3	SNSP	Analog Input	Positive Sense Input. Current sensing positive input to the ADC.

ELECTRICAL CHARACTERISTICS

Table 2. MAXIMUM RATING TABLE

Rating	Symbol	Value	Unit
Power pins (Group 1): VIN, CPP to GND	V_{IN}, V_{CPP}	−0.3 to + 26	V
Power pins (Group 2): CPN, VOUT	V_{OUT}, V_{CPN}	−0.3 to + 13	V
Boostrap pin to GND	V_{CB}	−0.3 to + 39	V
Clamp voltage pin to GND	V_{VCL}	−0.3 to +13	V
Charge OK pin to GND	V_{CHOK}	−0.3 to +VLDO	V
LDO voltage pin to GND	V_{VLDO}	−0.3 to +6.0	V
Mode pin to GND	V_{MODE}	−0.3 to VLDO	V
Sense pin positive to GND	V_{SENSP}	−0.3 to +2.5	V
Sense pin negative to GND	V_{SENSN}	−0.3 to +2.5	V
Digital pins: CLK, DATA, CLI, CLO to GND Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to VLDO 10	 V mA
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 1)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage		4.0	−	24	V
V_{OUT}	Output voltage		4.0	−	12	V
V_{VCL}	Clamping voltage		−	−	VOUT	V
V_{SENSP}	Positive sense of input current		−	0	−	V
V_{SENSN}	Negative sense of input current		−0.1	−	−	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 4)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		−	40	−	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case		−	10	−	°C/W
C_{CB}	Output Capacitors for V_{CB}		10	−	−	nF
Cvin	Input Capacitor		10	−	−	μF
Cfly	Flying capacitor		10	−	−	μF
Cvout	Output capacitor		10	−	−	μF
Cvldo	Low dropout output capacitor		1	−	−	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
3. Refer to the Application Information section of this data sheet for more details.
4. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
5. The $R_{\theta CA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2” x 2” NCPXXXEVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
6. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$P_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC} \text{ with } \left(R_{\theta JA} = R_{\theta JC} + R_{\theta CA}\right)$$

Table 4. ELECTRICAL CHARACTERISTICS
Min & Max Limits apply for T_A from 0°C to 85°C and T_J up to +125°C unless otherwise specified. V_{IN} = 10 V (Unless otherwise noted). VLDO = 2.5 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS VIN						
I_{STBY}	Product standby mode current	Vin < $V_{UVLO\ -\ hyst}$ and VLDO off	−	30	−	μA
I_Q	Operating quiescent current	V_{IN} = 5 V, pass through	−	1.2	2	mA
		V_{IN} = 10 V, Div2	−	5.4	10	mA
POWER STAGE						
V_{IN}	Input Voltage Range		4.0	−	24	V
I_{OUTMAX}	Maximum Output Current		2	−	−	A
V_{OUT}	Output Voltage Range		4.0	−	12	V
Vth	Change mode threshold	Vin rising (Note 10)	−	9.8	−	V
	Vth programmable range	100 mV steps	9.5	−	11	V
	Change mode threshold hysteresis	Vin falling	50	100	150	mV
	Accuracy		−1.5	−	1.5	%
V_{OUTMAX}	Max Vout voltage	During change mode transition, Vin rising 12 mV/μs, Vth = 9.8 V, (Note 8)	−	−	10	V
V_{UVLO}	Undervoltage comparator	Vin rising	3.8	−	4.0	V
	Undervoltage comparator hysteresis	Vin falling	50	100	150	mV
Ron	Pass through resistance	V_{IN} to V_{OUT}, T_J = 85°C	−	55	130	mΩ
Peff	Power efficiency	V_{IN} = 8 V, Pin= 5 W, T_J = 85°C	−	99	−	%
		V_{IN} = 10 V, Pin= 5 W, T_J = 85°C	−	95	−	
		V_{IN} = 12 V, Pin= 5 W, T_J = 85°C	−	96	−	
Fint	Internal Switching frequency		−	860	−	kHz
	Accuracy		−10	−	10	%
I_{STUP}	Start up inrush current	UVLO crossing	−	100	−	mA
LDO						
V_{LDO}	LDO voltage	Default value (Note 10) SCY1751FCCT1G	−	2.5	−	V
	LDO programmable range	Default value (Note 10) SCY1751FCCAT1G	−	1.8	−	V
V_{UVLDO}	VLDO turn off comparator	Vin falling edge.	−	3	−	V
PSRR	Ripple rejection	At 1 kHz, 100 mV peak peak. 1 mA load	−	−60	−	dB
Iout	Current capability		30	−	−	mA
Iclamp	Clamp threshold	V_{IN} = 10 V, 25°C	50	70	90	mA
Ifldb	Foldback current	VLDO shorted to GND	−	14	−	mA
$VLDO_R$	LDO output rise time	90% VLDO, I load = 1 mA, (Note 9)	−	−	100	μs
VCL						
Voh_{VCL}	Clamp voltage	V_{IN} > $V_{VCL,}$ I sink 5 mA	Vout – 0.3	−	Vout	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
8. Guaranteed by design and functional production test.
9. Guaranteed by design and characterization.
10. Please contact your ON Semiconductor representative for additional option and version (default values).

Table 4. ELECTRICAL CHARACTERISTICS
Min & Max Limits apply for T_A from 0°C to 85°C and T_J up to +125°C unless otherwise specified. V_{IN} = 10 V (Unless otherwise noted). VLDO = 2.5 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCL						
V_{VCL}	Clamp threshold	Vin rising (Note 10)	−	22.9	−	V
	Threshold range	Programmable	19.4	−	22.9	V
	Clamp accuracy		−1.8	−	1.8	%
	Digital alarm		−	2.5	−	μs
$V_{VCL\ REARM}$	Clamp rearming threshold	Vin falling	7	−	7.3	V
Toff	VCL response time	From V_{IN} > Vvcl to VCL = 4.5 V. 0.3 V/100 ns Vin rising edge 2 nF load. (Note 8)	−	250	500	ns
MODE						
Vil		Slave mode	−	−	0.6	V
Vih		Slave mode	1.2	−	VLDO	V
Vol		Master mode. Sink − 500 μA	−	−	0.4	V
Voh		Master mode. Sink 1 mA	VLDO – 0.3	−	VLDO	V
CHGOK						
Voh	Charge status		VLDO −0.3	−	VLDO	V
Vol		Sink −2 mA	−	−	0.4	V
$CHOK_C$	High impedance state capacitance	(Note 9)	−	−	30	pF
Rpu	Pull up resistor		−	10	−	kΩ
Vil			−	−	0.4	V
Vih			1.2	−	VLDO	V
CLI						
Fext	External clock frequency		0.5	−	20	MHz
Vil	Low threshold		−	−	0.6	V
Vih	High threshold		1.2	−	VLDO	V
CLI_{STB}	Standby input leakage	V_{IN} = 0 V	−	−	1	μA
CLO						
Vol	CLO low		0	−	0.4	V
Voh	CLO high	Connected on CLI, slave mode	VLDO – 0.3	−	VLDO	V
CLO_{det}	GND detection		−	150	−	μA
V_{SL}	Slave mode detection threshold		−	−	0.4	V
V_M	Master mode detection threshold		1.2	−	VLDO	V
CLK, DATA						
CLK_{Vil}, $DATA_{Vil}$	Low Threshold		−	−	0.5	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CLK, DATA						
V_{I2C}	Voltage rail at CLK/DATA lines		1.7	−	5.5	V
CLK_{Vih}, $DATA_{Vih}$	High Threshold	Cf I^2C interface description	0.8 x V_{I2C}	−	V_{I2C}	V
CLK_{Vol}, $DATA_{Vol}$	Low output voltage	I_{SINK} = −3 mA	0	−	0.4	V
CLK_{leak}, $DATA_{leak}$	Off state leakage current	V_{IN} = 0 V	−	−	2	μA
CLK_Z, $DATA_Z$	High impedance state capacitance	(Note 9)	−	−	30	pF
F_{I2C}	I^2C clock frequency		−	−	3.4	MHz
F_{OWI}	OWI reference clock	CLK	−	32.768	−	kHz
	OWI reference clock required accuracy	(Note 9)	−10	−	+10	%
F_{DATA}	OWI bit rate	Referred to CLK (F_{OWI} x 225/64)	−	115.2	−	kbps
	OWI bit rate Accuracy	Transmit, referred to CLK	−2	−	2	%
SEL						
Vil	Low Threshold		−	−	0.5	V
Vih	High threshold		1.2	−	VLDO	V
ADC						
	Bias current	During conversion	−	1	−	mA
	Reference voltage		−	2.4	−	V
	Input range	From 0 to full scale	0	−	2.3906	V
	Total bit number		−	8	−	bits
	Total conversion time	All channels	−	420	−	μs
	Single Channel conversion time		−	100	−	μs
	Absolute Gain error		−	−	1	%
	Absolute Offset error		−	−	1	LSB
ADC INPUT STAGE						
	Output filter attenuation	At Fsw	−	30	−	dB
THERMAL BLOCK						
T_{SD}	Thermal Shut Down Protection		−	150	−	°C
$T_{WARNING}$	Warning Rising Edge	Alarm on register	−	135	−	°C
T_{SDR}	Thermal Shut Down Rearming		−	110	−	°C

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9. Guaranteed by design and characterization.
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DETAILED DESCRIPTION

The SCY1751 integrated circuit is a 10W charge pump converter that can automatically switch between a pass−through and a divide−by−2 mode of operation. It provides a narrowed 4 V to 12 V output voltage from a wide input voltage range of 4 V to 24 V. Together with the adjustable input overvoltage protection this allows supplying medium voltage devices from a varying higher voltage source such as a wireless charging interface. The charge pump can run on an internal or external clock while two devices can be put in parallel to increase the power capability. The input voltage, system current and die temperature are converted by an 8−bit ADC for full control by the host which can program or read out the device through the One−Wire / I^2C interface.

Enabling and Under Voltage Lockout

When upon application of power to Vin the input voltage exceeds the V_{UVLO} threshold, the SCY1751 will automatically be enabled and the regulator VLDO turned on. When the input voltage drops below the under voltage lockout (UVLO) threshold minus a hysteresis, all internal circuitry except the VLDO are disabled and the I^2C and OWI registers reset to their default values. The VLDO is turned off when Vin drops below V_{UVLDO}.

Charge Pump Functionality

The converter can operate in three modes: pass−through, wait state and divide−by−2 or x0.5 mode.

Upon application of a valid voltage at Vin the part enters pass−through mode, charges the output capacitors up to the Vin level and fully turns on the power switches between VIN and VOUT. As long as Vin does not reach Vth, the part stays in this pass−through mode, keeps the MODE pin low and maintains the clock output CLO off.

When Vin exceeds the Vth threshold, the charge pump transitions into wait state where the power switches are opened. As a result the load at the output will discharge the output capacitor and the voltage will drop. The MODE pin is driven high in this mode, but CLO stays off. When the output voltage Vout reaches the Vin/2 level, the charge pump is enabled and the part enters the divided−by−2 mode. The MODE pin is maintained high while CLO is now actively driven.

Table 5. VTH THRESHOLD TABLE

Vth (V)	Vth [3:0]	Vth (V)	Vth [3:0]
9.5	0000	9.9	0100
9.6	0001	10	0101
9.7	0010	10.1	0110
9.8	**0011**	10.2	0111
10.3	1000	10.7	1100
10.4	1001	10.8	1101
10.5	1010	10.9	1110
10.6	1011	11	1111

In the divide−by−2 mode two pairs of identical MOSFET output stages run in opposite phase and at a 50% duty cycle. During phase 1 the flying capacitor connected between CPP and CPN and the output capacitor at VOUT are switched in series while during phase 2 they are switched in parallel. By alternating these two phases rapidly, the output voltage of the charge pump will establish itself at half the input voltage. The charge pump can operate from both an internal or external clock, see clocking section.

An external bootstrap capacitor, connected between CB and CPP, is used to provide sufficient drive voltage for the input NMOS power switch.

An overvoltage condition is detected when Vin exceeds V_{VCL}. The IC stays in the divide−by−2 mode while the VCL pin is rapidly pulled up to Vout in order to drive the gate of an external FET. The latter will interact with the wireless charging application to decrease the Vin voltage to safe levels.

Table 6. VCL THRESHOLD TABLE

VCL (V)	Vcl [2:0]	VCL (V)	Vcl [2:0]
19.4	000	21.4	100
19.9	001	21.9	101
20.4	010	22.4	110
20.9	011	22.9	111

Flying Capacitor and Output Capacitor

The choice of flying and bypass capacitors is essential in obtaining a good efficiency of the charge pump. It is to be noted that the significant voltage drop over the capacitors reduce the effective capacitance of the capacitors compared to its value at a 0V bias voltage. The larger the capacitor physical size the lesser this effect will be noticeable.

Charge and Power OK Communication

The CHOK pin and its related control and sense bits allow the host to communicate through the SCY1751 with the system PMIC about the state of charge.

The CHOK pin is internally pulled high if all 3 below conditions are fulfilled:

- Vin > UVLO (input voltage high enough for charging)
- PWR_ok bit is set high (controller allows charging)
- CHOK pin is not externally forced low by the PMIC (supply is requested)

The CHOK pin is low for any of the following conditions:

- Vin < UVLO (input voltage too low for charging)
- PWR_ok bit is cleared (controls blocks charging)
- CHOK pin is externally pulled low by the PMIC (supply is not requested)

The state of the CHOK pin is monitored and reflect by the sense bit CHOK_S. For instance, if CHOK_S=0 while PWR_ok=1, this can be interpreted as the charging of the battery being completed.

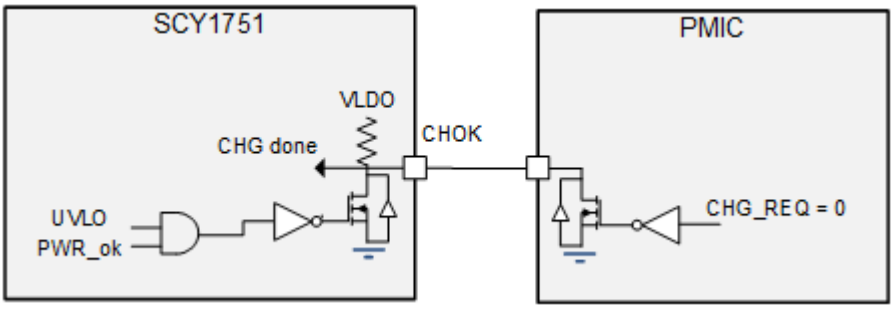


Figure 2. CHOK Pin

Tiling Configuration

In some applications, more power is required than a single SCY1751 can handle. To be able to increase the amount of power, SCY1751 parts can be placed in parallel, also referred to as Tiling. To avoid conflicts between Tiles, a single device should make the decision for pass−through or divide−by−2 operating modes. The SCY1751 can therefore be configured as a Master (CLO floating or capacitively loaded) or as a Slave (CLO tied to ground). The CLO condition is verified at power up. Note that Master mode is the standard operating mode for the SCY1751.

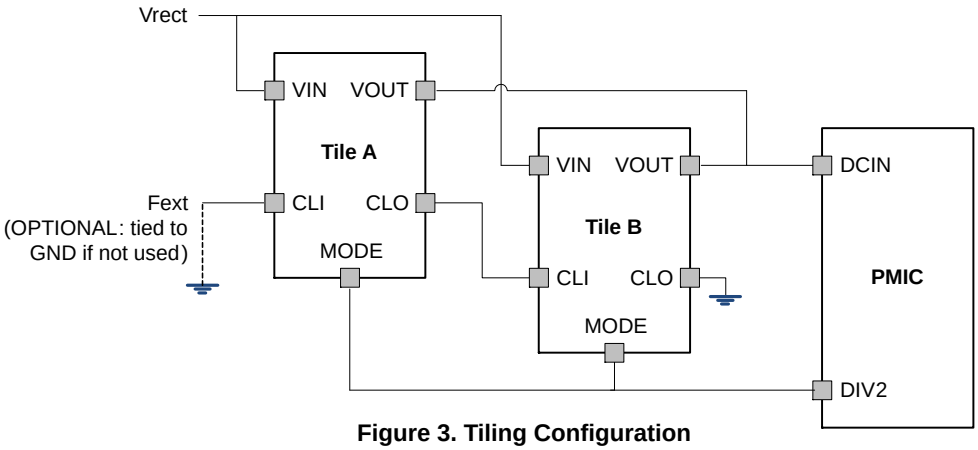


Figure 3. Tiling Configuration

The SCY1751 configured as a Master (Tile A in above diagram) will have its MODE pin configured as an output. The MODE pin reflects the status of the operating mode. If the input voltage Vin is below Vth, the MODE pin is forced low (pass−through mode), in divide−by−2 mode it is driven high. When Vin drops below Vth, the MODE pin is forced low while the charge pump will not immediately enter the divide−by−2 mode. A debounce is applied between comparator detection and the actual mode transition to give time to the system to anticipate this change. This debounce is programmable through OWI or I^2C (Div_2_delay).

The SCY1751 configured as a Slave (Tile B in above diagram) will have its MODE pin configured as an input. Based on the MODE signal the Slave will be forced into pass−through or divide−by−2 mode. The synchronization of the charge pump activity of the two Tiles is achieved by connecting the CLO output of the Master to the CLI input of the Slave.

Table 7. Div_2_delay TABLE

Div_2_delay	Delay (μs)
000	75
001	150 (default)
010	300
011	600
100	1200
101	2400
110	4800
111	0

NOTE: Please contact your ON representative for additional option and version (default value).

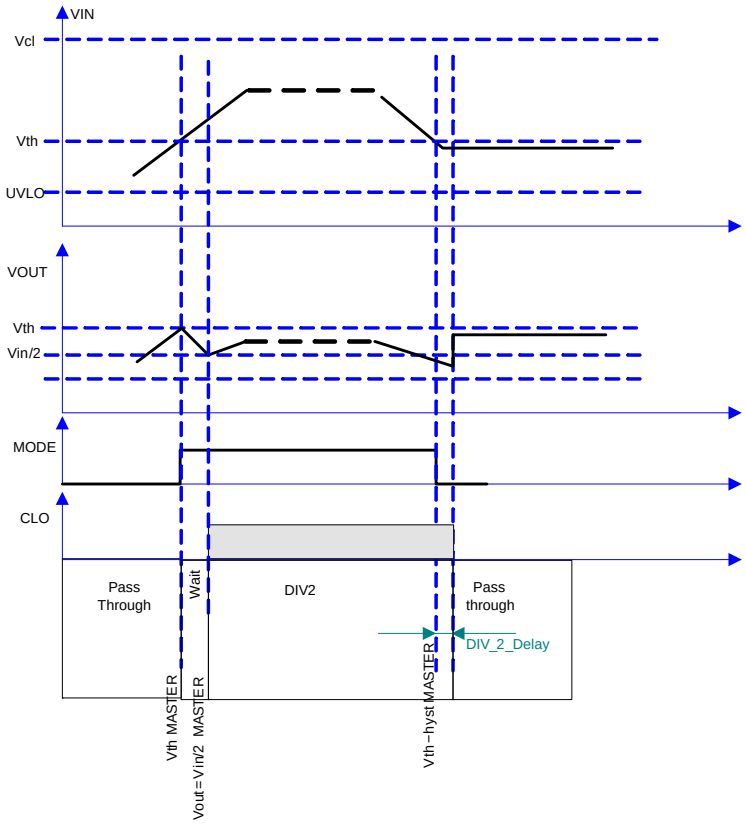


Figure 4. MODE/CLO Behavior, DIV 2 / Pass Through

Clocking and External Clock

The charge pump of the SCY1751 can run on either the internal clock Fint or on an external clock applied to CLI. For an external clock to be detected, it has to be greater than Fint/2. Up to 2*Fint the clock will be used directly by the charge pump. When exceeding this range the clock will be automatically divided by N so that the charge pump continues operating in its target range. The divider ratio N is even and limited to 28 so that, independent on the CLI duty cycle, the charge pump will run on a clock at a 50/50 duty cycle. The actual charge pump clock (from internal or CLI) can be routed out in opposite phase to CLO to drive the slave tile. This ensures both tiles always run at the same frequency and out of phase which reduces overall ripple.

Important note: If no external clock is used in the application, the CLI pin has to be grounded to avoid erratic behavior.

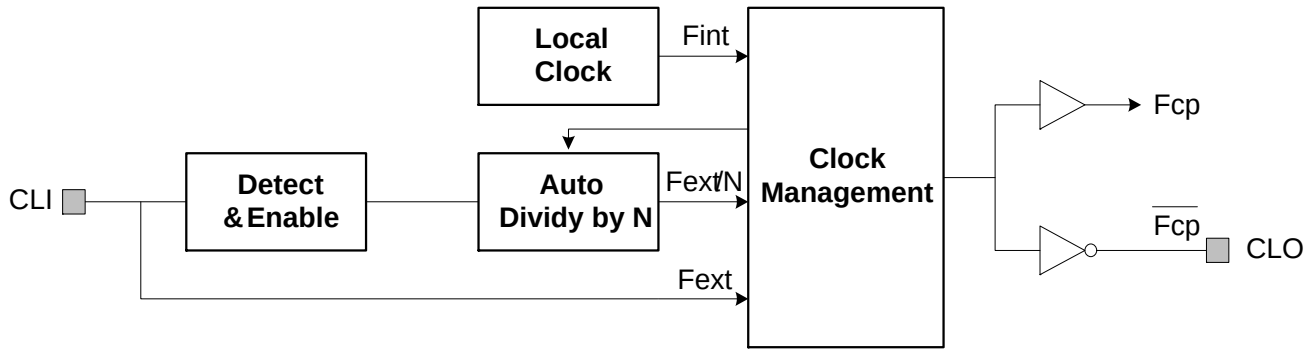


Figure 5. CLI/CLO Schematic

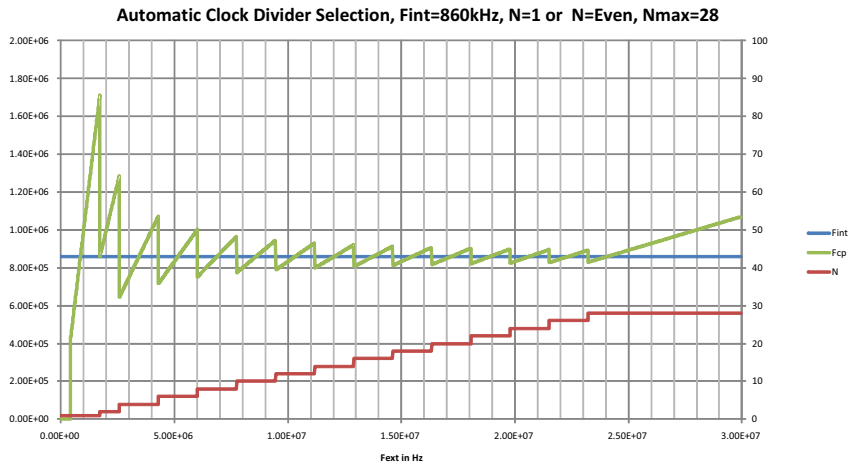


Figure 6. Clock Divider Selection

For proper operation, in particular in the Tiling configuration, the frequency of the external clock should not be changed on the fly. The clock should first be disabled for a minimum of 5 periods of the internal clock before being re−applied at the new frequency.

Table 8. N_CLI TABLE

N_CLI [3:0]				N
0	0	0	0	No external clock
0	0	0	1	External clock detected N = 1
0	0	1	0	2
0	0	1	1	4
0	1	0	0	6
0	1	0	1	8
0	1	1	0	10
0	1	1	1	12
1	0	0	0	14
1	0	0	1	16
1	0	1	0	18
1	0	1	1	20
1	1	0	0	22
1	1	0	1	24
1	1	1	0	26
1	1	1	1	28

Thermal Shutdown

Given the output power capabilities of the on chip charge pump converter, the thermal capabilities of the device can be exceeded. A thermal protection circuit is therefore implemented to prevent the part from damage (TSD). This protection circuit is only active when the core is in active mode (Vin > UVLO). In addition to the TSD, a thermal warning is implemented which informs the processor through an interrupt bit and a status bit (latched on an interrupt and cleared only if the event disappears and interrupt bit is reset) that the device is close to TSD so that preventive action can be taken through software, such as reducing the load current. The die temperature can be read out through the ADC.

In case of a TSD event, the power MOSFETs are all made non−conducting, the VLDO remains enabled and a thermal shutdown interrupt is generated. The input supply at VIN should be reduced to below the UVLO threshold to force a complete reset.

The TSD behavior is different between Master and Slave. If the Slave encounters a TSD event, the master is not informed. At the same time, the Master now has to provide twice the power and will quickly hit the TSD threshold. This will eventually lead to a full system reset. If the Master encounters a TSD event, it will continue to correctly control the Slave, that is to say, MODE continues to indicate the proper operating mode while CLO will only be disabled after the Div_2_delay.

The below diagram depicts above described behavior.

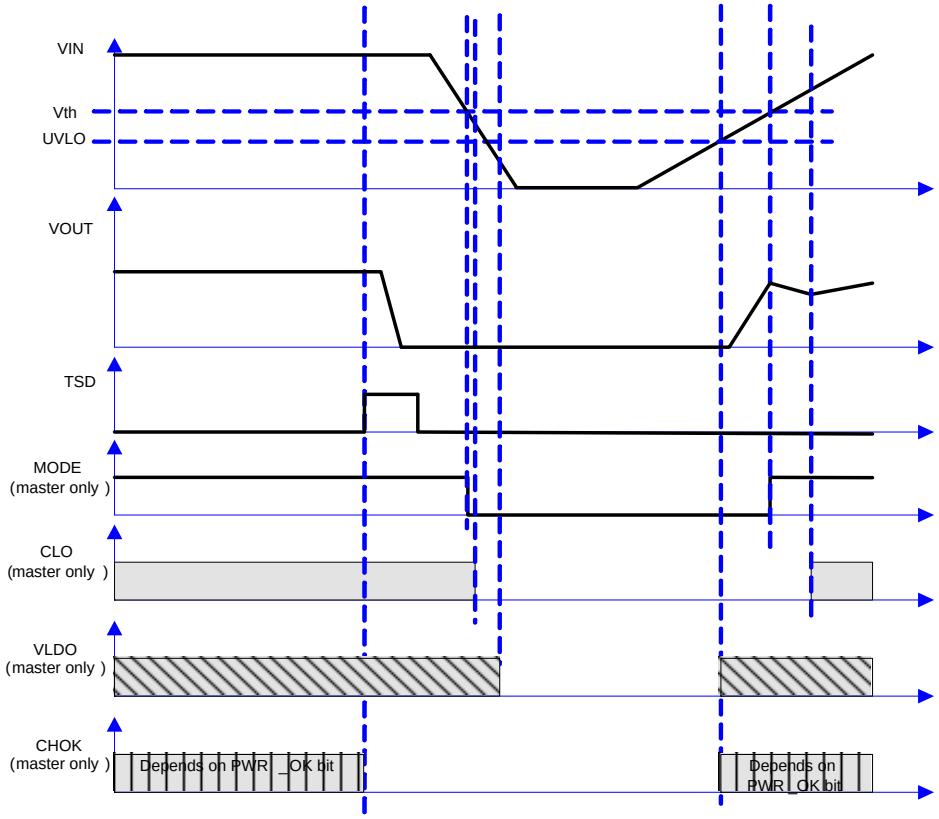


Figure 7. MODE/CLO Behavior on a TSD Event

ADC

The A to D converter is based on a differential 10 bit switched capacitor core. It is supplied from the core voltage and uses an on−chip reference Vref. The 8 most significant bits can be consulted through both the I^2C or OWI bus interfaces.

The ADC converts the input voltage at VIN, the remote differential current as sensed between SNSP and SNSN, and the die temperature. The latter provides close die temperature monitoring on top of the thermal warning and shutdown. Each signal is first scaled by the A to D converter in order to adapt it to its input range. When, despite the scaling, the input range is exceeded, the read out is clamped in either direction.

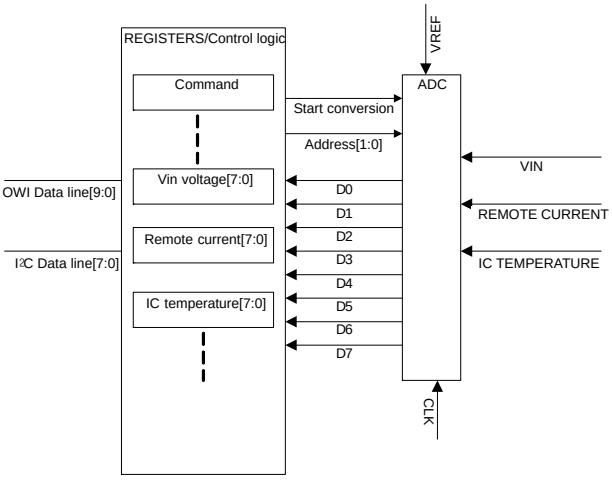


Figure 8. ADC diagram

Table 9. ADC INPUT CHANNELS

Channel	Pin	Input Min	Input Max	Scaling	Full Range Ref	LSB	LSB Value
Input voltage	Internal On the Vin ball.	0 V	24 V	/10	2.4 V − 1 LSB = 2.4 V − 0.009375 = 2.390625	2.4/256	93.75 mV
External input current	SNSP, SNSN. Differential.	−120 mV	0	x 20	2.4 V − 1 LSB = 2.4 V − 0.009375 = 2.390625	2.4/256	13 mA 26 mA
Internal temperature	Internal temperature	−40 (IC rating)	150°C (IC rating)	1	2.4 V − 1 LSB = 2.4 V − 0.009375 = 2.390625	2.4/256	−1.5°C

Input Voltage Conversion

Before conversion, the input voltage at VIN is scaled down by a factor of 10 in order to fit the input range of the ADC. Below the figure provide relationship between the input voltage and the converted voltage.

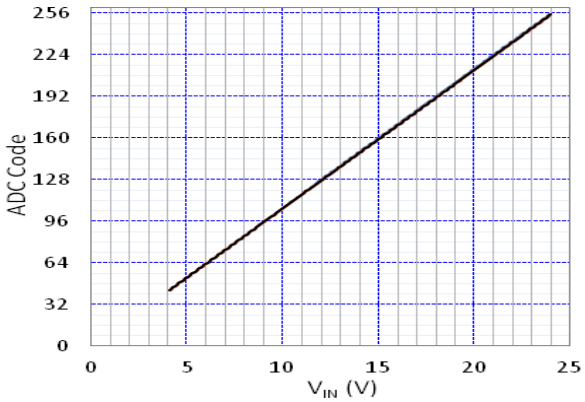


Figure 9. Vin ADC Conversion

Table 10. VOLTAGE CONVERSION

LSB Value (V)	Vin (V)	Dec	Hex	Bin
0.09375	0	0	0	0
0.09375	1	11	A	1010
0.09375	2	21	15	10101
0.09375	3	32	20	100000
0.09375	4	43	2A	101010
0.09375	5	53	35	110101
0.09375	6	64	40	1000000
0.09375	7	75	4A	1001010
0.09375	8	85	55	1010101
0.09375	9	96	60	1100000
0.09375	10	107	6A	1101010
0.09375	11	117	75	1110101
0.09375	12	128	80	10000000
0.09375	13	139	8A	10001010
0.09375	14	149	95	10010101
0.09375	15	160	A0	10100000
0.09375	16	171	AA	10101010
0.09375	17	181	B5	10110101
0.09375	18	192	C0	11000000
0.09375	19	203	CA	11001010
0.09375	20	213	D5	11010101
0.09375	21	224	E0	11100000
0.09375	22	235	EA	11101010
0.09375	23	245	F5	11110101
0.09375	23.8	254	FD	11111101
0.09375	23.91	255	FF	11111111

Voltage Conversion

$$\text{Vin(V)} = \left(\text{ADC value} \cdot \frac{2.4}{256}\right) \cdot 10 \qquad \text{(eq. 1)}$$

Input Current Conversion

The input current is measured as a voltage drop over a low ohmic sense resistor connected between SNSP and SNSN. Before conversion, the voltage over the sense resistor amplified in order to fit the input range of the ADC. The value of the sense resistor is to be selected as function of the maximum current to be measured. Below table provides the results of the conversion for two different resistor choices.

Table 11. CURRENT CONVERSION

				36 mΩ				18 mΩ			
LSB/V	LSB/I 18 mΩ	LSB/I 36 mΩ	Current	Drop	AtD Dec Conv	AtD Hex Conv	AtD Bin Conv	Drop	AtD Dec Conv	AtD Hex Conv	AtD Bin Conv
0.0004688	0.026041667	0.013020833	0	0.0000	0	0	0	0.0000	0	0	0
0.0004688	0.026041667	0.013020833	0.2	0.0072	15	F	1111	0.0036	8	7	111
0.0004688	0.026041667	0.013020833	0.4	0.0144	31	1E	11110	0.0072	15	F	1111
0.0004688	0.026041667	0.013020833	0.6	0.0216	46	2E	101110	0.0108	23	17	10111
0.0004688	0.026041667	0.013020833	0.8	0.0288	61	3D	111101	0.0144	31	1E	11110
0.0004688	0.026041667	0.013020833	1	0.0360	77	4C	1001100	0.0180	38	26	100110
0.0004688	0.026041667	0.013020833	1.2	0.0432	92	5C	1011100	0.0216	46	2E	101110
0.0004688	0.026041667	0.013020833	1.4	0.0504	108	6B	1101011	0.0252	54	35	110101
0.0004688	0.026041667	0.013020833	1.6	0.0576	123	7A	1111010	0.0288	61	3D	111101
0.0004688	0.026041667	0.013020833	1.8	0.0648	138	8A	10001010	0.0324	69	45	1000101
0.0004688	0.026041667	0.013020833	2	0.0720	154	99	10011001	0.0360	77	4C	1001100
0.0004688	0.026041667	0.013020833	2.2	0.0792	169	A8	10101000	0.0396	84	54	1010100
0.0004688	0.026041667	0.013020833	2.4	0.0864	184	B8	10111000	0.0432	92	5C	1011100
0.0004688	0.026041667	0.013020833	2.6	0.0936	200	C7	11000111	0.0468	100	63	1100011
0.0004688	0.026041667	0.013020833	2.8	0.1008	215	D7	11010111	0.0504	108	6B	1101011
0.0004688	0.026041667	0.013020833	3	0.1080	230	E6	11100110	0.0540	115	73	1110011
0.0004688	0.026041667	0.013020833	3.2	0.1152	246	F5	11110101	0.0576	123	7A	1111010
0.0004688	0.026041667	0.013020833	3.4	Full Range	255	FF	11111111	0.0612	131	82	10000010
0.0004688	0.026041667	0.013020833	3.6		255	FF	11111111	0.0648	138	8A	10001010
0.0004688	0.026041667	0.013020833	3.8		255	FF	11111111	0.0684	146	91	10010001
0.0004688	0.026041667	0.013020833	4		255	FF	11111111	0.0720	154	99	10011001
0.0004688	0.026041667	0.013020833	4.2		255	FF	11111111	0.0756	161	A1	10100001
0.0004688	0.026041667	0.013020833	4.4		255	FF	11111111	0.0792	169	A8	10101000
0.0004688	0.026041667	0.013020833	4.6		255	FF	11111111	0.0828	177	B0	10110000
0.0004688	0.026041667	0.013020833	4.8		255	FF	11111111	0.0864	184	B8	10111000
0.0004688	0.026041667	0.013020833	5		255	FF	11111111	0.0900	192	C0	11000000
0.0004688	0.026041667	0.013020833	5.2		255	FF	11111111	0.0936	200	C7	11000111
0.0004688	0.026041667	0.013020833	5.4		255	FF	11111111	0.0972	207	CF	11001111
0.0004688	0.026041667	0.013020833	5.6		255	FF	11111111	0.1008	215	D7	11010111
0.0004688	0.026041667	0.013020833	5.8		255	FF	11111111	0.1044	223	DE	11011110
0.0004688	0.026041667	0.013020833	6		255	FF	11111111	0.1080	230	E6	11100110
0.0004688	0.026041667	0.013020833	6.2		255	FF	11111111	0.1116	238	EE	11101110
0.0004688	0.026041667	0.013020833	6.4		255	FF	11111111	0.1152	246	F5	11110101
0.0004688	0.026041667	0.013020833	6.6		255	FF	11111111	0.1188	253	FD	11111101
0.0004688	0.026041667	0.013020833	6.8		255	FF	11111111	Full Range	255	FF	11111111

Remote current 36 mΩ (mA) = 13x ADC code (eq. 2)

Remote current 18 mΩ (mA) = 26x ADC code

Internal Temperature Conversion

The temperature of the IC is measured by means of a voltage drop over a series of diodes. Below figure and formula provide the relationship between the converted voltage and the die temperature.

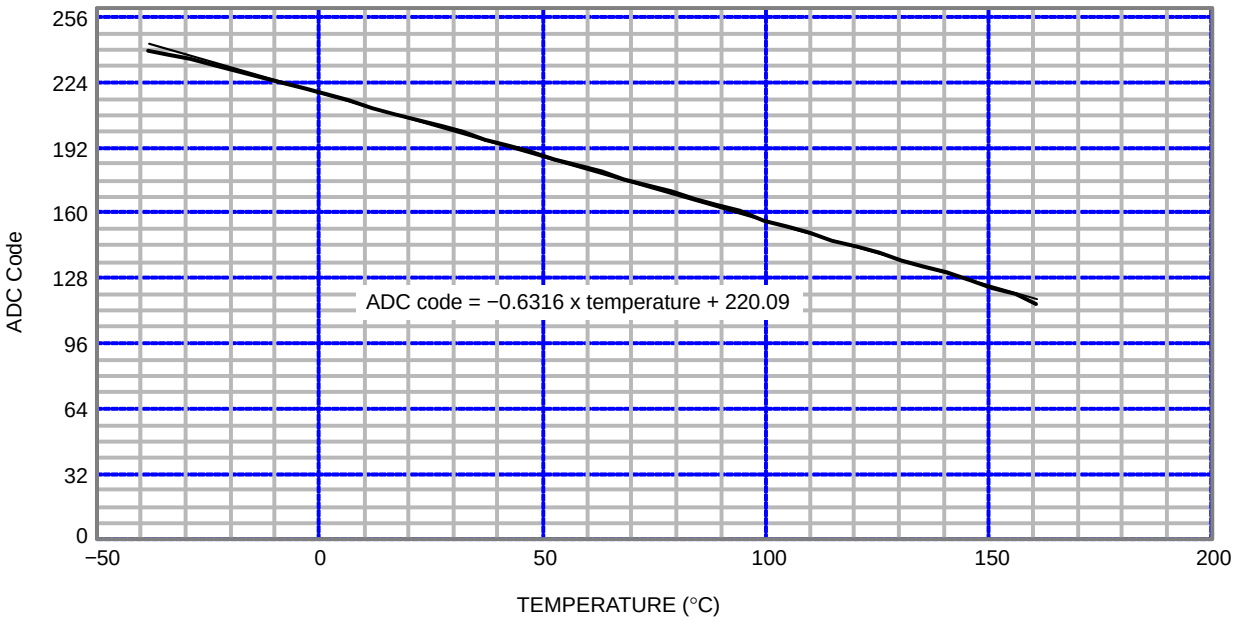


Figure 10. Temperature Conversion

The ADC conversions are done upon OWI request as depicted in below diagrams. For I^2C operation the ADC will be placed in an automatic conversion mode at programmable repetition rate or manual conversion.

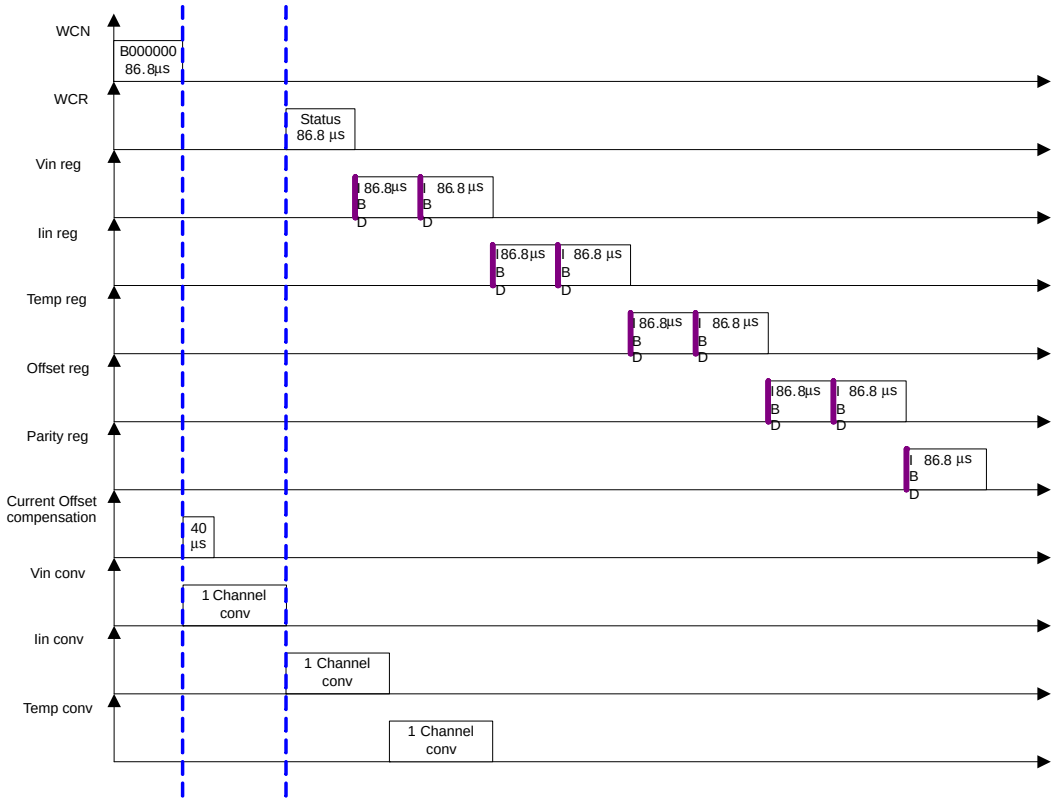


Figure 11. ADC Conversion Sequence, OWI Communication Interface: WCN Command Cmd$0

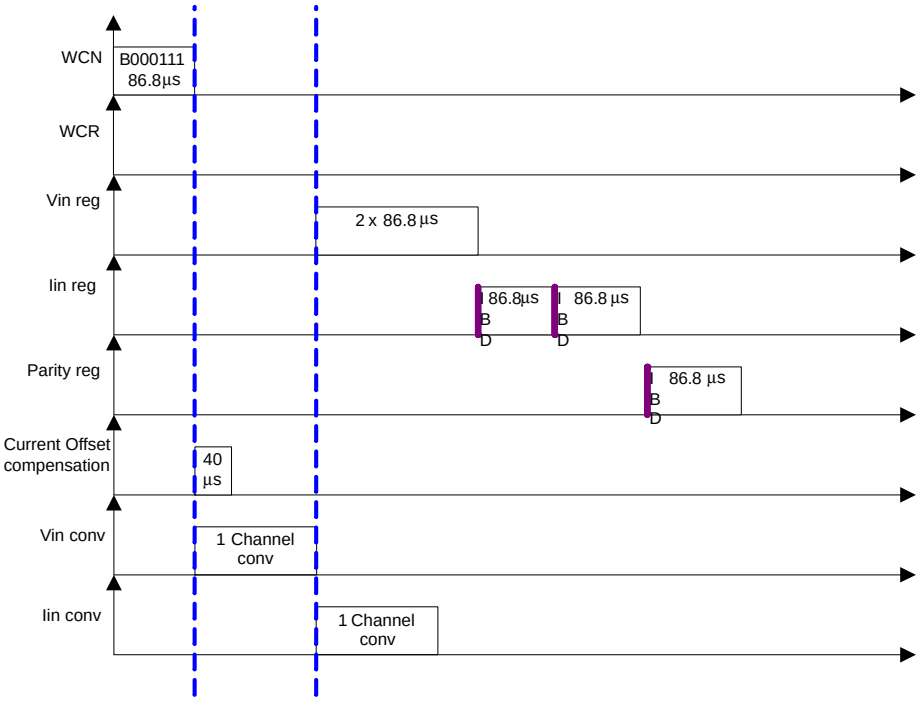


Figure 12. ADC Conversion Sequence, OWI Communication Interface: WCN Command Cmd$7

ELECTRICAL CURVES

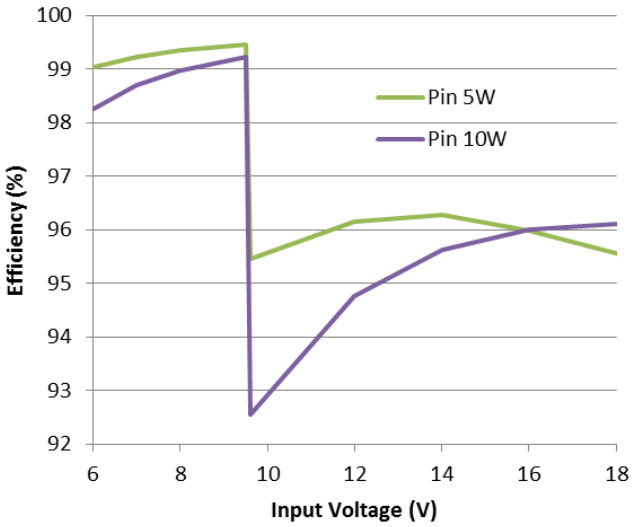


Figure 13. SCY1751 Efficiency vs. Vin

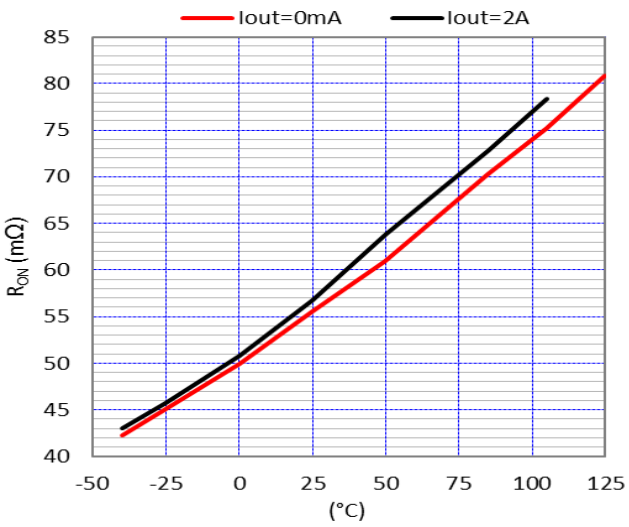


Figure 14. Pass Through Resistance vs. Temperature, Vin = 5 V

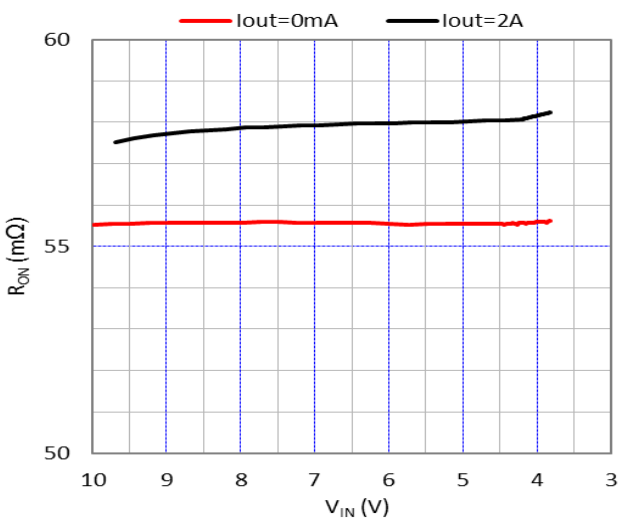


Figure 15. Pass Through Resistance vs. Vin. Ambient Temperature

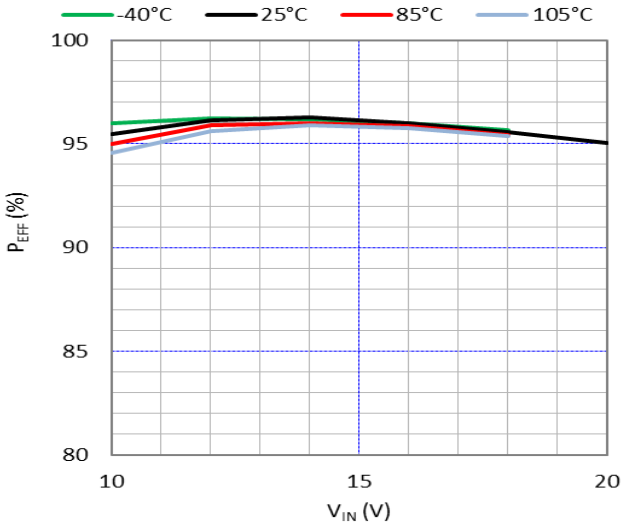


Figure 16. DIV2 Mode: Efficiency vs. Vin, Pin 5W, Over Temperature

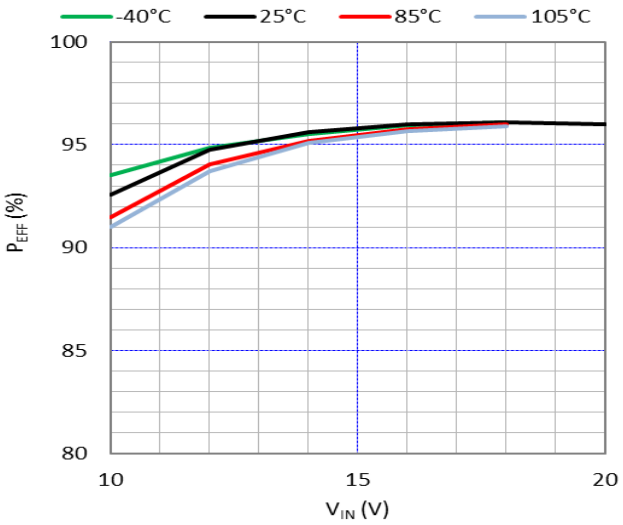


Figure 17. DIV2 Mode: Efficiency vs. Vin, Pin 10W, Over Temperature

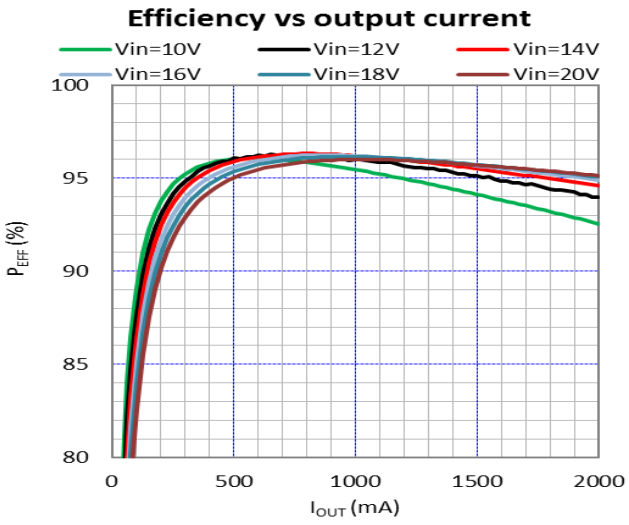


Figure 18. DIV2 Mode: Efficiency vs. Iout, Over Vin, Room Temperature

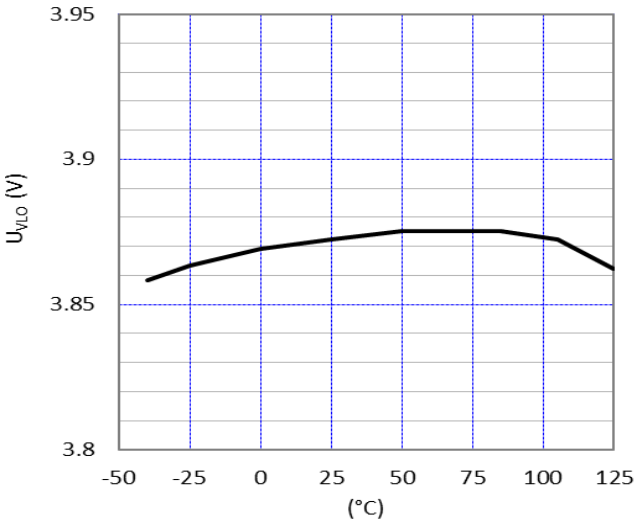


Figure 19. UVLO Threshold, vs. Temperature (Vin rising)

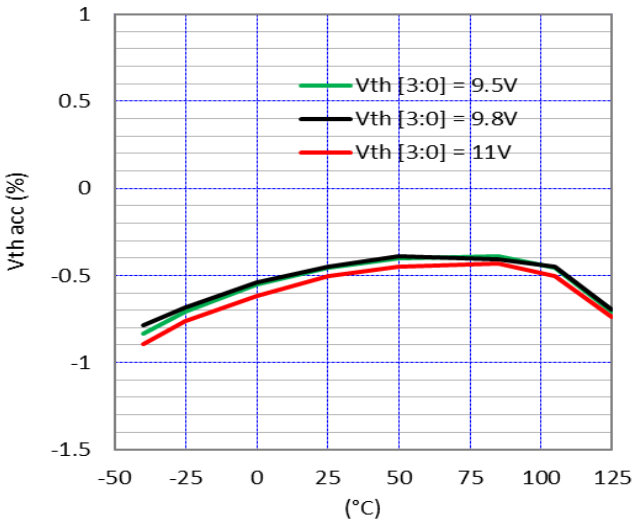


Figure 20. VTH Threshold Accuracy vs. Temperature (Vin rising)

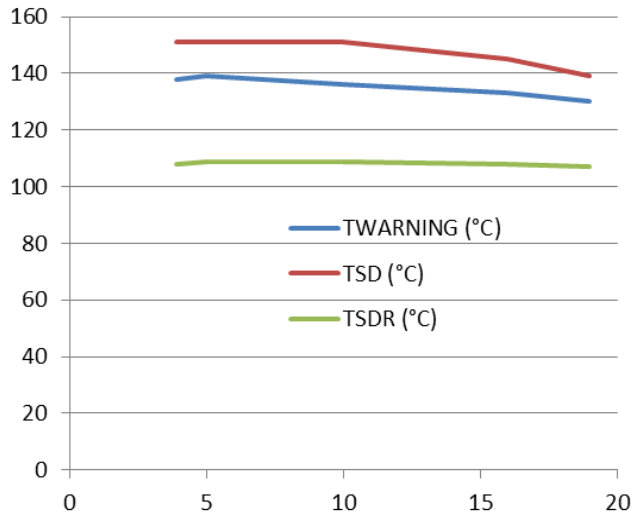


Figure 21. Thermal Comparators vs. Vin

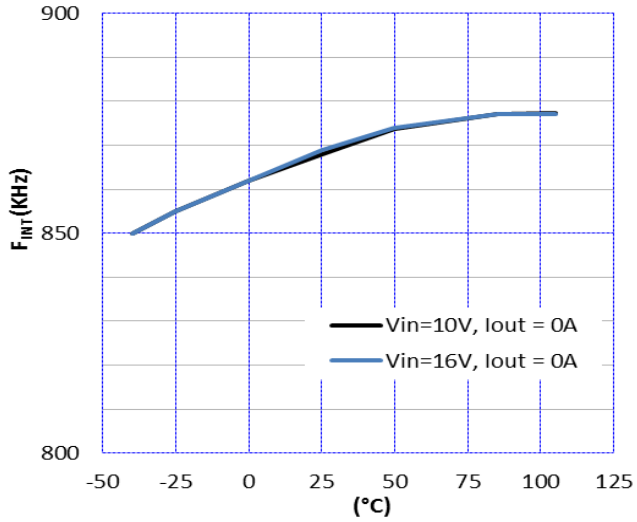


Figure 22. Switching Frequency vs. Temperature

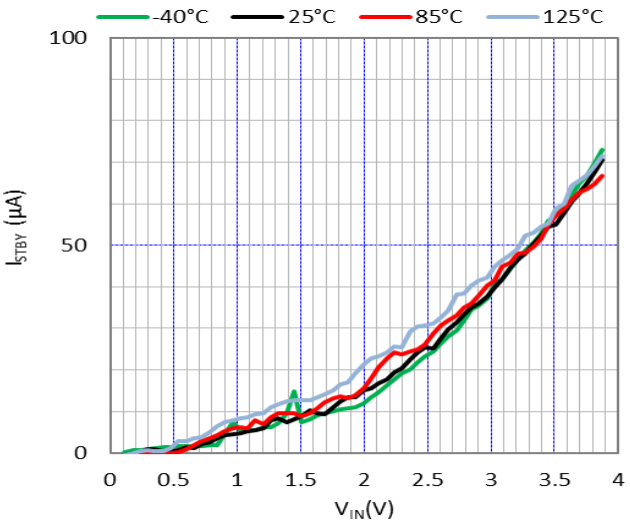


Figure 23. Standby Current vs. Vin, Over Temperature

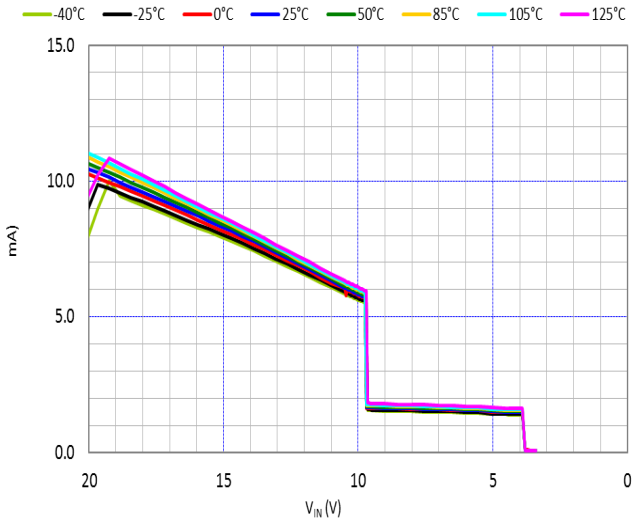


Figure 24. Quiescent Current vs. Vin, Over Temperature, PWR_OK=0

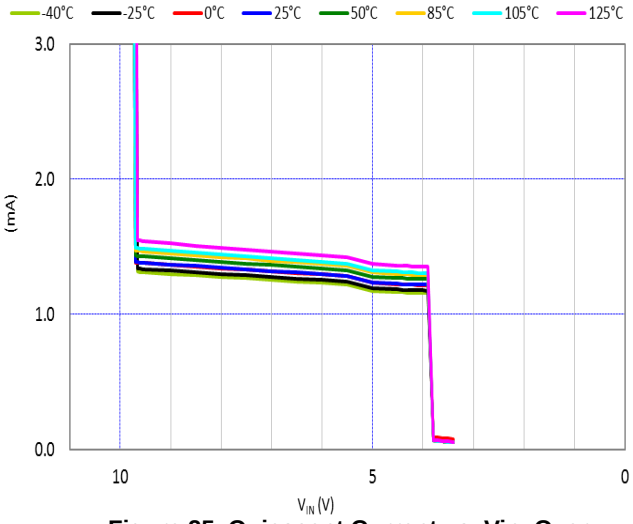


Figure 25. Quiescent Current vs. Vin, Over Temperature, PWR_OK=1

One Wire Interface

Note: to select one wire interface: SEL pin = low level or connected to AGND . As State of the Sel pin is not latched, programming is not recommended before the state of theSEL is established.

The one wire interface is intended for communication between only two devices, where the SCY1751 is considered as a slave. The one wire interface is usable 100 micro seconds after VLDO is available.

Bi−directional communication over the one−wire interface is achieved by multiplexing the transmit and receive functions of the UARTs over the one−wire link. That is, the RX input is ORED with the open−drain TX output onto the one−wire interface at each device.

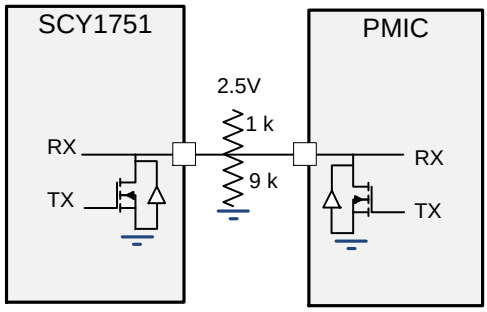


Figure 26. OWI Pull Up Connection

A modified half−duplex UART protocol is used over the one−wire connection. In their quiescent state, both ends are at reception, presenting a high impedance state to the line (held high by the resistor network).

UARTs at both ends are configured as follows, and run at 115.2 kbps:

- One start bit
- Eight data, including command
- One stop bit

Single bit duration is 8.68 μs, so 86.8 μs for a byte, including start and stop.

The data sampling frequency must not exceed ± 3.95 % accuracy to respect 75% of the eyes pattern.

The SCY1751 does not initiate unrequested transmissions. Data transmission is byte oriented. Per a standard UART spec, the line is at “1” (Mark) state when idle. When neither party is transmitting, both ends are tri−stated. The start bit is initiated by a transition to “0” (Space), where the party entering the TX state starts transmission by driving the line to a low level. The least significant bit of a transmitted byte is the first bit on the line.

When the Controller fails to receive a response from the SCY1751 after it has sent a command and is expecting a return, the Controller will timeout and return to the TX state, where:

Timeout = (expected number of bytes) * (byte transmission time + inter byte delay) * 1.1 + 20 ms

NOTE: Timeout is not applicable when no response is expected

The Controller monitors its own data output. Transmission errors detected at the Controller cause the Controller to back off and return to its receive state for at least 25 ms. The SCY1751 does not detect collisions or act on them.

OWI Register MAP

Data is structured as a sequence of bytes, each conveying 6 bits worth of data and 2 bits worth of signaling.

Bits [5:0] convey data; bits [7:6] arbitrate transmission as follows:

Table 12. COMMAND BIT DESCRIPTION TABLE

Command [7:6]	Bit Description
D00	Start byte (command or response), more bytes may follow depending on command
D01	Data continuation, more bytes to follow
D10	End byte (parity) no more bytes to follow
D11	Reserved

Table 13. OWI REGISTER MAP TABLE

WCN command	Reg Name	D7	D6	D5	D4	D3	D2	D1	D0
b000000 (data read)	Status Reg	0	0	OCA_L	OTA_L	1 (Unsd)	COM_ER_L	OVA_L	CHG_OK
	Vin LSB	0	1	Vin [5:0]					
	Vin MSB	0	1	0 (Unsd)				Vin [7:6]	
	Iin LSB	0	1	I in [5:0]					
	Iin MSB	0	1	0 (Unsd)				I in [7:6]	
	Temp LSB	0	1						
	Temp MSB	0	1	0 (Unsd)				Temp [7:6]	
	Offset LSB	0	1	0 (Unsd)					
	Offset MSB	0	1	0 (Unsd)					
	Parity	1	0	Parity					
b000001 (reg read)	Vth Reg	0	0	0 (Unsd)	0 (Unsd)	Vth3	Vth2	Vth1	Vth0
	Vcl Reg	0	1	0 (Unsd)	0 (Unsd)	0 (Unsd)	VCL2	VCL1	VCL0
	Control Reg	0	1	Div_2_delay2	Div_2_delay1	Div_2_delay0	0 (Unsd)	0 (Unsd)	CLO
	Sense Reg	0	1	N_CLI[3:0]				0 (Unsd)	Mode_M
	Parity	1	0	Parity					
b000010 (reg write)	Vth Reg	0	1	0 (Unsd)	0 (Unsd)	Vth3	Vth2	Vth1	Vth0
	Vcl Reg	0	1	0 (Unsd)	0 (Unsd)	0 (Unsd)	VCL2	VCL1	VCL0
	Control Reg	0	1	Div_2_delay2	Div_2_delay1	Div_2_delay0	0 (Unsd)	0 (Unsd)	CLO
	Sense Reg	0	1	N_CLI[3:0]				0 (Unsd)	Mode_M
	Parity	1	0	Parity					
b000011 (reg read)	Status Reg	0	0	OCA_L	OTA_L	1 (Unsd)	COM_ER_L	OVA_L	CHG_OK
b000100 (reg read)	Config Reg	0	0	0 (Unsd)	0 (Unsd)	IB_DLY[1:0]		PWR_OK	1 (Unsd)
	Current Limit	0	1	0	0	1	1	1	1
	Interrupt Reg	0	1	0 (Unsd)	TSD_L	COM_ER_L	OTA_L	OVA_L	OCA_L
	Impedance Limit	0	1	0	0	0	1	0	1
	Parity	1	0	Parity					
b000101 (reg write)	Config Reg	0	1	0 (Unsd)	0 (Unsd)	IB_DLY[1:0]		PWR_OK	1 (Unsd)
	Current Limit	0	1	0	0	1	1	1	1
	Interrupt Reg	0	1	0 (Unsd)	TSD_L	COM_ER_L	OTA_L	OVA_L	OCA_L
	Impedance Limit	0	1	0	0	0	1	0	1
	Parity	1	0	Parity					
b000110 (revision read)	Rev Reg	0	0	REV_ID[5:0]					
b000111 (data read)	Vin LSB	0	0	Vin [5:0]					
	Vin MSB	0	1	0 (Unsd)				Vin [7:6]	
	Iin LSB	0	1	I in [5:0]					
	Iin MSB	0	1	0 (Unsd)				I in [7:6]	
	Parity	1	0	Parity					
b001000−111111		–	–	–	–	–	–	–	–

NOTE: There are no physical bits behind the fixed bits (Unsd: unused) so the bits are hardcoded. So they are read only.

OWI Registers Description

Table 14. STATUS REGISTER

Register Name: Status							
Type: Read				**Default: $08**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	OCA_L	OTA_L	1	COM_ER_L	OVA_L	CHG_OK

Bits	Bits Description
D0	CH_OK bit. 0: CHOK pin is low, CHOK pin is high
D1	OVA_L. Latched over−voltage: 0: Vin<VCL, 1: Vin>VCL
D2	COM_ER_L. Latched comm error : 0 = no error, 1 = error
D3	Unused. Default value: 1
D4	OTA_L. Latched internal warning over−temperature : 0 = no temperature fault, 1 = Over−temperature
D5	OCA_L. Latched internal over−current: 0: No current fault, 1 = Over−current (full scale of current)

NOTE: A status bit read does not clear the associated latched values. Status bits are cleared upon interrupt read and if the interrupt event has disappeared.

Communication Error Details

Three sources of error are detected by the SCY1751:

1. Parity Error: This is defined as a mismatch between the calculated parity and the received parity for a message containing the parity byte. The message is discarded.
2. Framing Error: This is defined as the reception of an invalid stop bit. The byte is discarded.
3. Sequence Error: A sequence error occurs when the SCY1751 receives a byte whose signaling bits (7:6) indicate a sequence error. Specifically, a sequence error is declared on the reception of a byte with end or continuation signaling bits when the start signaling bits are expected, or the reception of start signaling bits when continuation or end signaling bits are expected.

When an unexpected continue byte or end byte is received, the byte is discarded. If an unexpected message start is received, the message in progress is discarded.

If any of these errors occur, the COM_ER bit is set.

Table 15. OWI EVENT TABLE

Event	COM_ER_L set ?	Return to IDLE ?
Receive continuation byte when in IDLE state.	Yes	Yes
Receive end byte when in IDLE state.	Yes	Yes
Receive start byte when expecting continuation byte.	Yes	Yes
Receive end byte when expecting continuation byte.	Yes	Yes
Receive start byte when expecting end byte.	Yes	Yes
Receive continuation byte when expecting end byte.	Yes	Yes
Receive unknown WCN command.	No	Yes
Detect Parity error.	Yes	Yes
Detect Framing error.	Yes	Yes

Table 16. INPUT VOLTAGE REGISTERS: LSB and MSB

Register Name: Vin LSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	Vin Voltage [5:0]					

Bits	**Bits Description**
D5−0	Vin voltage ADC conv

Register Name: Vin MSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	0	Vin Voltage [7−6]	

Bits	**Bits Description**
D1−0	Vin voltage ADC conv. MSB bits 6 and 7.
D5−2	Unused. Default value 0 (read access only)

Table 17. REMOTE CURRENT REGISTERS: LSB and MSB

Register Name: Iin LSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	Input current [5:0]					

Bits	**Bits Description**
D5−0	Input current ADC conv

Register Name: Iin MSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	0	Input current [7−6]	

Bits	**Bits Description**
D1−0	Iin voltage ADC conv. MSB bits 6 and 7.
D5−2	Unused. Default value 0 (read access only)

Table 18. IC TEMPERATURE REGISTERS

Register Name: Temperature LSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	IC temperature [5:0]					

Bits	Bits Description
D5−0	IC temperature ADC conversion

Register Name: Iin MSB							
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	0	IC temperature [7−6]	

Bits	Bits Description
D1−0	IC temperature ADC conv. MSB bits 6 and 7.
D5−2	Unused. Default value 0 (read access only)

Offset Registers: LSB and MSB: Unused

Note: There are no physical register behind the offset bits. The bits are hardcoded, with $00 default value. Only a read can be done to upload the values through OWI interface.

Parity Register and Calculation

Note: Read only can be done to upload the values through OWI interface, and be the result of parity calculation described below.

A multi−byte transmission consists of a command byte and data bytes. The appended parity byte ensure the integrity of the data. Each bit of the parity byte is the result of the XOR of the bits in the same bit location on the parity but. In other words, the parity but Dn is set to 1 if the number of the ones of the corresponding control and data bits Dn is even, and null otherwise.

Table 19. Vth THRESHOLD PROGRAMMING REGISTER

Register Name: Vth							
Type: Read / Write				**Default: $03**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	Vth [3:0]			

Bits	Bits Description
D3−0	Vth comparator programming. Cf Vth table.
D5−4	Unused: Default value 0 (Read access only)

Table 20. Vcl THRESHOLD PROGRAMMING REGISTER

Register Name: Vcl							
Type: Read / Write				**Default: $07**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	VCL [2:0]		

Bits	Bits Description
D2−0	V clamp comparator. Cf Vth table.
D5−3	Unused: Default value 0 (Read access only)

NOTE: Refer to Charge pump functionality chapter for VCL programmable table.

Table 21. CONTROL REGISTER

Register Name: Control register							
Type: Read / Write				**Default: $08**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	Div_2_delay2	Div_2_delay1	Div_2_delay0	0	0	CLO

Bits	Bits Description
D0	0: CLO output is valid, 1: CLO pin is disable
D2−1	Unused: Default value 0 (Read access only)
D5−3	Delay between MODE being de−asserted (divide−by−2−mode) and PT (Vin falling, Vth is crossed)

Table 22. SENSE REGISTER

Register Name: Sense register							
Type: Read / Write				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	N_CLI [5:2]				0	Mode_M

Bits	Bits Description
D0	0 if Vin < Vth, pass through. 1 if Vin > Vth, CP x0.5
D1	Unused: Default value 0 (Read access only)
D5−2	N Factor. Cf N factor Table

Table 23. CONFIGURATION REGISTER

Register Name: Configuration_0							
Type: Read / Write				**Default: $01**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	IB_DLY1	IB_DLY0	PWR_OK	1

Bits	Bits Description
D0	Unused: Default value 1 (Read access only)
D1	PWR_OK = 0 force CHOK low, PWR_OK = 1 force CHOK high (if Vin > UVLO).
D3−2	Inter Byte delay. Default 00
D5−4	Unused: Default value 0 (Read access only)

Inter Byte Delay Description:

The byte transmission rate will be controlled by setting the inter byte delay on SCY1751. This latency is intended to minimize the possibility of data loss at the host when servicing data reception in firmware. The host will emit bytes without timing restriction as hardware processing is expected.

Table 24. INTER BYTES DELAY TABLE

IB_DLY	Delay
00	0 ms + 4 bit times
01	1 ms + 4 bit times
10	2 ms + 4 bit times
11	4 ms + 4 bit times

Notes:

1. Single byte transmission time = 10 bits/115.2 kbps = 86.8 μs
2. Assuming that the host UART may have a two−byte receiving buffer and is serviced with an interrupt as is common in many microcontrollers, multi−byte transmissions may require an inter−byte transmission delay to accommodate the slow processing of the receiving device. The host can configure SCY1751 to set different inter−byte delay values.

Table 25. CURRENT LIMIT REGISTER

Register Name: Current limit							
Type: Read / Write				**Default: $0F**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	1	1	1	1

Bits	Bits Description
D5−0	Reserved − Default values 001111. R/W access allowed.

Table 26. INTERRUPTS REGISTER

Register Name: Alarm interrupts							
Type: Read to clear				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	TSD_L	COM_ER_L	OTA_L	OVA_L	OCA_L

Bits	Bits Description
D0	OCA_L (latched over current alarm) is reset to present value upon read operation. This bit is latched and held true (True = 1) if the condition occurs between reads.
D1	OVA_L (latched VCL) is reset to present value upon read operation. This bit is latched and held true (True = 1) if the condition occurs between reads.
D2	OTA_L (latched TSD warning) is reset to present value upon read operation. This bit is latched and held true (True = 1) if the condition occurs between reads.
D3	COM_ER_L is reset to present value upon read operation. This bit is latched and held true (True = 1) if the condition occurs between reads.
D4	TSD_L (latched TSD) is reset to present value upon read operation. This bit is latched and held true (True = 1) if the condition occurs between reads.
D5	Unused: Default value 0 (Read access only)

NOTE: Interrupt are cleared upon read only if the event is no more present.

Table 27. IMPEDANCE LIMIT REGISTER

Register Name: Impedance limit register							
Type: Read / Write				**Default: $05**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	1	0	1

Bits	Bits Description
D5−0	Reserved − Default values 000101. R/W access allowed.

Table 28. REVISION ID REGISTER

Register Name: Revision ID							
Type: Read / Write				**Default: $01**			
D7	D6	D5	D4	D3	D2	D1	D0
−	−	0	0	0	0	0	1

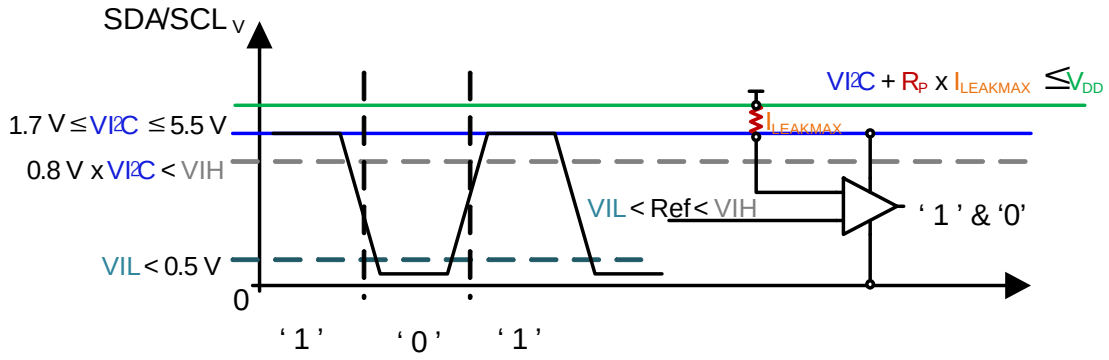
Bits	Bits Description
D5−0	IC revision

I²C Compatible Interface

NOTE: To select I²C interface: SEL pin = high level or connected to VLDO. As State of the Sel pin is not latched, programming is not recommended before the state of theSEL is established.

The I²C is intended for communication between only two devices, where the SCY1751 is considered as a slave. The one wire interface is usable 100 micro seconds after VLDO is available.

Voltage levels are describe below:



I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

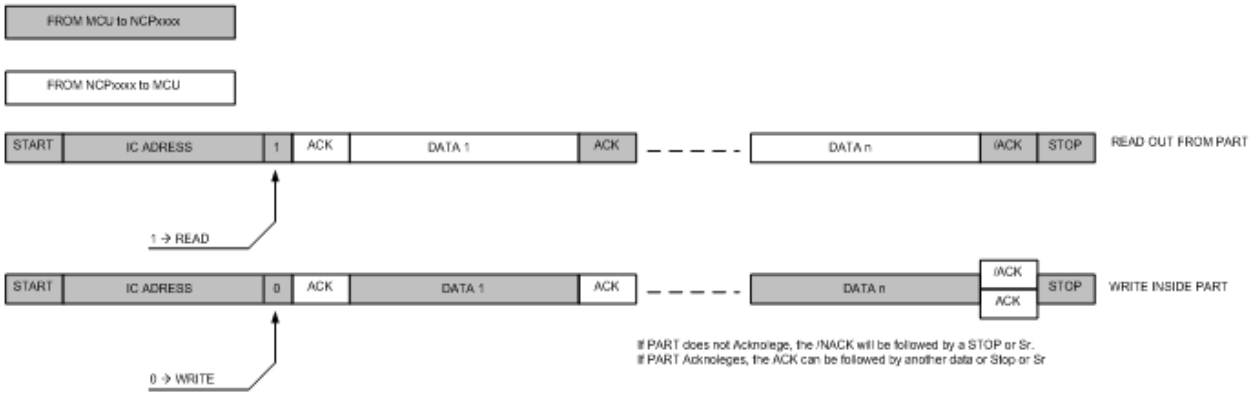


Figure 27. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) pointing to the register we want to write in followed by the data we will write in that location. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1 ... etc.
- In case of read operation, the SCY1751 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.

Read out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set.

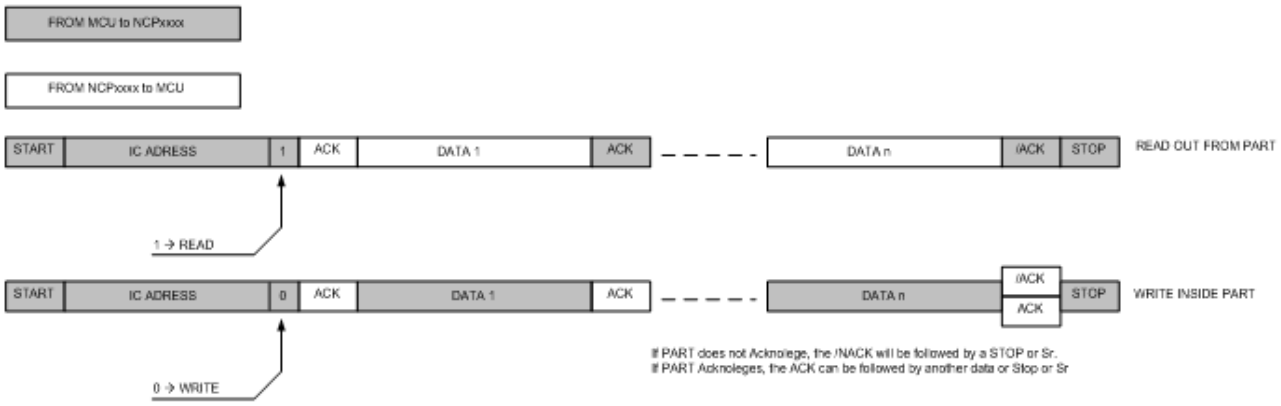


Figure 28. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

1. With Stop Then Start

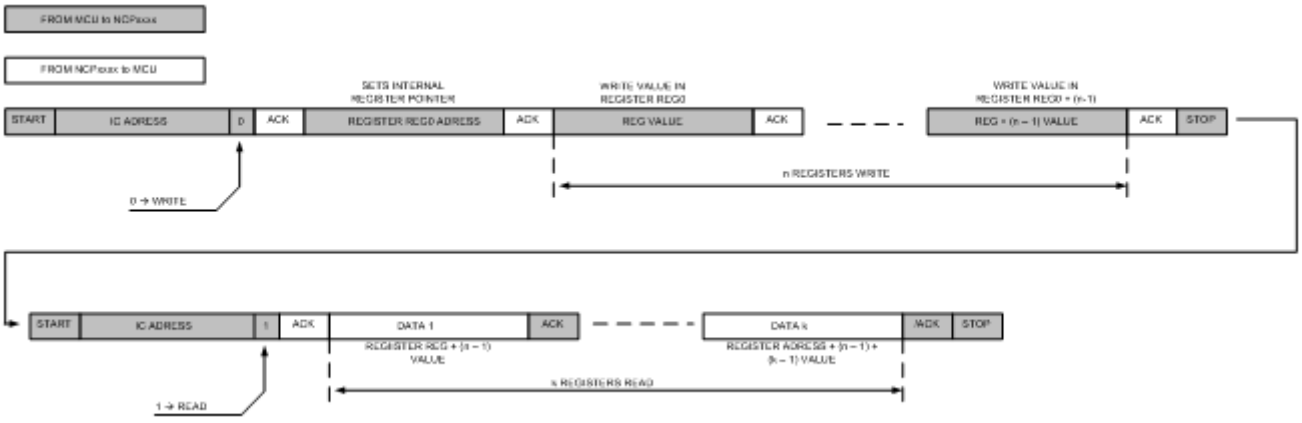


Figure 29. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg +n.

Write n Registers:

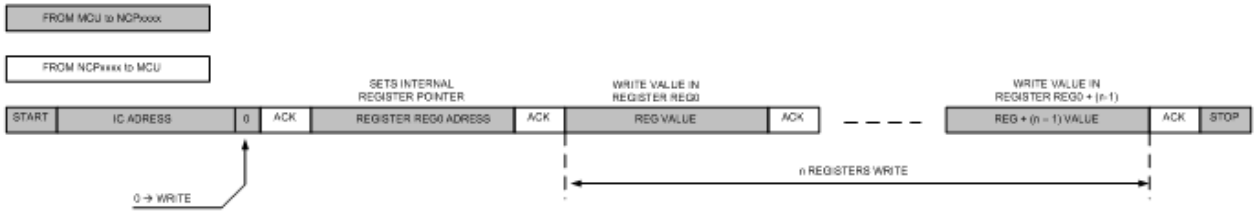


Figure 30. Write in n Registers

Table 29. I²C ADDRESS

Register Name: I²C address							
Type: Read / Write				**Default: $31**			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	R (1)/W(0)

Table 30. I²C REGISTER MAP SUMMARY

Name	Address	Def value	B7	B6	B5	B4	B3	B2	B1	B0
Status	$00	$00	I_LDO_L	Mode_L	OCA_L	OTA_L	TSD_L	CONV_L	OVA_L	CHG_OK_L
Vin LSB/MSB	$01	$00	Vin voltage [7:0]							
Iin LSB/MSB	$02	$00	Remote current [7:0]							
Temp LSB/MSB	$03	$00	IC Temperature [7:0]							
Command 1	$04	$73	0	VCL [2:0]			Vth [3:0]			
Command 2	$05	$29	Div_2_delay2	Div_2_delay1	Div_2_delay0	CONV_Delay [4:3]		CLO_DIS	PWR_OK	1
Command 3	$06	$02 (VLDO 2.5V) $01 (VLDO 1.8V)	0	0	0	0	CONV_M	CONV_R	VLDO[1:0]	
Sense 1	$07	$00	I_LDO_S	Mode_S	OCA_S	OTA_S	TSD_S	CONV_S	OVA_S	CONV_S
Sense 2	$08	$00	0	0	N_CLI[5:2]				0	0
Interrupt	$09	$00	I_LDO_I	Mode_I	OCA_I	OTA_I	TSD_I	CONV_I	OVA_I	CONV_I
ID	$0A	$02	0	0	0	0	0	0	1	0

Table 31. STATUS REGISTER

Register Name: Status				Address: $00			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
I_LDO_L	Mode_L	OCA_L	OTA_L	TSD_L	CONV_L	OVA_L	CHG_OK_L

Bits	Bits Description
D0	Latched CHG_OK_L (0: CHG_DONE, 1: CHG_REQ)
D1	Latched over voltage (0: Vin<VCL, 1: Vin>VCL)
D2	Latched ADC Conversion (0: Conversion not done , 1: Conversion done)
D3	Latched thermal shutdown (0: No TSD event, 1: TSD comparator crossed)
D4	Latched thermal warning (0: IC temp < TSD Warning, 1: IC temp > TSD Warning)
D5	Latched over current (1: FF on the remote current reading)
D6	Latched Vth threshold (0: Vth not crossed, 1: Vth crossed)
D7	Latched VLDO over current (0: clamp current not crossed, 1: clamp crossed)

Table 32. INPUT VOLTAGE REGISTER

Register Name: Vin LSB/MSB				Address: $01			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
Vin Voltage [7:0]							

Bits	Bits Description
D7−0	Vin voltage ADC conv

Table 33. REMOTE CURRENT REGISTER

Register Name: Iin LSB/MSB				**Address: $02**			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
Iin Current [7:0]							

Bits	Bits Description
D7−0	Iin current ADC conv

Table 34. INPUT TEMPERATURE REGISTER

Register Name: Temp LSB/MSB				**Address: $03**			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
IC temperature [7:0]							

Bits	Bits Description
D7−0	IC temperature ADC conv

Table 35. COMMAND 1 REGISTER

Register Name: Command 1				**Address: $04**			
Type: R/W				**Default: $73**			
D7	D6	D5	D4	D3	D2	D1	D0
0	Vcl [2:0]			Vth [3:0]			

Bits	Bits Description
D3−0	Vth threshold. Cf Vth table. Default value: 9.8 V. (0011)
D6−4	Vcl threshold. Cf Vcl table. Default value: 22.9 V (111)
D7	Unused. Default value : 0

Table 36. COMMAND 2 REGISTER

Register Name: Command 2				**Address: $05**			
Type: R/W				**Default: $29**			
D7	D6	D5	D4	D3	D2	D1	D0
Div_2_delay2 [7:5]			CONV_Delay (4:3]		CLO_DIS	PWR_OK	1

Bits	Bits Description
D0	Unused. Default value: 1
D1	PWR_OK bit. PWR_OK= 0 force CHOK low, PWR_OK= 1 force CHOK high, default = 0
D2	CLO bit. CLO forced off: 1
D4−3	CONV_Delay. ADC Conversion delay in automatic mode. Delay between 2 conversions. 00: 10 ms 01: 2 ms (Default) 10: 1 ms 11: 500 μs
D7−5	DIV_2_Delay: Cf DIV_2_delay table

Table 37. COMMAND 3 REGISTER

Register Name: Command 3				**Address: $06**			
Type: R/W				**Default: Depends on VLOD version**			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	CONV_M	CONV_R	VLDO [1:0]	

Bits	Bits Description
D1−0	VLDO threshold programming. b00: 1.5 V b01: 1.8 V b10: 2.5 V b11: 3.3 V
D2	CONV_R bit. Manual ADC conversion request. Need CONV_M = 1
D3	CONV_M bit. This bit is set to 1 to force manual convesion of the ADC.
D7−4	Unused bits. Default value 0.

Table 38. SENSE 1 REGISTER

Register Name: Sense 1				**Address: $07**			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
I_LDO_S	Mode_S	OCA_S	OTA_S	TSD_S	CONV_S	OVA_S	CHG_OK_S

Bits	Bits Description
D0	CHG OK S bit. Comparator output. 0: CH_OK low, 1: CH_OK high
D1	OVA_S bit. Vcl comparator output. 0: Vin<VCL, 1: Vin>VCL
D2	CONV_S bit. ADC conversion status. 1: ADC conversion on going.
D3	TSD_S bit. Thermal Shutdown comparator output. 0: no TSD, 1: IC temperature over TSD
D4	OTA_S bit. Thermal Warning comparator output. 0: IC temp < TSD Warn, 1: IC temp > TSD Warn
D5	OCA_S bit. 0: no over current, 1: FF on the remote current reading
D6	Mode_S bit. Vth comparator output. 0: Vin<Vth (pass through), 1: Vin>Vth (Div2)
D7	I_LDO_S bit. LDO current clamp comparator output. 1: Load current on VLDO > clamp current

Table 39. SENSE 2 REGISTER

Register Name: Sense 2				**Address: $08**			
Type: Read				**Default: $00**			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	N_CLI [5:2]				0	0

Bits	Bits Description
D1−0	Unused. Default value 0
D5−2	N Factor. Cf N factor table
D7−6	Unused. Default value 0

Table 40. INTERRUPTS REGISTER

Register Name: Interrupt				Address: $09			
Type: Read to clear				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
I_LDO_I	Mode_I	OCA_I	OTA_I	TSD_I	CONV_I	OVA_I	CHG_OK_I

Bits	Bits Description
D0	CH OK I bit. Charge OK interrupt.
D1	OVA_I bit. Over voltage onterrupt (Vcl comparator)
D2	CONV_I bit. ADC conversion interrupt.
D3	TSD_I bit. Thermal Shutdown interrupt.
D4	OTA_I bit. Thermal Warning interrupt.
D5	OCA_I bit. Over current interrupt (ADC full scale on current input).
D6	Mode_I bit. Change mode interrupt (Vth comparator).
D7	I_LDO_I bit. Interrupt of the current protection of the VLDO.

Table 41. REVISION ID REGISTER

Register Name: REV_ID				Address: $0A			
Type: Read				Default: $02			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0

ORDERING INFORMATION

Device	Marking	Package	Shipping†
SCY1751FCCT1G	1751	WLCSP28 (Pb-Free)	3000 / Tape & Reel
SCY1751FCCAT1G	1751A		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PROGRAMMING OPTIONS PER OPN

OPN#	Vth		VCL		DIV2_Delay		IB_DLY (OWI only)		CONV_Delay (I^2C only)		VLDO (I^2C only)	
SCY1751FCCT1G	9.8 V	b0011	22.9 V	b111	150 μS	b001	0 ms	b00	2 ms	b01	2.5 V	b10
SCY1751FCCAT1G	9.8 V	b0011	22.9 V	b111	150 μS	b001	0 ms	b00	2 ms	b01	1.8 V	b01

DEMOBOARD SCHEMATIC

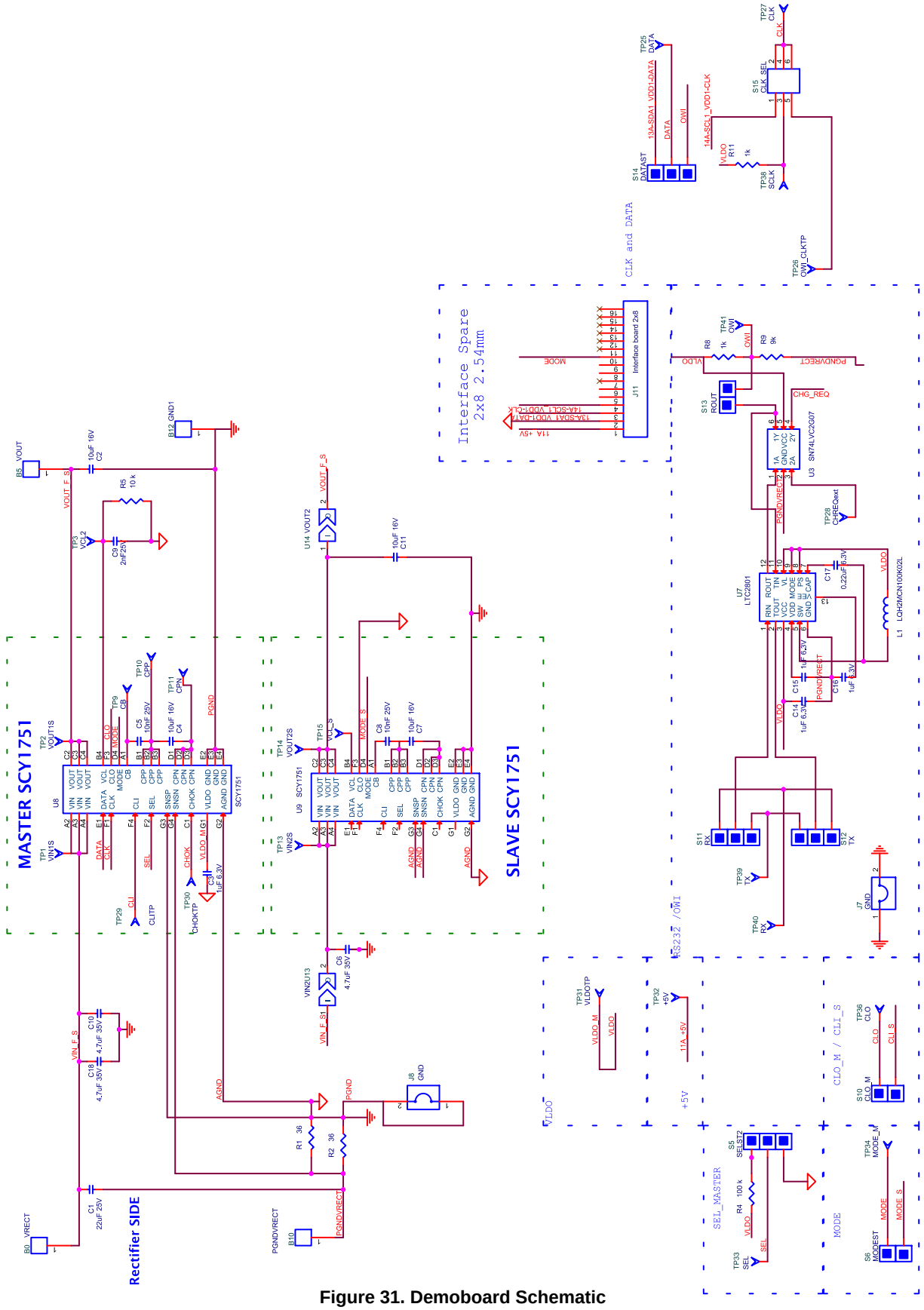


Figure 31. Demoboard Schematic

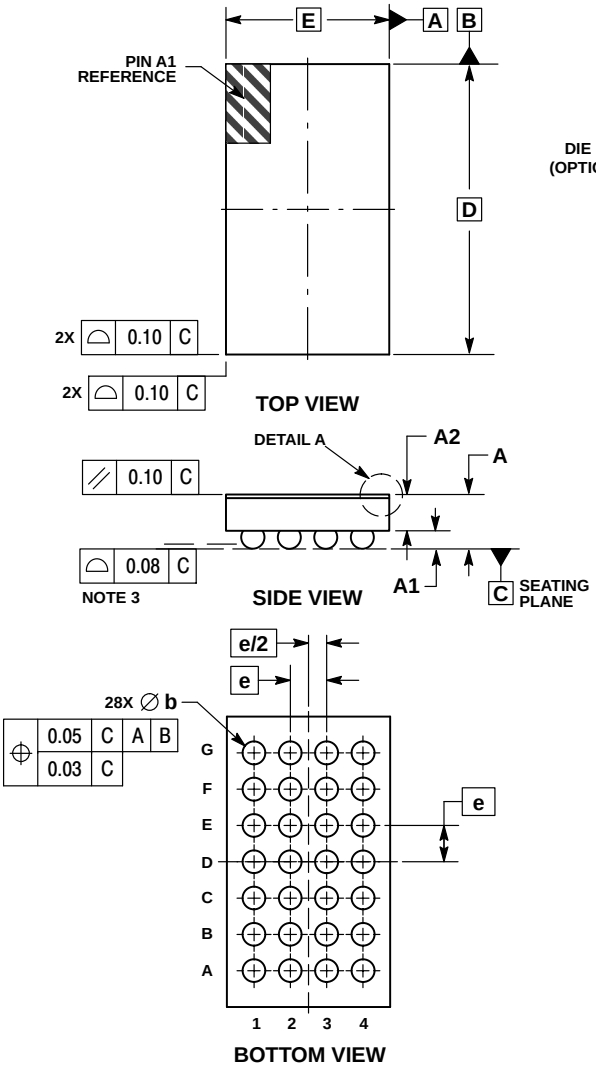
Table 42. BILL OF MATERIAL (BOM)

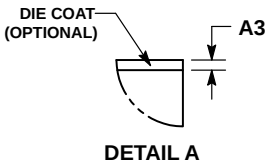
Reference	Value	Manufatcurer −Reference	PCB Footprint
B0	VRECT	MULTICOMP 24.243.1	A−2.107
B5	VOUT	MULTICOMP 24.243.1	A−2.107
B10	PGNDVRECT	MULTICOMP 24.243.2	A−2.107
B12	GND1	MULTICOMP 24.243.2	A−2.107
C1	22uF 25V	MURATA_GRM31CR61E226ME15	SMD_0805/1206
C2,C4,C7,C11	10uF 16V	MURATA_GRM188R61C106KAAL	SMD_0603/0805
C3,C14,C15,C16	1uF 6.3V	Murata_GRM185R60J105KE26	SMD_0603/0805
C5,C8	10nF 25V	Murata_GDM155B11E103MA01	SMD_0402
C6,C10,C18	4.7uF 35V	MURATA_GRM188R6YA475ME15	SMD_0603/0805
C9	2nF 25V	Murata_GRM188B11E202JA01	SMD_0402/0603
C17	0.22uF 6.3V	Murata_GRM152B30J224KE19	SMD_0603/0805
J7,J8	GND	Harwin_D3082F05	JUMPER400_H
J11	Interface board 2x8		HE10−20MD−2
L1	LQH2MCN100K02L	Murata_LQH2MCN100K02L	SMD_0805/1206
R1,R2	36	Panasonic_ERJ6BWFR036	SMD_0603/0805/1206
R4	100 k	Multicomp_MC0063W06031100K	SMD_0603/0805
R5	10 k	Multicomp_MC0063W0603110K	SMD_0603/0805
R8,R11	1k	Multicomp_MC0063W060311K	SMD_0603/0805
R9	9k	Multicomp_MC0063W060319K09	SMD_0603/0805
S5	SELST2	77311_401_36LF	HEADER_3_100
S6	MODEST	77311_401_36LF	HEADER_2_100
S10	CLO_M	77311_401_36LF	HEADER_2_100
S11	RX	77311_401_36LF	HEADER_3_100
S12	TX	77311_401_36LF	HEADER_3_100
S13	ROUT	77311_401_36LF	HEADER_2_100
S14	DATAST	77311_401_36LF	HEADER_3_100
S15	CLK_SEL	Fisher_SL202572G	HEADER_3X2_100
TP1	VIN1S	Keystone_5016	PAD3.5x4.7
TP2	VOUT1S	Keystone_5016	PAD3.5x4.7
TP3	VCL2	Keystone_5016	PAD3.5x4.7
TP9	CB	Keystone_5016	PAD3.5x4.7
TP10	CPP	Keystone_5016	PAD3.5x4.7
TP11	CPN	Keystone_5016	PAD3.5x4.7
TP13	VIN2S	Keystone_5016	PAD3.5x4.7
TP14	VOUT2S	Keystone_5016	PAD3.5x4.7
TP15	VCL_S	Keystone_5016	PAD3.5x4.7
TP25	DATA	Keystone_5016	PAD3.5x4.7
TP26	OWI_CLKTP	Keystone_5016	PAD3.5x4.7
TP27	CLK	Keystone_5016	PAD3.5x4.7
TP29	CLITP	Keystone_5016	PAD3.5x4.7
TP30	CHOKTP	Keystone_5016	PAD3.5x4.7
TP31	VLDOTP	Keystone_5016	PAD3.5x4.7
TP32	+5V	Keystone_5016	PAD3.5x4.7
TP33	SEL	Keystone_5016	PAD3.5x4.7
TP34	MODE_M	Keystone_5016	PAD3.5x4.7
TP36	CLO	Keystone_5016	PAD3.5x4.7
TP38	SCLK	Keystone_5016	PAD3.5x4.7
TP39	TX	Keystone_5016	PAD3.5x4.7
TP40	RX	Keystone_5016	PAD3.5x4.7
TP41	OWI	Keystone_5016	PAD3.5x4.7
U3	SN74LVC2G07	SN74LVC2G07DCKR	DCK−R−PDS0−G6
U7	LTC2801	LT_2801CDEPBF	DFN_12_4X3_0.5P
U8,U9	SCY1751		FLIP−CHIP_28_3.2X1.8_0.4P
U13	VIN2		STRAP_PCB
U14	VOUT2		STRAP_PCB

SCY1751

PACKAGE DIMENSIONS

WLCSP28, 2.9x1.9, 0.4P
CASE 567JJ
ISSUE D

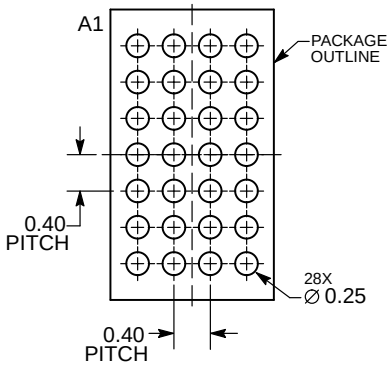




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.02	0.03
b	0.24	0.30
D	2.90 BSC	
E	1.90 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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