ON Semiconductor®

SSR1N60BTM-WS / SSU1N60BTU-WS

N-Channel MOSFET

600 V, 0.9 A, 12 Ω

Features

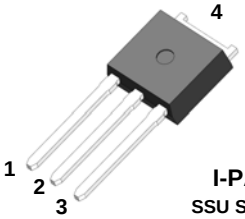
- 0.9A, 600V, $R_{DS(on)}$ = 12Ω @V_{GS} = 10 V
- Low gate charge (typical 5.9 nC)
- Low Crss (typical 3.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

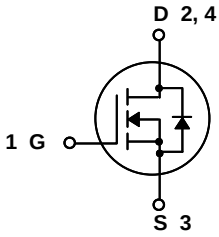
These N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

D-PAK
SSR Series



I-PAK
SSU Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		SSR1N60BTM-WS / SSU1N60BTU-WS	Unit
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		0.9	A
	- Continuous (T_C = 100°C)		0.57	
I_{DM}	Drain Current - Pulsed	(Note 1)	3.0	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	50	mJ
I_{AR}	Avalanche Current	(Note 1)	0.9	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		28	W
	- Derate above 25°C		0.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	4.53	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	-	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

September-2017, Rev. 2

Publication Order Number:
SSR1N60BTM-WS/D

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.65	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	10	μA
		V_{DS} = 480 V, T_C = 125°C	-	-	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 0.45 A	-	9.7	12	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 0.45 A (Note4)	-	0.92	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	-	165	215	pF
C_{oss}	Output Capacitance		-	18	25	pF
C_{rss}	Reverse Transfer Capacitance		-	3.6	4.7	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 1.0 A, R_G = 25 Ω	-	14	40	ns
t_r	Turn-On Rise Time		-	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		-	25	60	ns
t_f	Turn-Off Fall Time	(Note 4,5)	-	35	80	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 1.0 A, V_{GS} = 10 V	-	5.9	7.7	nC
Q_{gs}	Gate-Source Charge		-	1.0	-	nC
Q_{gd}	Gate-Drain Charge	(Note 4,5)	-	2.7	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.9	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	3.0	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.9 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 1.0 A, dI_F / dt = 100 A/μs (Note 4)	-	180	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.47	-	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 115mH, I_{AS} = 0.9A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 1.0A, di/dt $\leq$ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300μs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

Figure 1. On-Region Characteristics

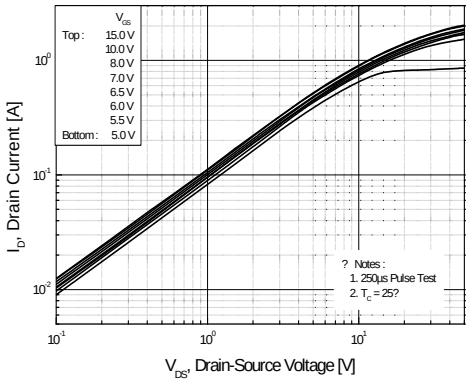


Figure 2. Transfer Characteristics

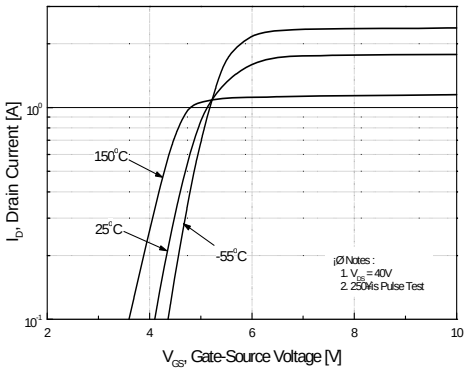


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

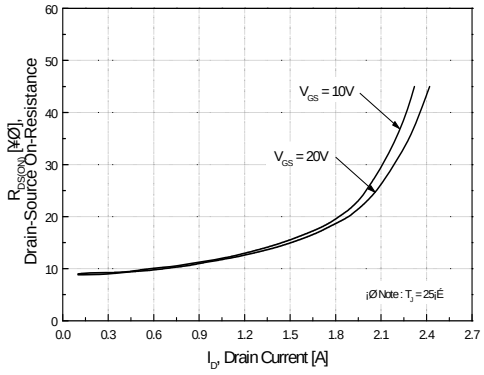


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

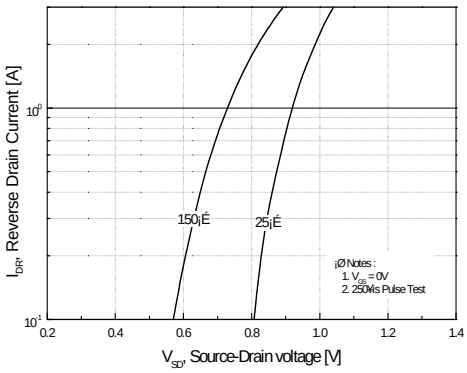


Figure 5. Capacitance Characteristics

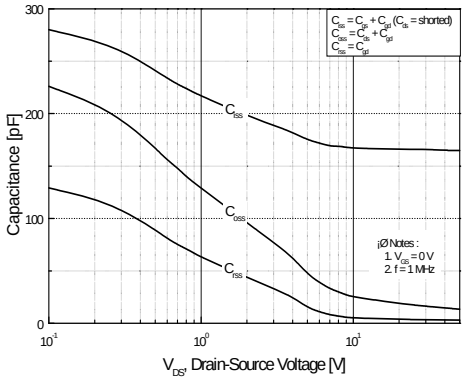
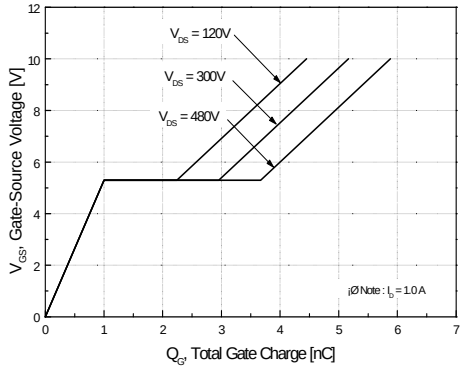


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

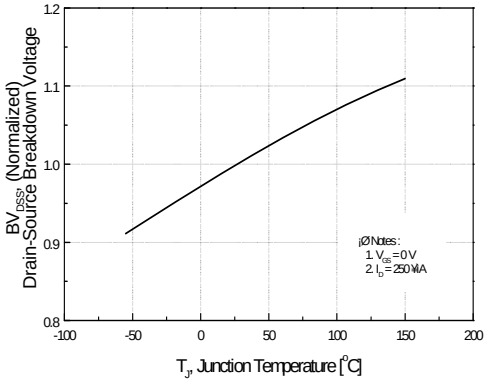


Figure 8. On-Resistance Variation vs. Temperature

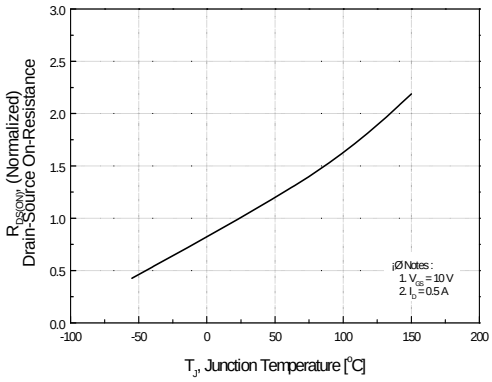


Figure 9. Maximum Safe Operating Area

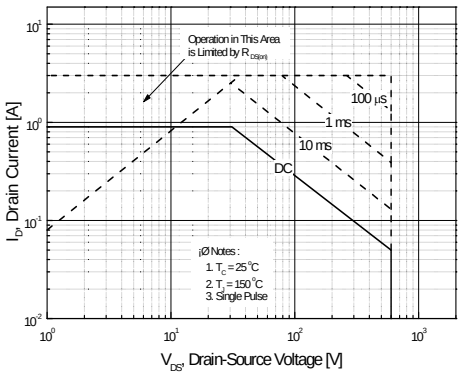


Figure 10.Maximum Safe Operating Area vs. Case Temperature

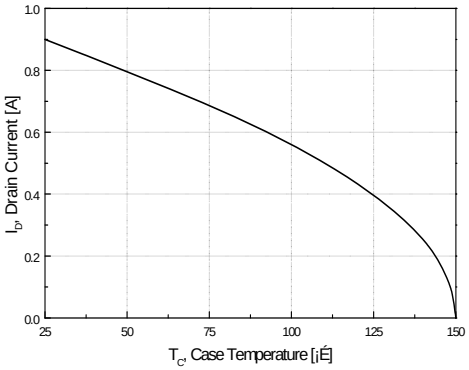


Figure 11. Transient Thermal Response Curve

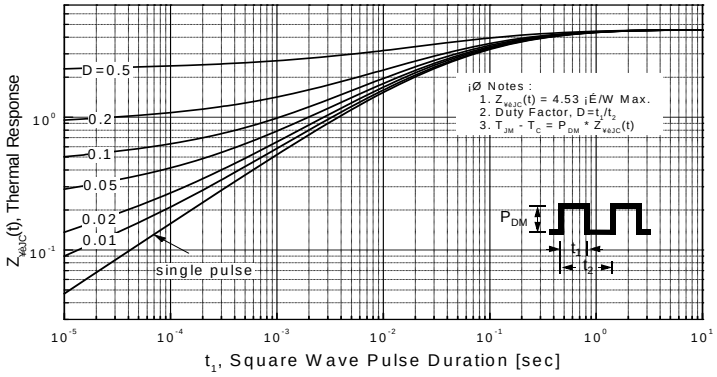


Figure 12. Gate Charge Test Circuit & Waveform

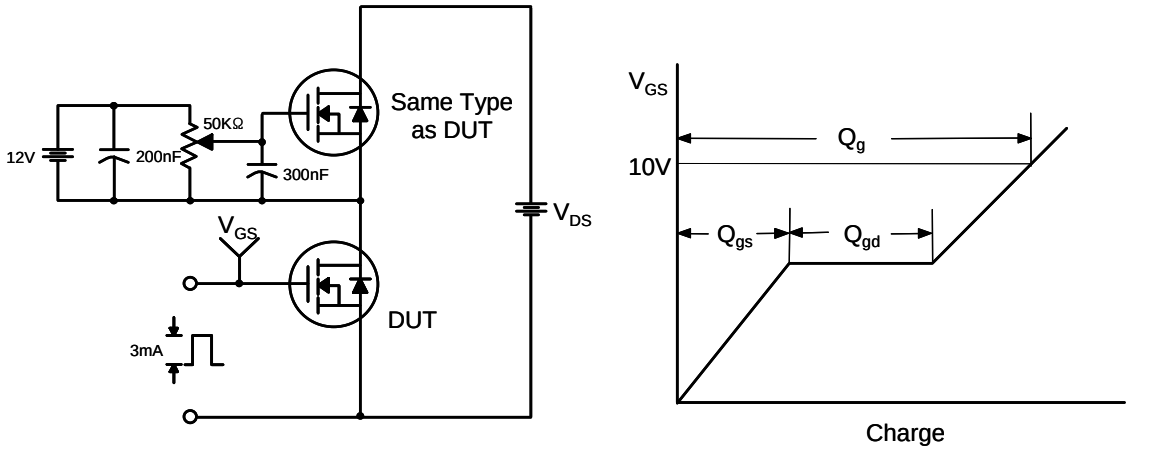


Figure 13. Resistive Switching Test Circuit & Waveforms

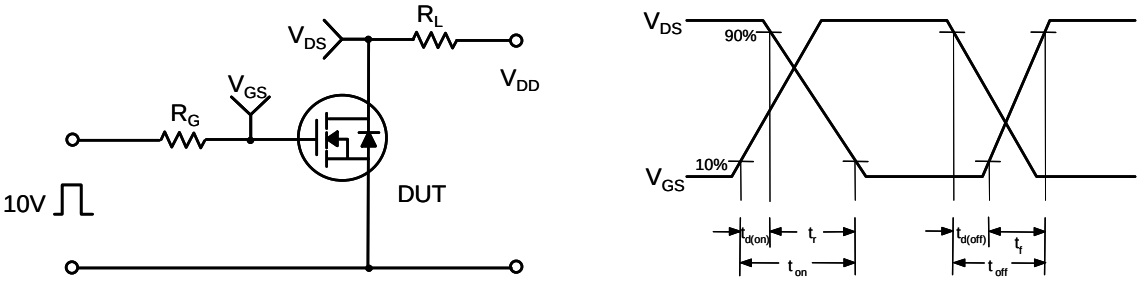


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

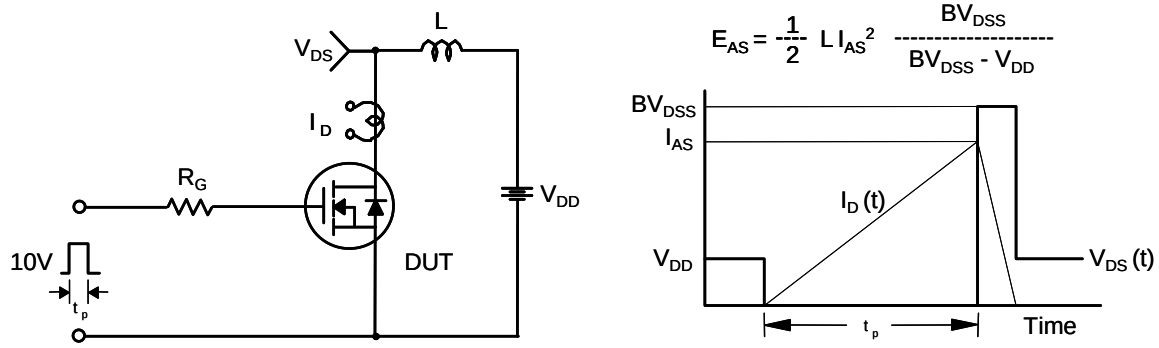
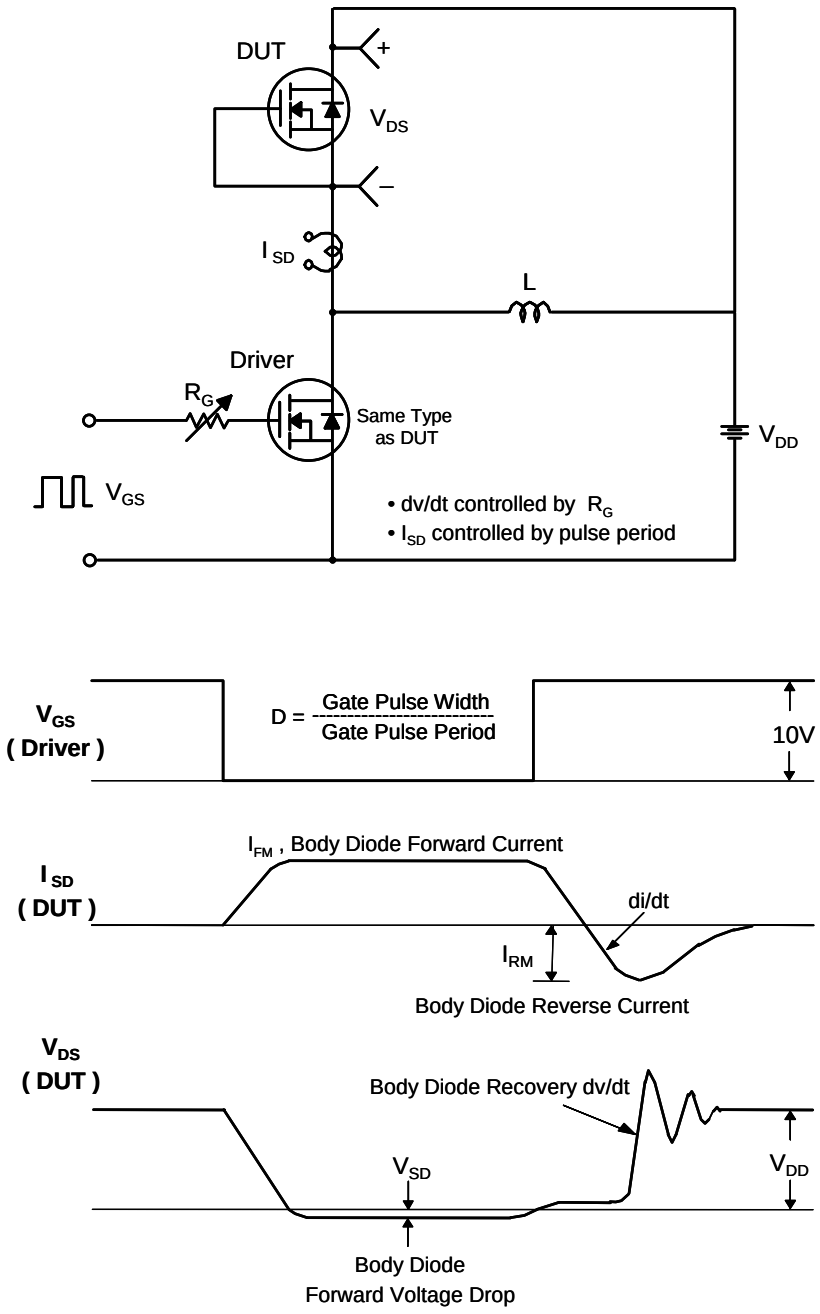
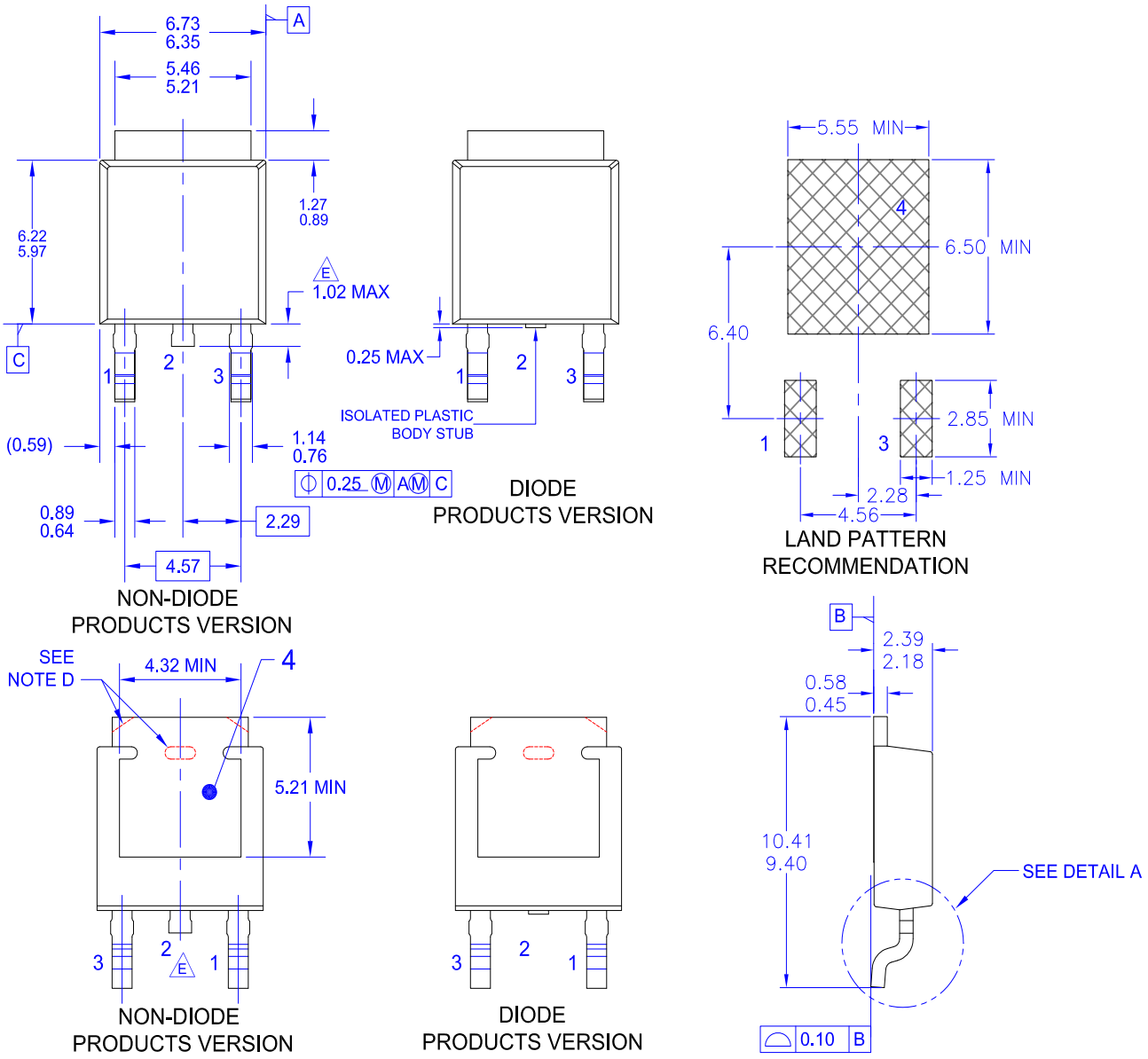


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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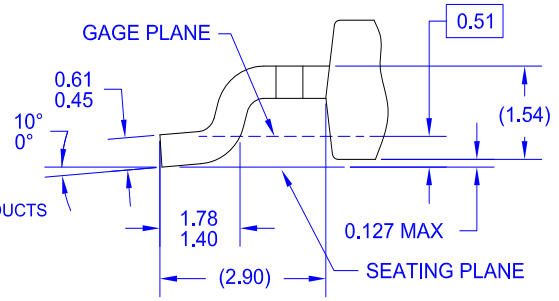
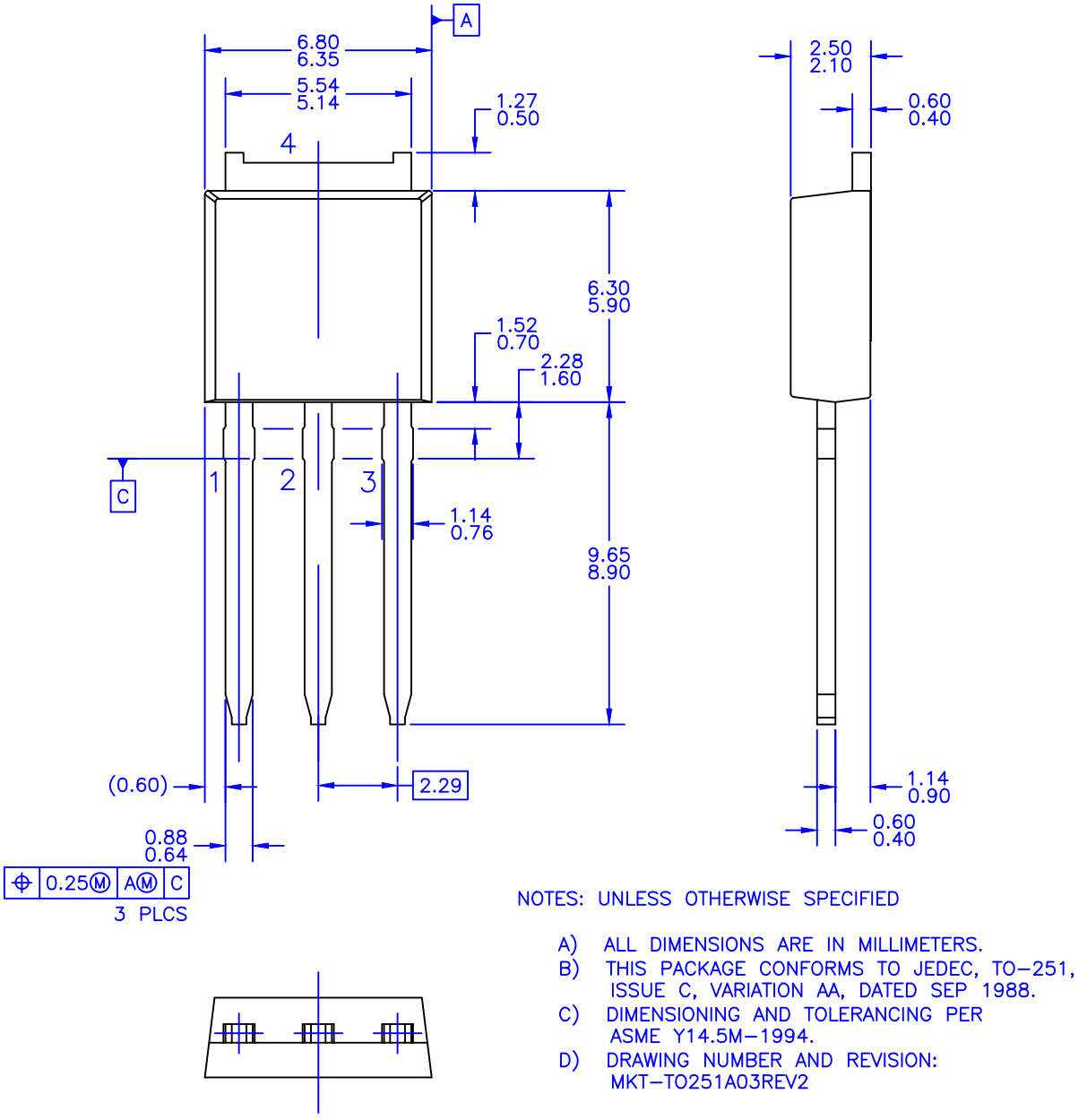
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X



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D) DRAWING NUMBER AND REVISION: MKT−TO251A03REV2

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