# STK5F4U3E2D-E

# Intelligent Power Module (IPM)
# 600 V, 50 A

ON Semiconductor®

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### Overview

This “Inverter Power IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single DIP module (Dual-In line Package). Output stage uses IGBT / FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

### Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- A single power supply drive is enabled through the use of bootstrap circuits for upper power supplies
- Built-in dead-time for shoot-thru protection
- Having open emitter output for low side IGBTs ; individual shunt resistor per phase for OCP
- Externally accessible embedded thermistor for substrate temperature measurement
- Shutdown function ‘ITRIP’ to disable all operations of the 6 phase output stage by external input

### Certification

- UL1557 (File number : E339285)

### Specifications

**Absolute Maximum Ratings** at Ta = 25°C

| Parameter | Symbol | Remarks | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | P to NU,NV,NW, surge < 500 V *1 | 450 | V |
| Collector-emitter voltage | $V_{CE}$ | P to U, V, W, U to NU, V to NV, or W to NW | 600 | V |
| Output current | Io | P, N, U, V, W terminal current | ±50 | A |
| | | P, N, U, V, W terminal current, Tc = 100°C | ±25 | |
| Output peak current | Iop | P, N, U, V, W terminal current, PW = 1 ms | ±100 | A |
| Pre-driver supply voltage | VD1, 2, 3, 4 | VB1 to VS1, VB2 to VS2, VB3 to VS3, $V_{DD}$ to $V_{SS}$ *2 | 20 | V |
| Input signal voltage | VIN | HIN1, 2, 3, LIN1, 2, 3, terminal | −0.3 to VDD | V |
| FAULT terminal voltage | VFAULT | FAULT terminal | −0.3 to VDD | V |
| Maximum loss | Pd | IGBT per channel | 62.5 | W |
| Junction temperature | Tj | IGBT, FRD | 150 | °C |
| Storage temperature | Tstg | | −40 to +125 | °C |
| Operating temperature | Tc | IPM case | −20 to +100 | °C |
| Tightening torque | MT | A screw part at use M4 type screw *3 | 1.17 | Nm |
| Withstand Voltage | Vis | 50 Hz sine wave AC 1 minute *4 | 2000 | VRMS |

Reference voltage is “$V_{SS}$” terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between the P and N terminals.
*2 : Terminal voltage : VD1 = VB1 to VS1, VD2 = VB2 to VS2, VD3 = VB3 to VS3, VD4 = $V_{DD}$ to $V_{SS}$.
*3 : Flatness of the heat-sink should be 0.25 mm and below.
*4 . Test conditions : AC 2500 V, 1 s.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

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**Electrical Characteristics** at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

| Parameters | Symbols | Conditions | Test Circuit | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| **Power output section** | | | | | | | |
| Collector-to-emitter cut-off current | $I_{CE}$ | $V_{CE}$ = 600 V | Fig.1 | - | - | 1.0 | mA |
| Boot-strap diode reverse current | IR(BD) | VR(BD) = 600 V | - | - | - | 0.5 | mA |
| Collector-to-emitter saturation voltage | $V_{CE}$(sat) | Io = 50 A, Tj = 25°C | Fig.2 | - | 1.7 | 2.6 | V |
| | | Io = 25 A, Tj = 100°C | | - | 2.3 | - | |
| Diode forward voltage | VF | Io = 50 A, Tj = 25°C | Fig.3 | - | 1.8 | 2.7 | V |
| | | Io = 25 A, Tj = 100°C | | - | 2.5 | - | |
| Junction to case thermal resistance | θj-c(T) | IGBT | - | - | 1.5 | - | °C/W |
| | θj-c(D) | FWD | - | - | 1.8 | - | °C/W |
| **Control (Pre-driver) section** | | | | | | | |
| Pre-drive power supply consumption current | ID | VD1, 2, 3 = 15 V | Fig.4 | - | 0.05 | 0.4 | mA |
| | | VD4 = 15 V | | - | 1.0 | 4.0 | |
| High level input voltage | Vin H | HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 | - | 2.5 | - | - | V |
| Low level input voltage | Vin L | | - | - | - | 0.8 | V |
| **Protection section** | | | | | | | |
| ITRIP threshold voltage | VITRIP | ITRIP(17) to $V_{SS}$(19) | Fig.5 | 0.44 | 0.49 | 0.54 | V |
| Pre-drive low voltage protection | UVLO | | - | 10 | - | 12 | V |
| FAULT terminal input electric current | IOSD | VFAULT = 0.1 V | - | - | 1.5 | - | mA |
| FAULT clearance delay time | FLTCLR | From time fault condition clear | - | 1.0 | - | 3.0 | ms |
| Thermistor for substrate temperature monitor | Rt | Resistance between the TH1 and TH2 terminals | - | 90 | - | 110 | kΩ |
| **Switching character** | | | | | | | |
| Switching time | tON | Io = 50 A, Inductive load | Fig.6 | - | 0.7 | 1.5 | μs |
| | tOFF | | | - | 1.1 | 2.1 | μs |
| Turn-on switching loss | Eon | Io = 50 A, $V_{CC}$ = 300 V, VD = 15 V, L = 280 μH | | - | 1100 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 1200 | - | μJ |
| Total switching loss | Etot | | | - | 2300 | - | μJ |
| Turn-on switching loss | Eon | Io = 50 A, $V_{CC}$ = 300 V, VD = 15 V, L = 280 μH, Tc = 100°C | | - | 1200 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 1350 | - | μJ |
| Total switching loss | Etot | | | - | 2550 | - | μJ |
| Diode reverse recovery energy | Erec | Io = 50 A, $V_{CC}$ = 300 V, VD = 15 V, L = 280 μH, Tc = 100°C | | - | 52.5 | - | μJ |
| Diode reverse recovery time | Trr | | | - | 104 | - | ns |

Reference Voltage is "$V_{SS}$" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

1. When the internal protection circuit operates, a FAULT signal is turned ON (When the FAULT terminal is low level, FAULT signal is ON state : output form is open DRAIN) but the FAULT signal does not latch. After protection operation ends, it returns automatically within about 1 ms to 3 ms and resumes operation beginning condition. So, after FAULT signal detection, set all input signal to OFF (Low) at once. How ever, the operation of pre-drive power supply low voltage protection (UVLO : with hysteresis about 0.2 V) is as follows.

   Upper side :
   The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'

   Lower side :
   The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M4 type screw, tightening torque range is 0.79 Nm to 1.17 Nm.

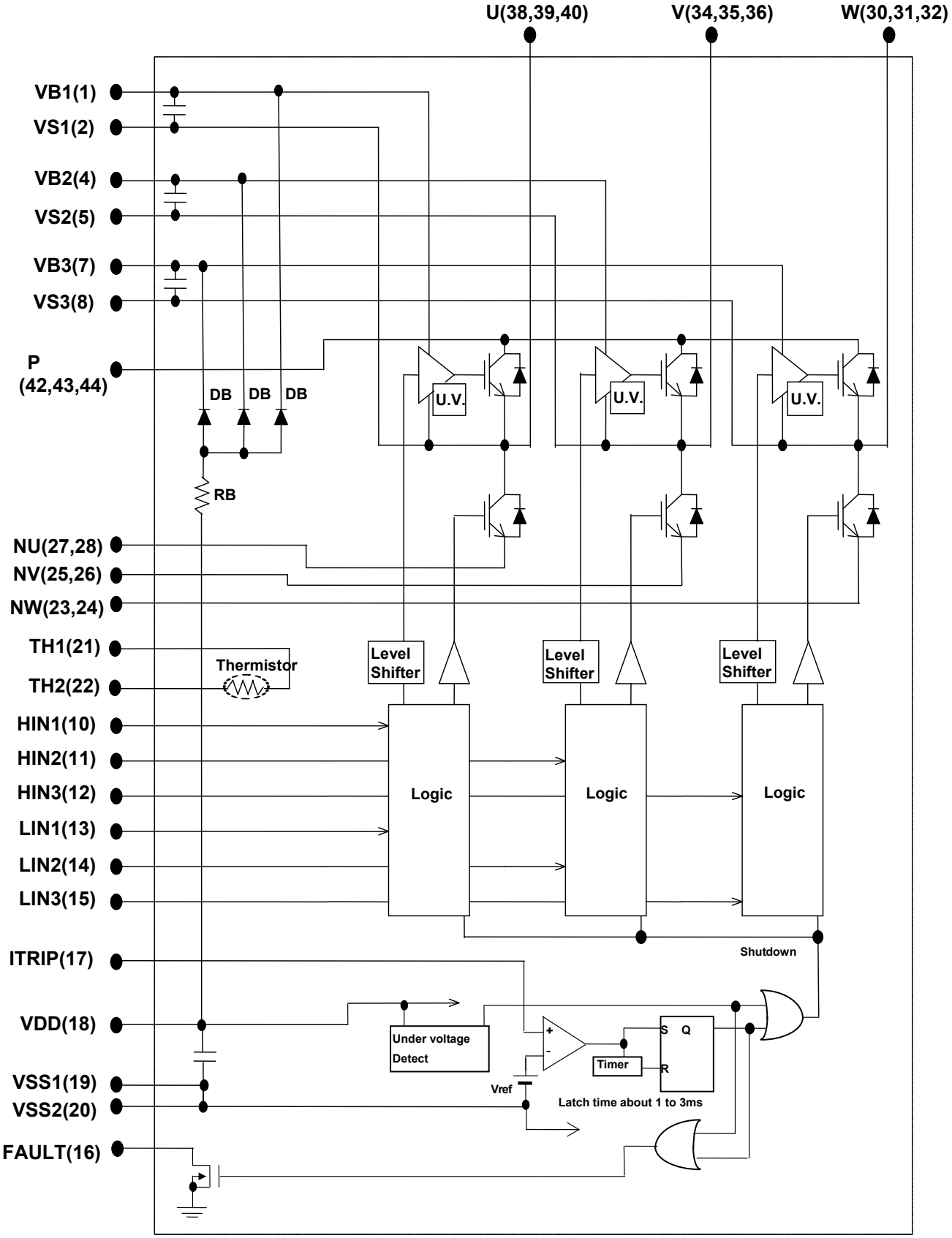
3. The pre-drive low voltage protection is the feature to protect a device when the pre-driver supply voltage falls due to an operating malfunction.

4. When use the over-current protection with external resistors, please set the current protection level to be equal or less than the rating of output peak current (Iop).

## Pin Assignment

| Pin No. | Name | Description | Pin No. | Name | Description |
|---|---|---|---|---|---|
| 1 | VB1 | High side floating supply voltage 1 | 44 | P | Positive bus input voltage |
| 2 | VS1 | High side floating supply offset voltage | 43 | P | Positive bus input voltage |
| 3 | - | Without pin | 42 | P | Positive bus input voltage |
| 4 | VB2 | High side floating supply voltage 2 | 41 | - | Without pin |
| 5 | VS2 | High side floating supply offset voltage | 40 | U | U+ phase output |
| 6 | - | Without pin | 39 | U | U+ phase output |
| 7 | VB3 | High side floating supply voltage 3 | 38 | U | U+ phase output |
| 8 | VS3 | High side floating supply offset voltage | 37 | - | Without pin |
| 9 | - | Without pin | 36 | V | V+ phase output |
| 10 | HIN1 | Logic input high side driver-Phase1 | 35 | V | V+ phase output |
| 11 | HIN2 | Logic input high side driver-Phase2 | 34 | V | V+ phase output |
| 12 | HIN3 | Logic input high side driver-Phase3 | 33 | - | Without pin |
| 13 | LIN1 | Logic input low side driver-Phase1 | 32 | W | W+ phase output |
| 14 | LIN2 | Logic input low side driver-Phase2 | 31 | W | W+ phase output |
| 15 | LIN3 | Logic input low side driver-Phase3 | 30 | W | W+ phase output |
| 16 | FAULT | Fault out | 29 | - | Without pin |
| 17 | ITRIP | Over-current protection level setting pin | 28 | NU | U- phase output |
| 18 | VDD | +15 V main supply | 27 | NU | U- phase output |
| 19 | VSS1 | Negative main supply | 26 | NV | V- phase output |
| 20 | VSS2 | Negative main supply | 25 | NV | V- phase output |
| 21 | TH1 | Thermistor out | 24 | NW | W- phase output |
| 22 | TH2 | Thermistor out | 23 | NW | W- phase output |

**Block Diagram**



## Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U− shows the lower side of the U phase)

### ■ $I_{CE}$ / IR(BD)

| | U+ | V+ | W+ | U- | V- | W- |
|---|---|---|---|---|---|---|
| M | 42 | 42 | 42 | 38 | 34 | 30 |
| N | 38 | 34 | 30 | 27 | 25 | 23 |

| | U(BD) | V(BD) | W(BD) |
|---|---|---|---|
| M | 1 | 4 | 7 |
| N | 19 | 19 | 19 |

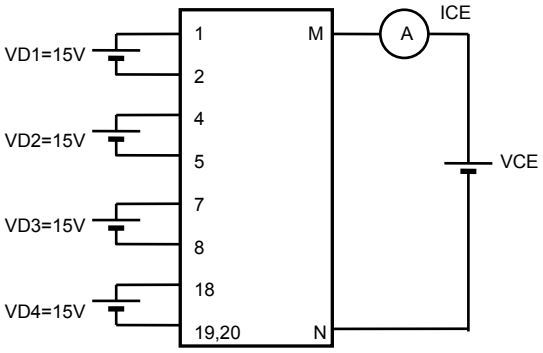



Fig.1

### ■ $V_{CE}$(sat) (Test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|---|---|---|---|---|---|
| M | 42 | 42 | 42 | 38 | 34 | 30 |
| N | 38 | 34 | 30 | 27 | 25 | 23 |
| m | 10 | 11 | 12 | 13 | 14 | 15 |

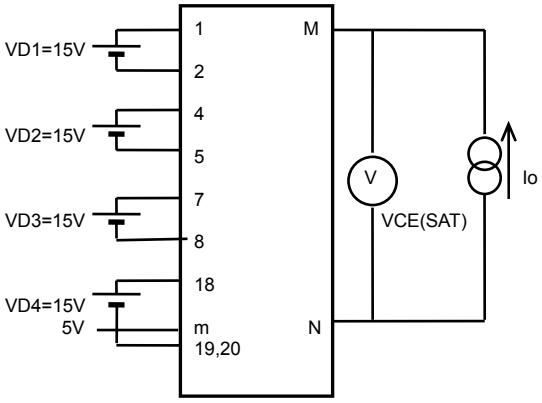



Fig.2

### ■ VF (Test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|---|---|---|---|---|---|
| M | 42 | 42 | 42 | 38 | 34 | 30 |
| N | 38 | 34 | 30 | 27 | 25 | 23 |

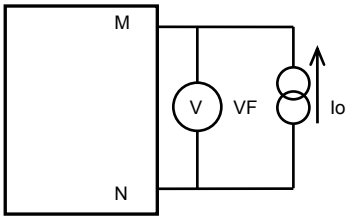



Fig.3

### ■ ID

| | VD1 | VD2 | VD3 | VD4 |
|---|---|---|---|---|
| M | 1 | 4 | 7 | 18 |
| N | 2 | 5 | 8 | 19 |

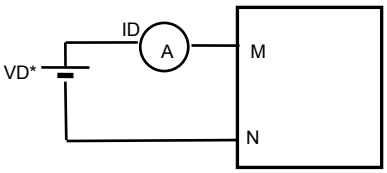
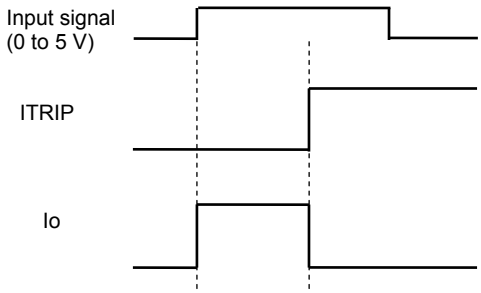



Fig.4

■ **ISD (The circuit is a representative example of the lower side U phase)**



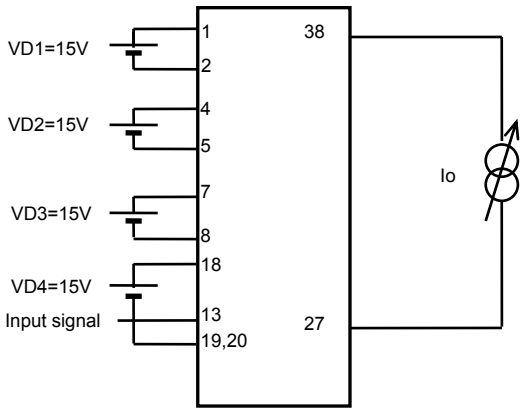
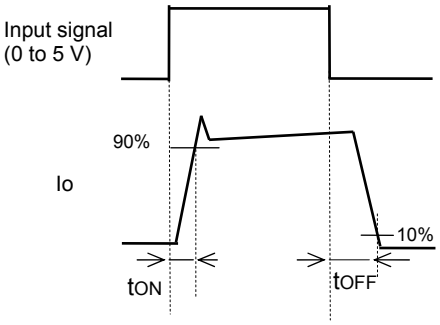




Fig.5

■ **Switching time (The circuit is a representative example of the lower side U phase)**



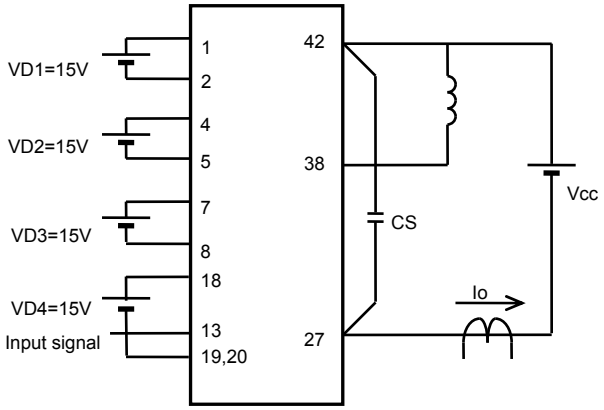
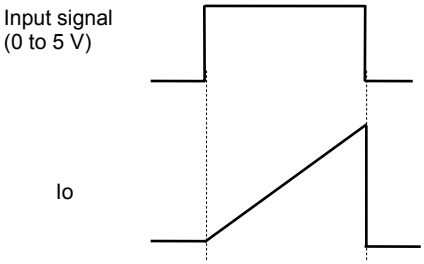




Fig.6

■ **RB-SOA (The circuit is a representative example of the lower side U phase.)**



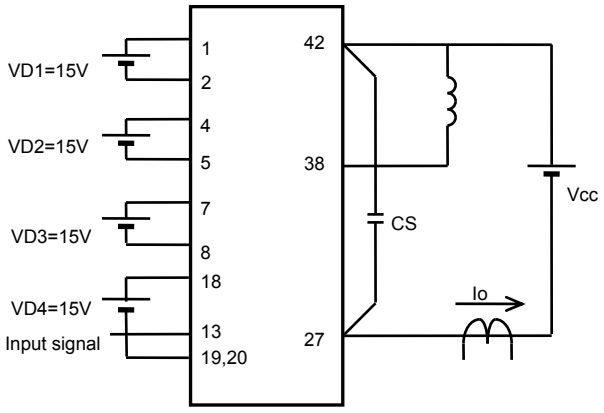




Fig.7

**Input / Output Timing Chart**

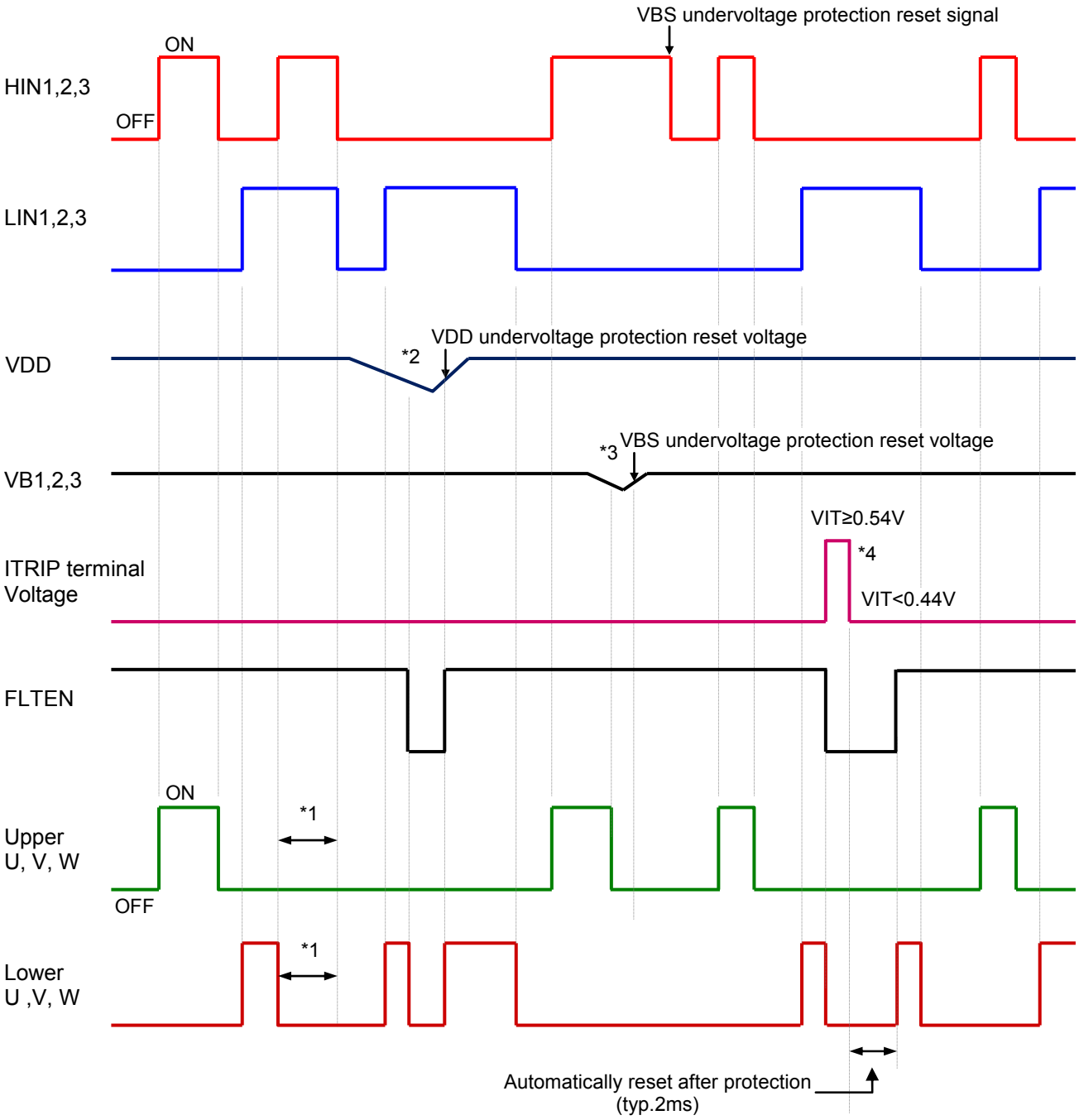



Fig. 8

Notes

*1 : Diagram shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.

*2 : When $V_{DD}$ decreases all gate output signals will go low and cut off all 6 IGBT outputs. When $V_{DD}$ rises the operation will resume immediately.

*3 : When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.

*4 : When VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 2 ms (typ) after over current condition is removed.

**Logic level table**

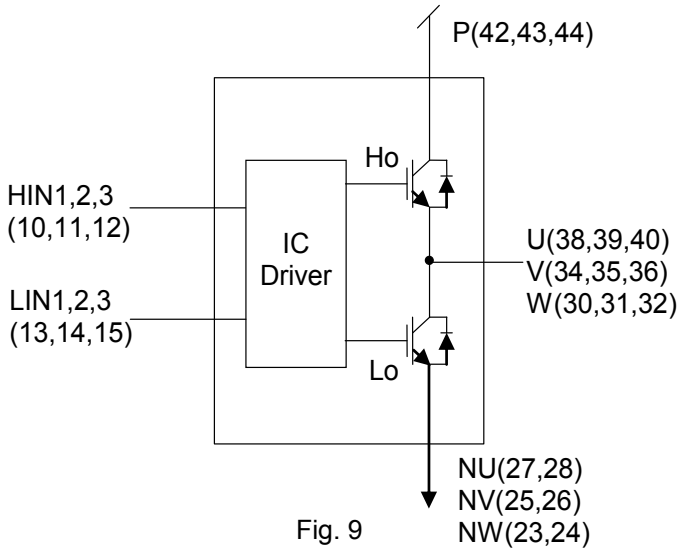



Fig. 9

| FLTEN | Itrip | HIN1,2,3 | LIN1,2,3 | U,V,W |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | Vbus |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | Off |
| 1 | 0 | 1 | 1 | Off |
| 1 | 1 | X | X | Off |
| 0 | X | X | X | Off |

**Application Circuit Example**

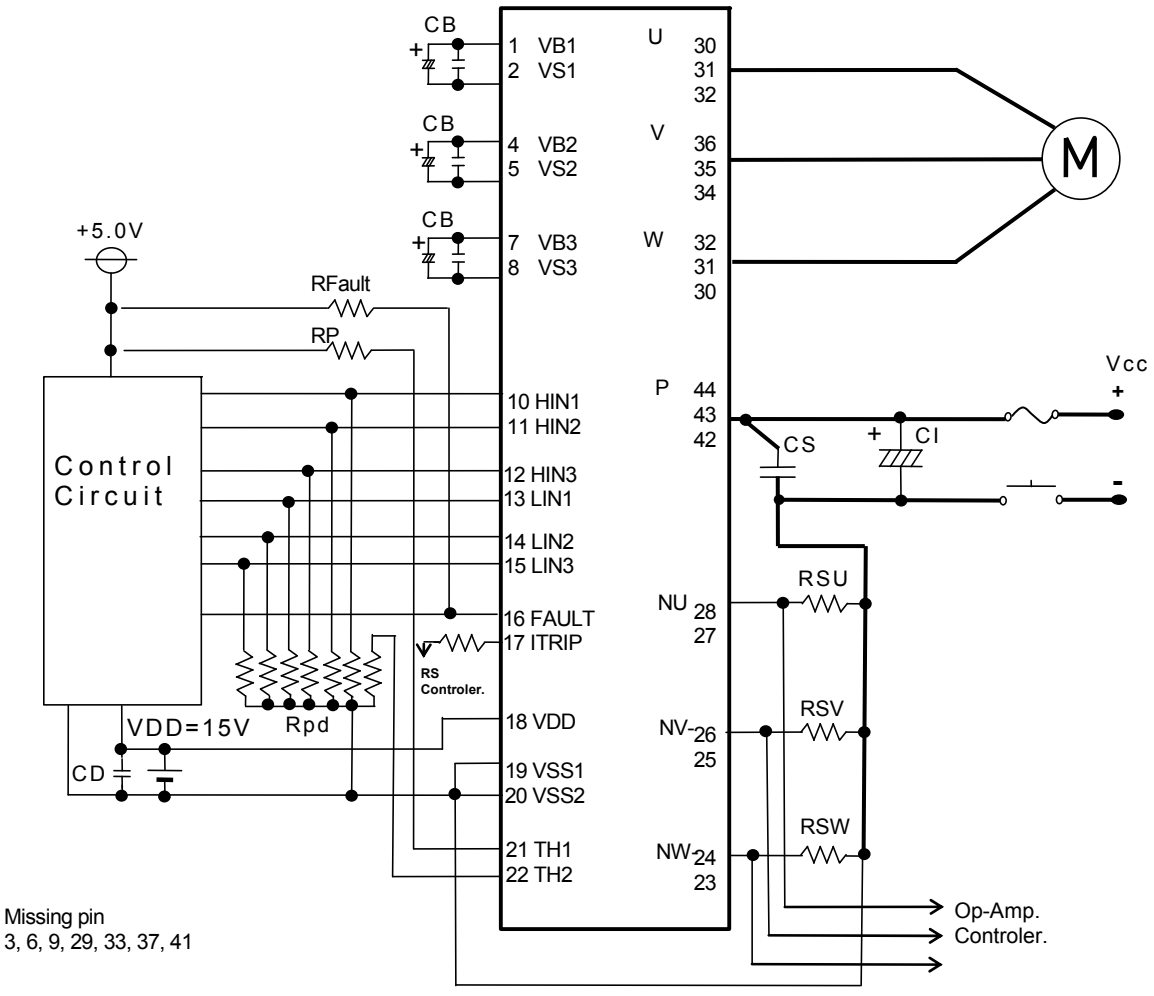



Fig. 10

**Recommended Operating Conditions** at Tc = 25°C

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{CC}$ | P to NU,NV,NW | 0 | 280 | 400 | V |
| Pre-driver supply voltage | VD1, 2, 3 | VB1 to VS1, VB2 to VS2, VB3 to VS3 | 12.5 | 15 | 17.5 | V |
| | VD4 | $V_{DD}$ to $V_{SS}$ *1 | 13.5 | 15 | 16.5 | |
| Input ON voltage | VIN(ON) | HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 | 3.0 | − | 5.0 | V |
| Input OFF voltage | VIN(OFF) | | 0 | − | 0.3 | |
| PWM frequency | fPWM | | 1.0 | − | 20 | kHz |
| Dead time | DT | Upper/lower input signal downtime | 2 | − | − | μs |
| Allowable input pulse width | PWIN | ON pulse width/OFF pulse width | 1 | − | − | |
| Tightening torque | MT | 'M4' Type Screw | 0.79 | − | 1.17 | Nm |

*1 Pre-driver power supply (VD4 = 15 ±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5 A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## Usage Precautions

1. This IPM includes internal bootstrap diodes and resistors. By adding a bootstrap capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF (±20%), however this value needs to be verified prior to production. If selecting the capacitance more than 47 μF (±20%), connect a resistor (about 40 Ω) in series between each 3-phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor. When not using the bootstrap circuit, each upper side pre-drive power supply requires n external independent power supply.

2. It is essential that wirning length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 μF.

3. "FAULT" (pin 16) is open DRAIN output terminal (Active Low). Pull up resistor is recommended more than 5.6 kΩ.

4. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between "TH1" and "TH2" . Generally, one of terminals is connected to $V_{SS}$, and the other is pulled up to external power supply with pull-up resistor (Rp) externally. The temperature monitor example application is as follows please refer the Fig.11 and Fig.12 below.

5. The pull-down resistor 33 kΩ is provided internally at the signal input terminals. An external resistor of 2.2 kΩ to 3.3 kΩ should be added to reduce the influence of external wiring noise.

6. As protection of IPM to unusual current by a short circuit etc, it recommended installing shunt resistors and an over-current protection circuit outside. Moreover, for safety, a fuse on Vcc line is recommended.

7. Disconnection of terminals U, V, W, during normal motor operation will cause damage to IPM, use caution with this connections.

8. The "ITRIP" terminal (pin 17) is the input terminal to shut down. When VITRIP exceeds threshold (0.44 V to 0.54 V), all IGBTs are turned off. And normal operation resumes 2 ms (typ) after over current condition is removed. Therefore, please turn all the input signal off (Low) in case of detecting error at the "FAULT" terminal.

9. When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

**The characteristic of thermistor**

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Resistance | $R_{25}$ | Tc = 25°C | 97 | 100 | 103 | kΩ |
| Resistance | $R_{100}$ | Tc = 100°C | 4.93 | 5.38 | 5.88 | kΩ |
| B-Constant (25 to 50°C) | B | | 4165 | 4250 | 4335 | K |
| Temperature Range | | | −40 | | +125 | °C |

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

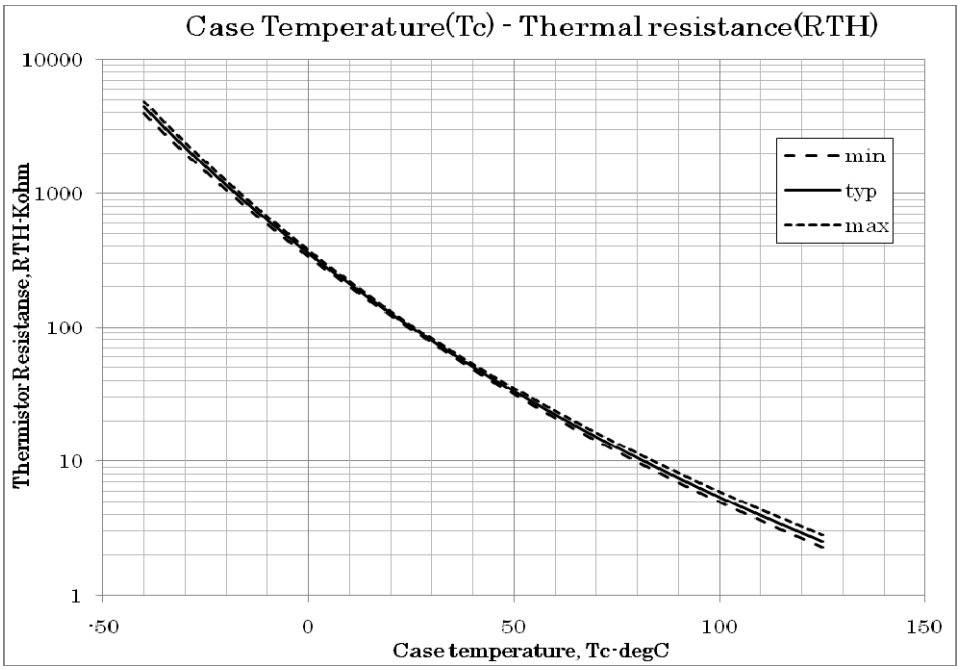



Fig.11 Variation of thermistor resistance with temperature

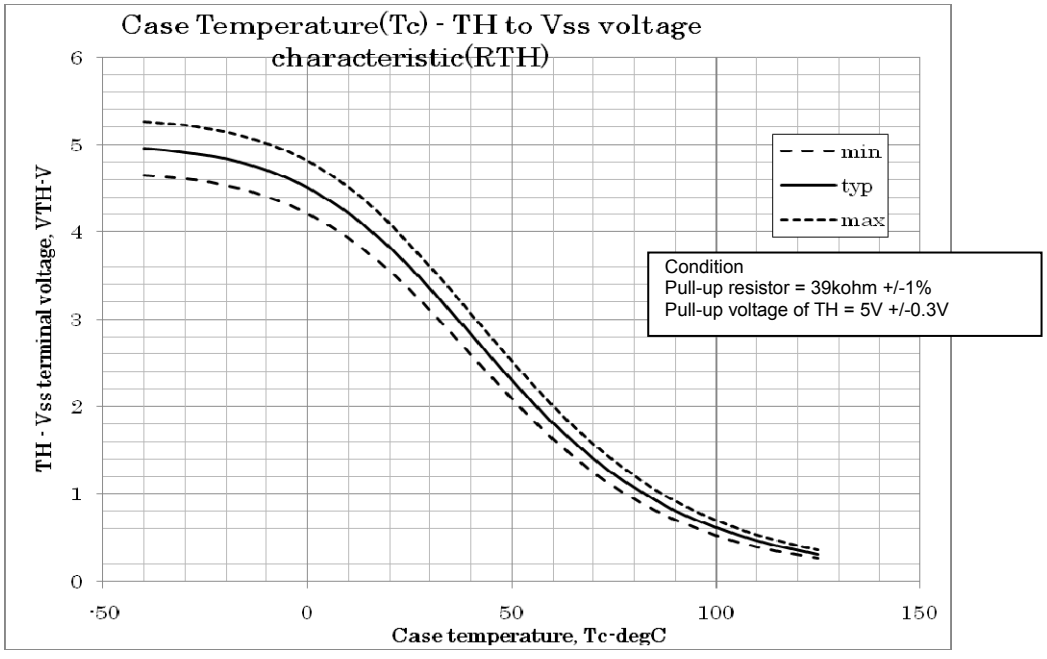



Fig.12 Variation of temperature sense voltage with thermistor temperature

**Io-f curve**

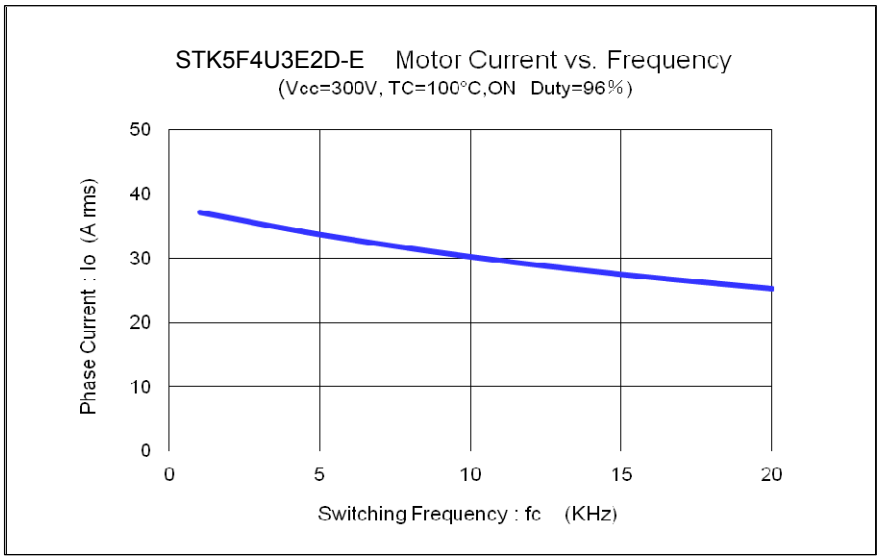
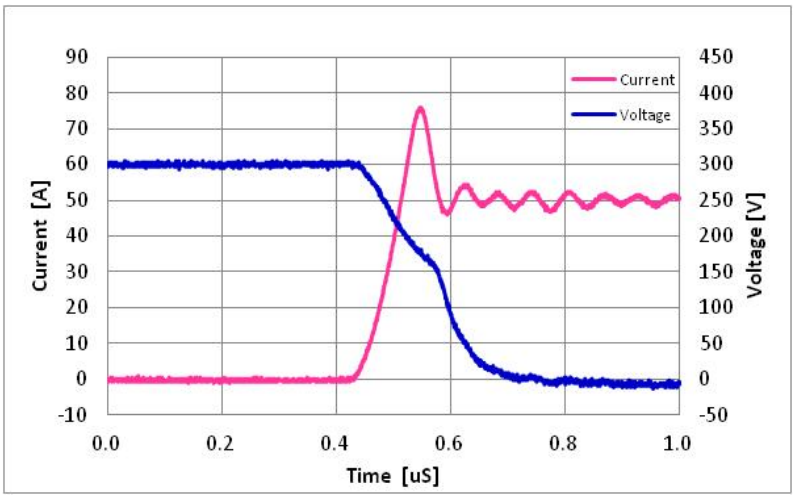


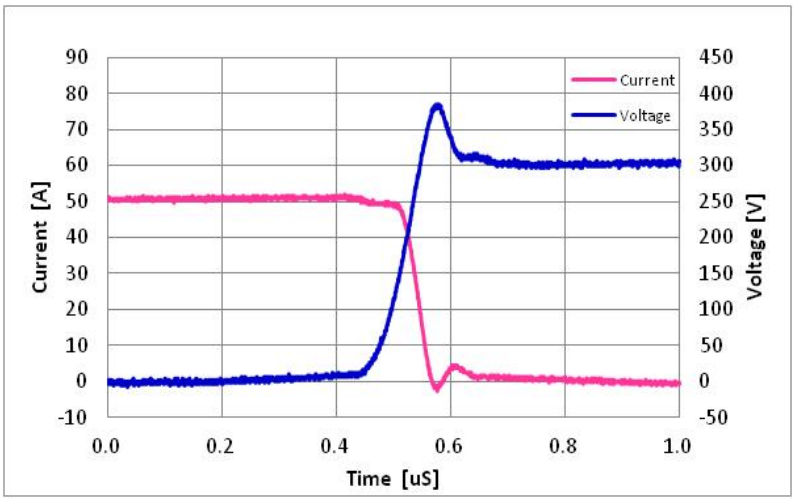

Fig.13 Maximum sinusoidal phase current as function of switching frequency at Tc = 100°C, $V_{CC}$ = 300 V

**Switching waveform**




Turn on

Fig. 14 IGBT Turn-on. Typical turn-on waveform at Tc = 100°C, $V_{CC}$ = 300 V, Ic = 50 A




Turn off

Fig. 15 IGBT Turn-off. Typical turn-off waveform at Tc = 100°C, $V_{CC}$ = 300 V, Ic = 50 A

## Capacitor value calculation for Boot strap (Cb)

### Calculate condition

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Upper side power supply | VBS | 15 | V |
| Total gate charge of output power IGBT at 15 V | Qg | 0.9 | μC |
| Upper side power supply low voltage protection | UVLO | 12.5 | V |
| Upper side power dissipation | IDMAX | 120 | μA |
| ON time required for CB voltage to fall from 15 V to UVLO | TONMAX | – | s |

### Capacitance calculation formula

TONMAX is upper arm maximum on time equal the time when the CB voltage falls from 15 V to the upper limit of Low voltage protection level.
“ton-maximum" of upper side is the time that CB decreases 15 V to the maximum low voltage protection of the upper side (12 V).
Thus, CB is calculated by the following formula.

VD x CB – Qg – IDMAX * TONMAX = UVLO * CB
CB = (Qg + IDMAX * TONMAX) / (VD – UVLO)

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production.

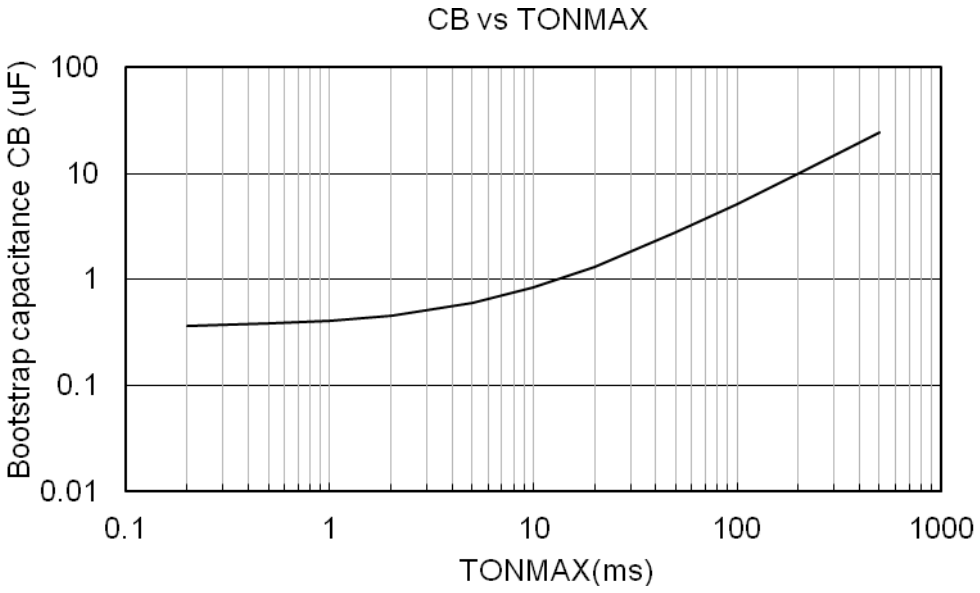
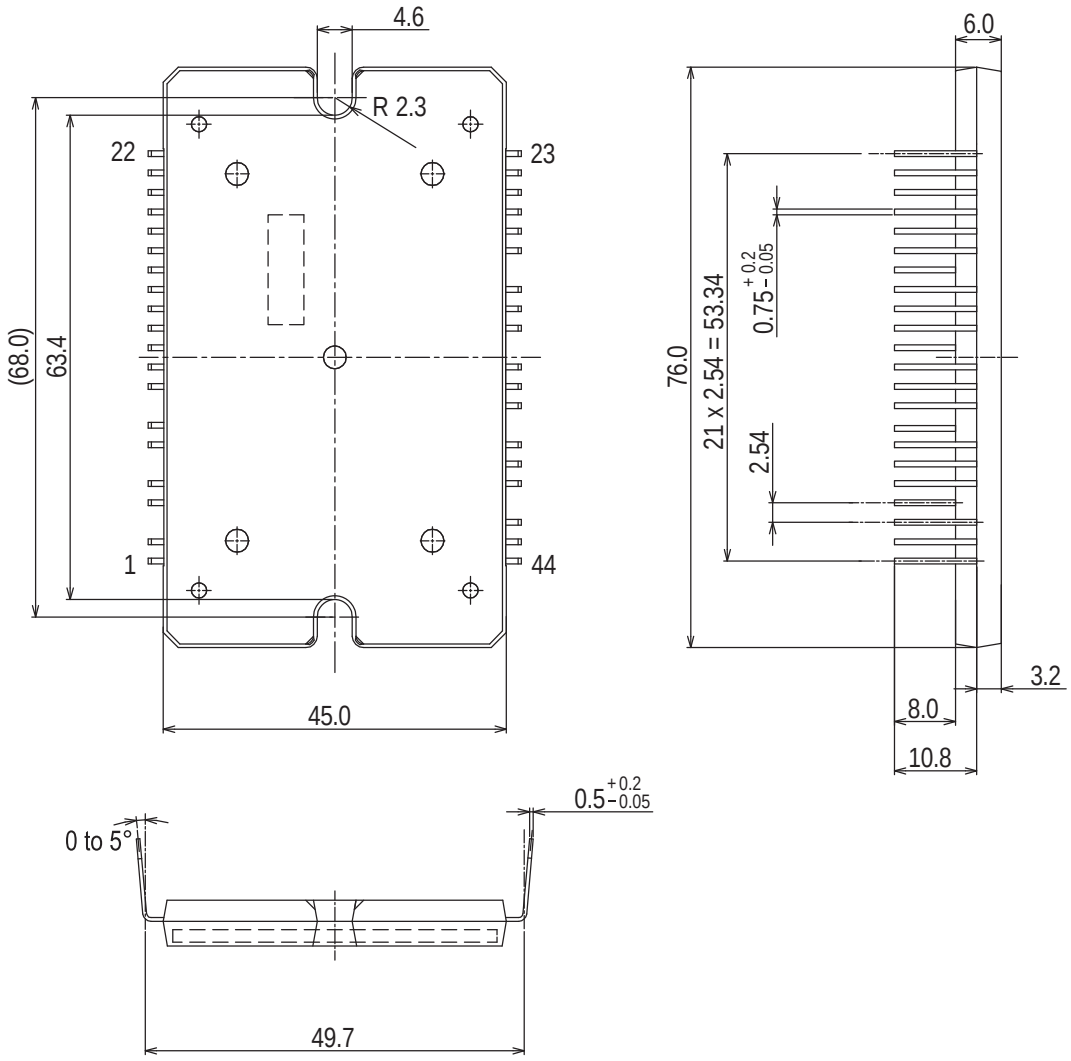



Fig.16 TONMAX vs CB characteristic

**PACKAGE DIMENSIONS**
unit : mm

**HYBRID INTEGRATED MODULE**
CASE MODAW
ISSUE O

**Missing Pin : 3,6,9,29,33,37,41**



## ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---|---|---|
| STK5F4U3E2D-E | MODAW / 610AC-DIP4-UL (Pb-Free) | 6 / Tube |

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