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AUTOMOTIVE ADAS PREREGULATOR
STR-ADAS-PREREGULATOR-GEVK
Test Report

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Introduction

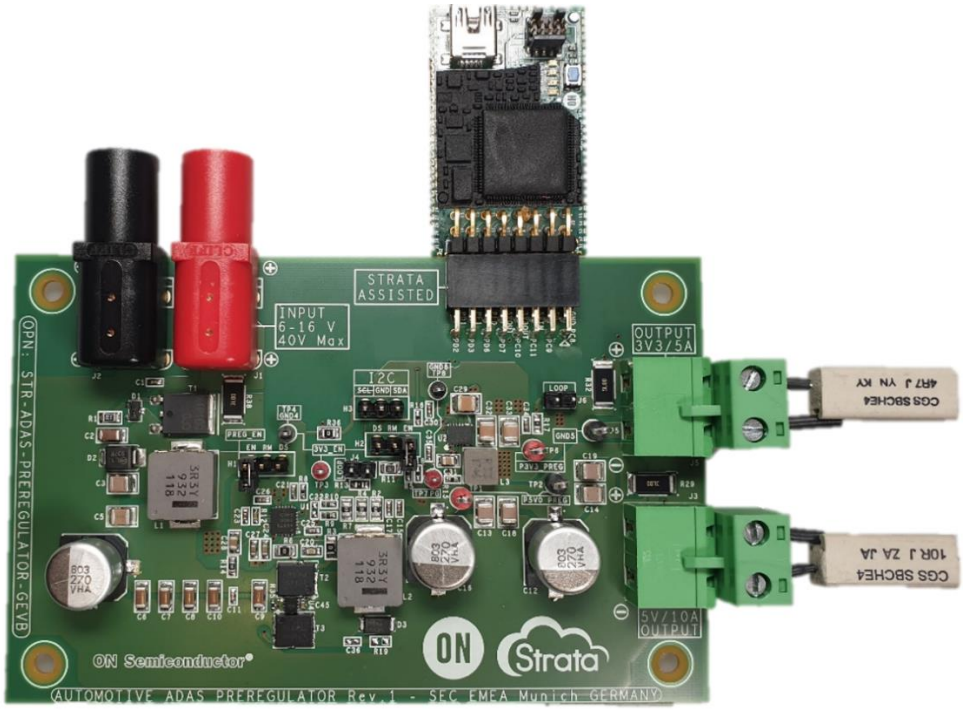
The Strata Assisted STR-ADAS-PREREGULATOR-GEVK provides an evaluation kit for the NCV881930 Synch Buck Controller and for the NCV6357 configurable 5.0 A Adaptive-On-Time (AOT) Step Down Converter a with I2C programmable output voltage from 0.6 V to 3.3 V in 12.5 mV steps. The NCV6357 also offers multiple operating modes: PFM for low load, Pseudo-PWM (PWM) for medium to high load, and forced PPWM which can be set by the operator. The evaluation kit is rated for automotive applications. This evaluation kit can be used in tandem with the Strata environment GUI to enable/disable the DC-DC converter, change the operating mode, and monitor other telemetry including interrupts, input/output voltage, power dissipated, and temperature.

Features

- **Vin range from 6.0 .. 16.0 V, 40.0 V peak**
  - **Output 1 5.0 V @ 10.0 A peak**
    - **NCV881930 Synchronous Buck Controller + NVMFS5C460NL 40 V Dual N-FET**
  - **Output 2 3.3 V @ 5.0 A peak**
    - **NCV6357MTWDTXG Step Down Converter, AOT, Configurable 5.0 A**
- **NCV6357MTWDTXG Programmable Vout from 0.6V to 3.3V in 12.5mV steps**
- **NCV6357MTWDTXG Adaptive-On-Time (AOT)**
- **NCV6357MTWDTXG Operation at up to 2.4MHz switching frequency**
- **NCV6357MTWDTXG Both PFM and PPWM operation with automatic transition for Optimum Efficiency**
- **NCV6357MTWDTXG 3.0 x 4.0 mm DFN-14 package**
- **Automotive and industrial rated AEC−Q100 Qualified and PPAP Capable**

Applications

- **DC-DC Power**
- **Advanced driver-assistance systems (ADAS).**
- **Automotive POL**
- **Instrumentation**



Test Report

This section will report important results and measurements from testing the **Strata Assisted STR-ADAS-PREREGULATOR-.**

1. Startup & Shutdown

The startup waveform at 12.0 V input voltage and no load is shown as follows:

Channel C1 **12.0 V Input Voltage**
2 V/div, 2 ms/div

Channel C2 **5.0 V Output Voltage**
2 V/div, 2 ms/div

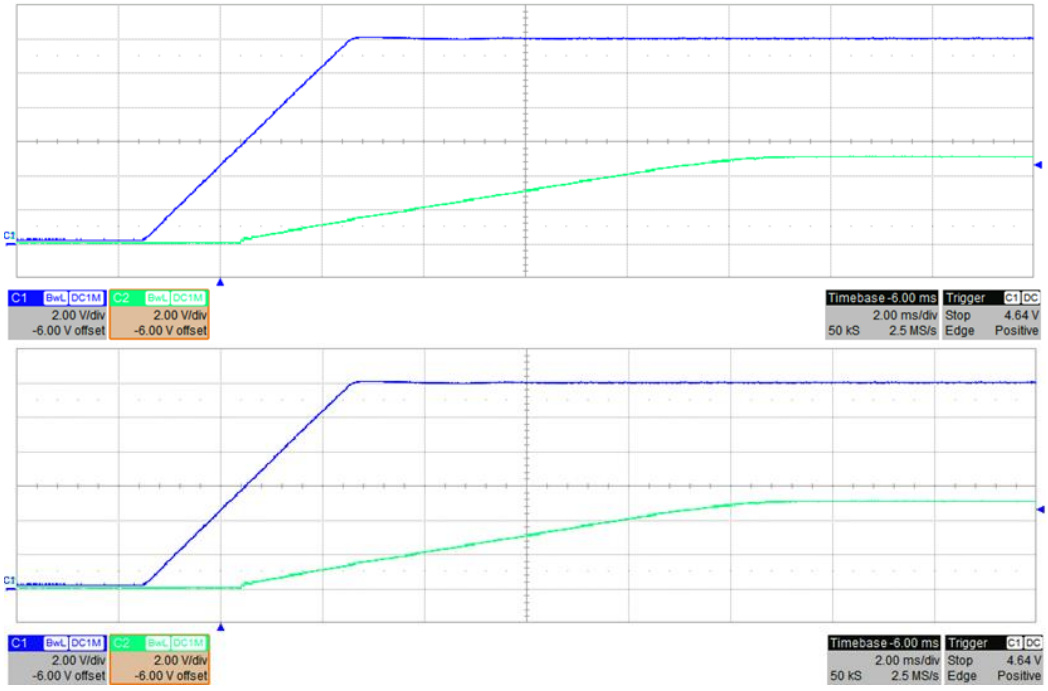


Figure 1

The shutdown waveform at 12.0 V input voltage and 6.0 A load is shown in

Figure 2.

Channel C1 **12.0 V Input Voltage**
2 V/div, 1 ms/div

Channel C1 **5.0 V Output Voltage**
2 V/div, 1 ms/div

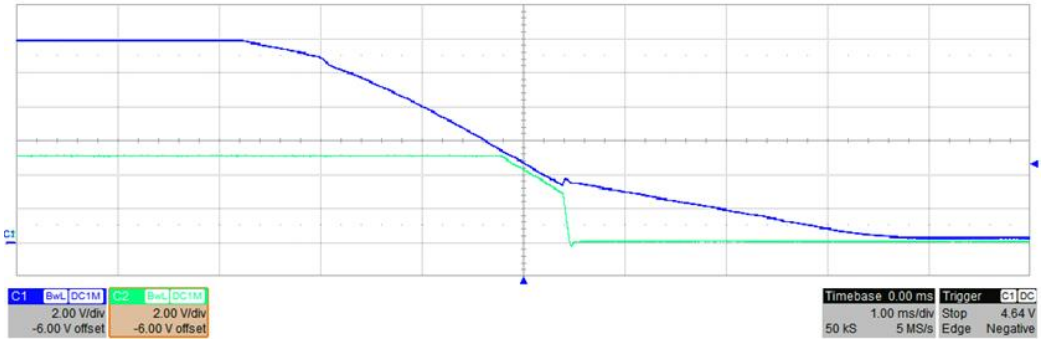


Figure 2

2. Efficiency

The efficiency and load regulation for **continuous synchronous mode** are shown in Figure 3 and Figure 4. **This measurement take into account the losses of the input filter**. VCCEXT is connected to VOUT.

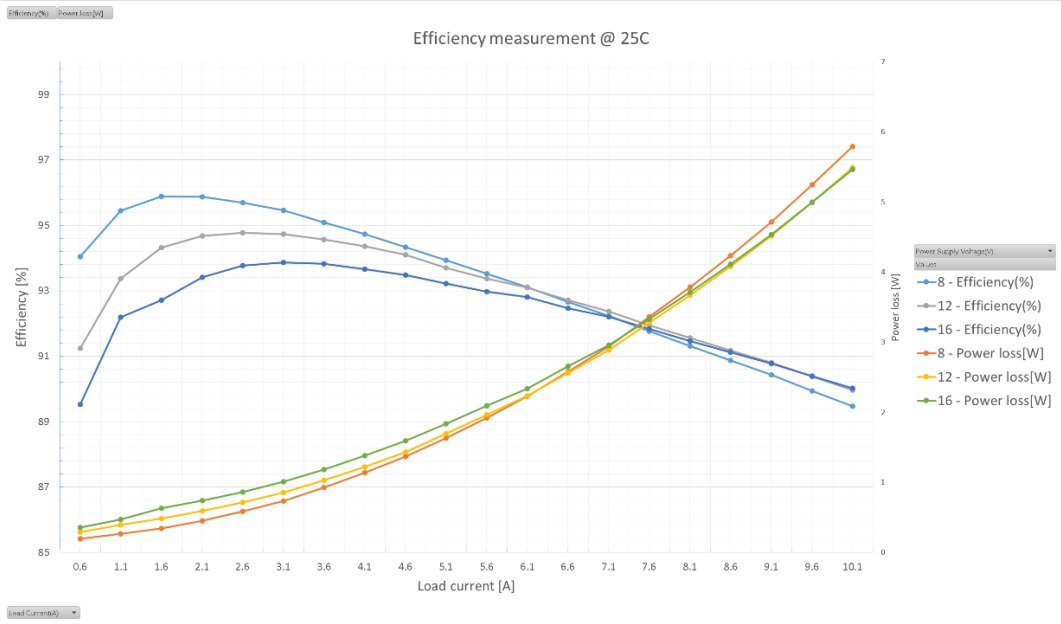


Figure 3

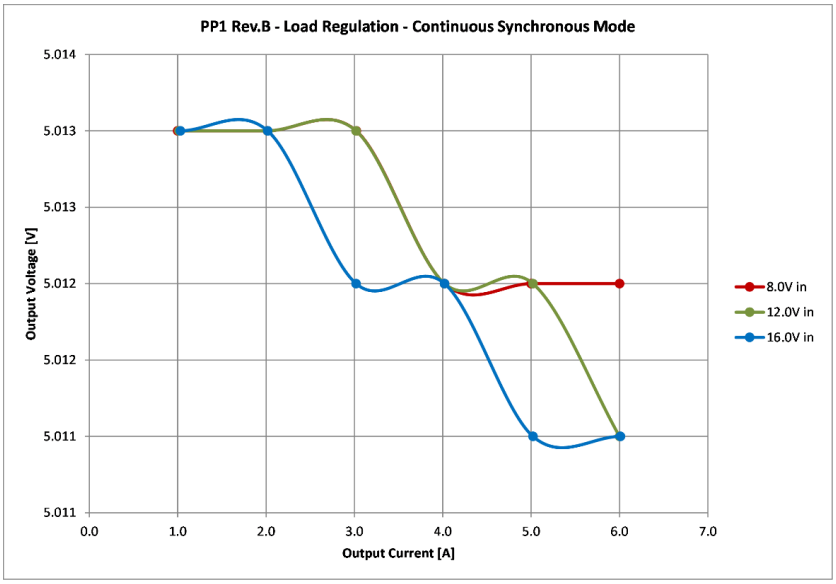


Figure 4

The efficiency and load regulation for **low I_q mode** are shown in Figure 5 and Figure 6. This measurement doesn't take into account the losses of the input filter.
VCCEXT is connected to VOUT.

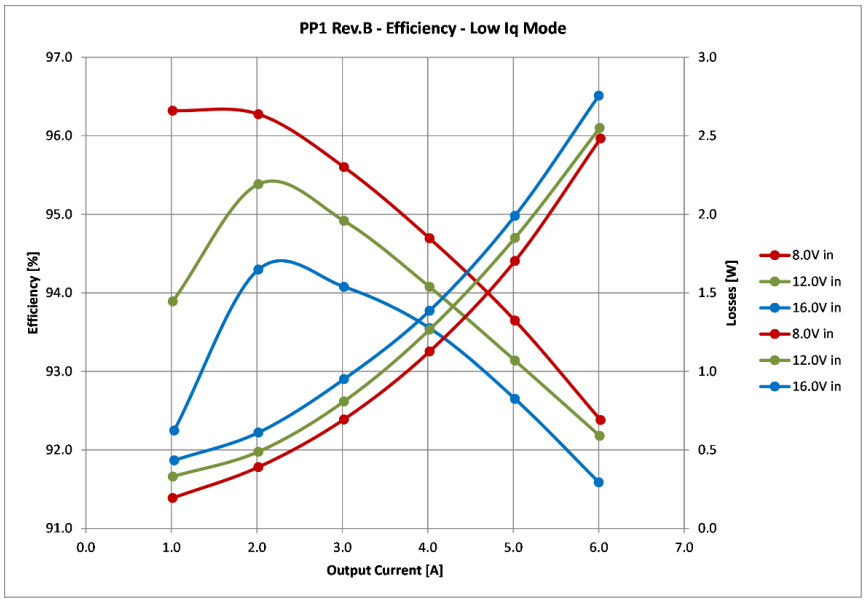


Figure 5

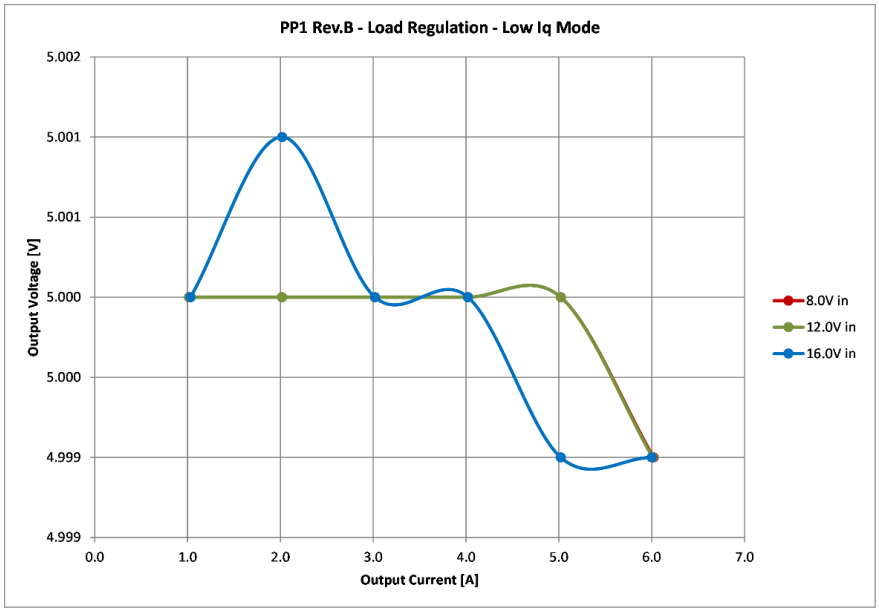


Figure 6

3. Transient Response

The response to a load step at 12.0 V input voltage is shown in Figure 7.

Channel C1 **Output Current**, Load Step 3.0 A to 6.0 A
2 A/div, 1 ms/div

Channel C2 **Output Voltage**, -111 mV undershoot (2.3 %), 112 mV overshoot (2.3 %)
100 mV/div, 1 ms/div, AC coupled

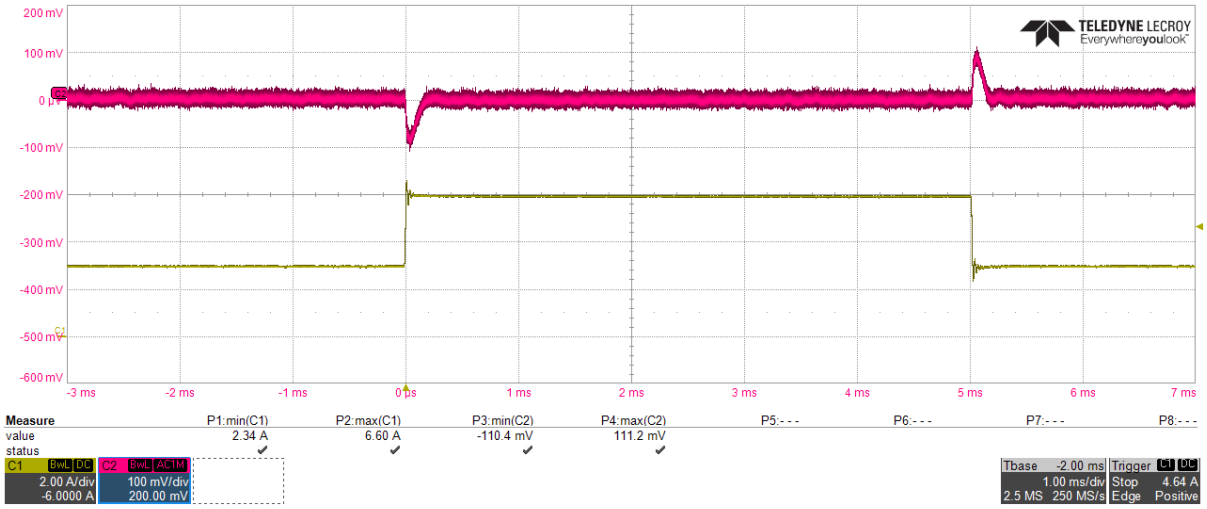


Figure 7

4. Frequency Response

The frequency response at 12.0 V input voltage and 6.0 A load is shown in Figure 8.

19.7 kHz bandwidth, 81 deg phase margin, -19 dB gain margin

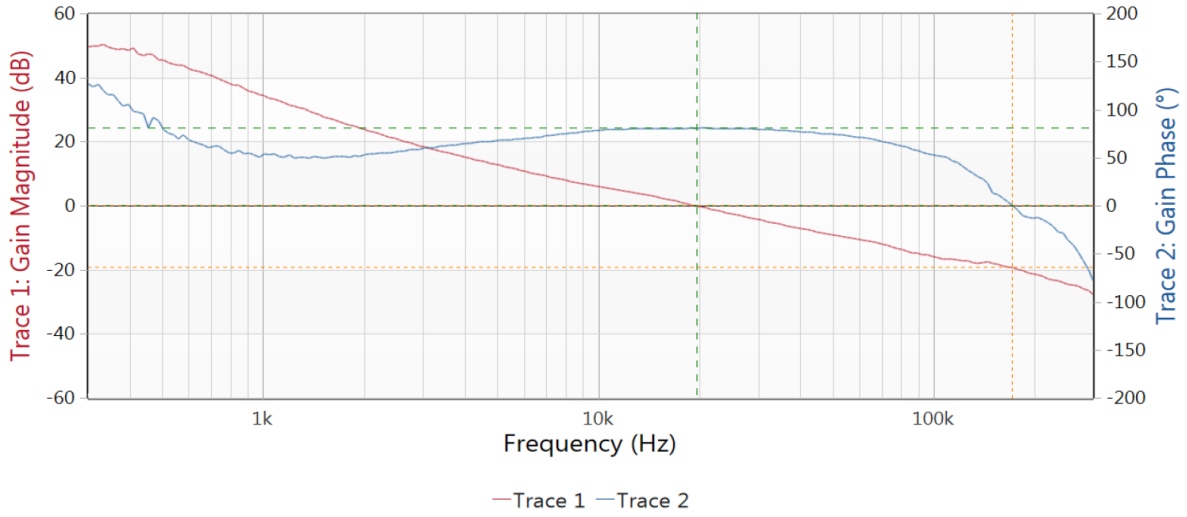


Figure 8

5. Input Ripple

The ripple voltage on C2 (connector) at 12.0 V input voltage and 6.0 A load is shown in

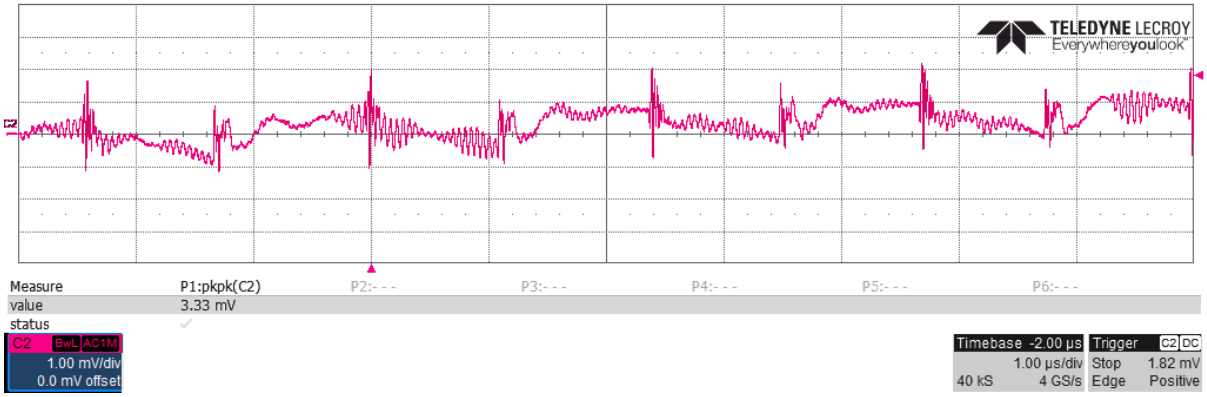


Figure 9.

Channel C2 **Input Voltage**, 1.1 mV peak-peak (0.01 %) ripple, 3.3 mV peak-peak (0.03 %) spikes
2 mV/div, 1 us/div, AC coupled

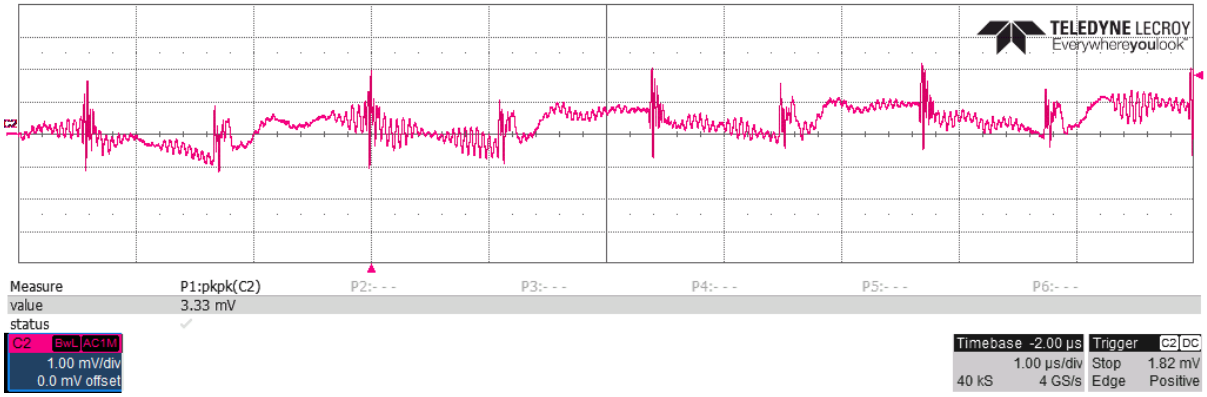


Figure 9

The ripple voltage on C1 (C9 on current board) (buck input) at 12.0 V input voltage and 6.0 A load is shown in

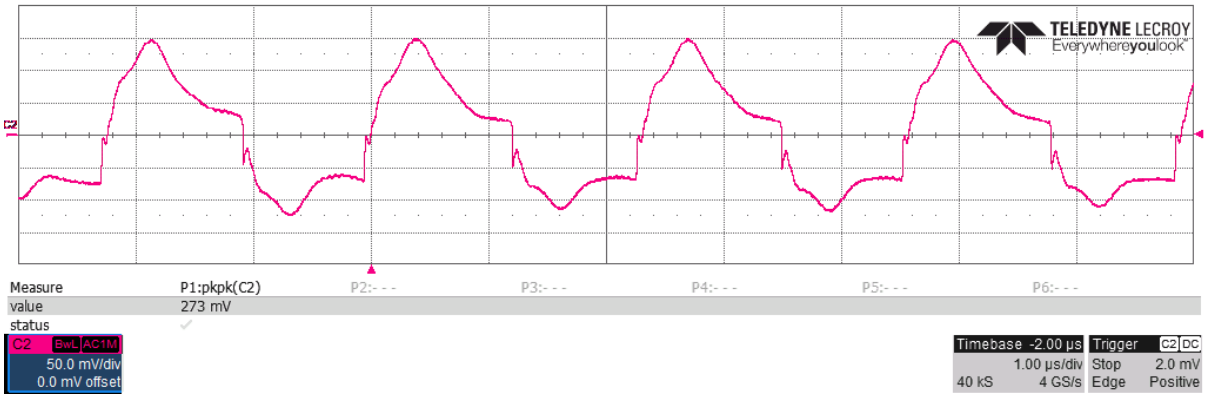


Figure 10.

Channel C2 **Input Voltage**, 270 mV peak-peak (2.3 %)
50 mV/div, 1 us/div, AC coupled

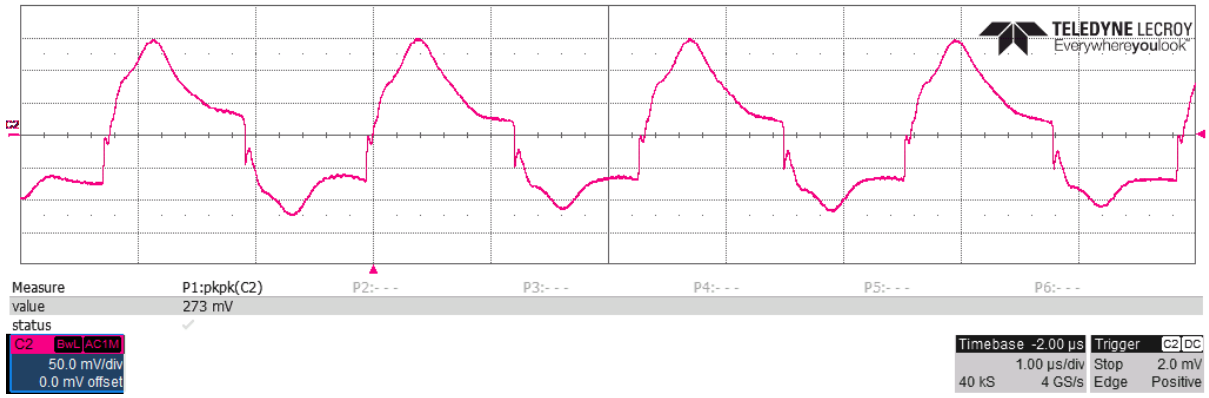


Figure 10

6. Output Ripple

The output ripple (at C13) voltage 12.0 V input voltage and 6.0 A load is shown in Figure 11.

Channel C2 **Output Voltage**, 12 mV peak-peak (0.3 %) ripple, ~~25 mV peak-peak (0.5 %) spikes~~
5 mV/div, 1 us/div, AC coupled

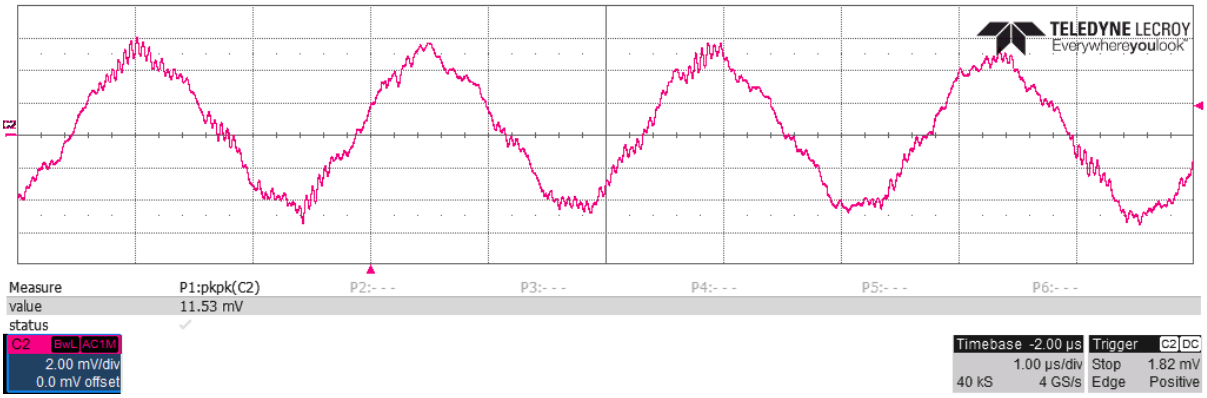


Figure 11

7. Low-Side FET (Switching Node)

The drain-source voltage of the low-side FET at 12.0V input voltage and 6.0A load is shown in Figure 12.

Channel C2 **Drain-Source Voltage**, -2.2 V minimum, 12.7 V maximum
5 V/div, 500 ns/div

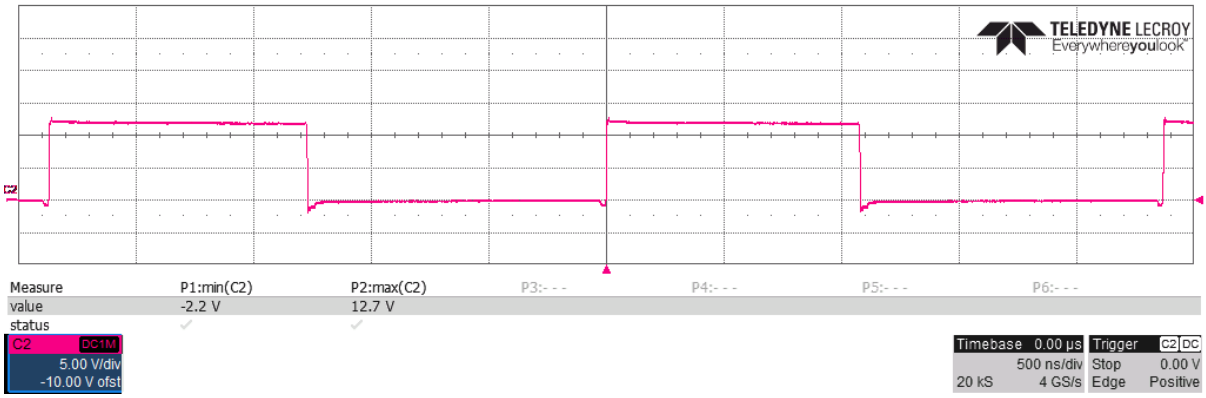

TELEDYNE LECROY
Everywhereyoulook
Measure
P1:min(C2)
P2:max(C2)
P3:- - -
P4:- - -
P5:- - -
P6:- - -
value
-2.2 V
12.7 V
status
C2
DC1M
5.00 V/div
-10.00 V ofst
Timebase 0.00 µs
500 ns/div
20 kS
4 GS/s
Trigger
C2 DC
Stop
0.00 V
Edge
Positive

Figure 12

8. Thermal Image

The thermal image (Figure 13) shows the circuit at an ambient temperature of 24 °C with an input voltage of 12.0 V and **5.0 A** load.

FET Q1: 51 °C, Inductor L2: 49 °C

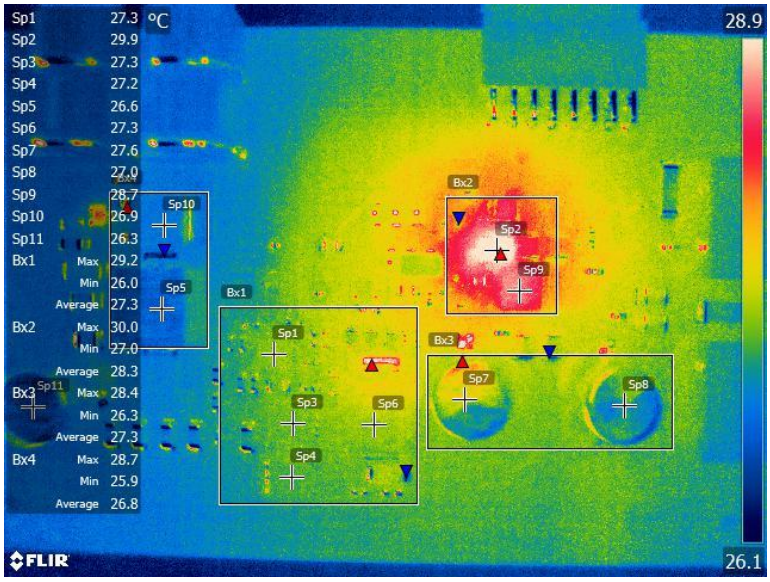


Figure 13

The thermal image (Figure 14) shows the circuit at an ambient temperature of 24 °C with an input voltage of 12.0 V and **10.0 A** load.

FET Q1: 110 °C, Inductor L2: 101 °C

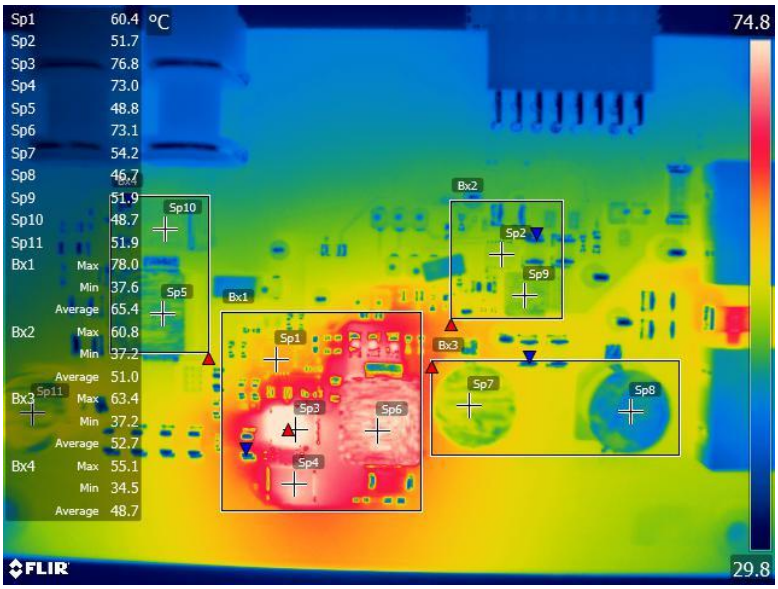


Figure 14

9. Schematic

Figure 15a

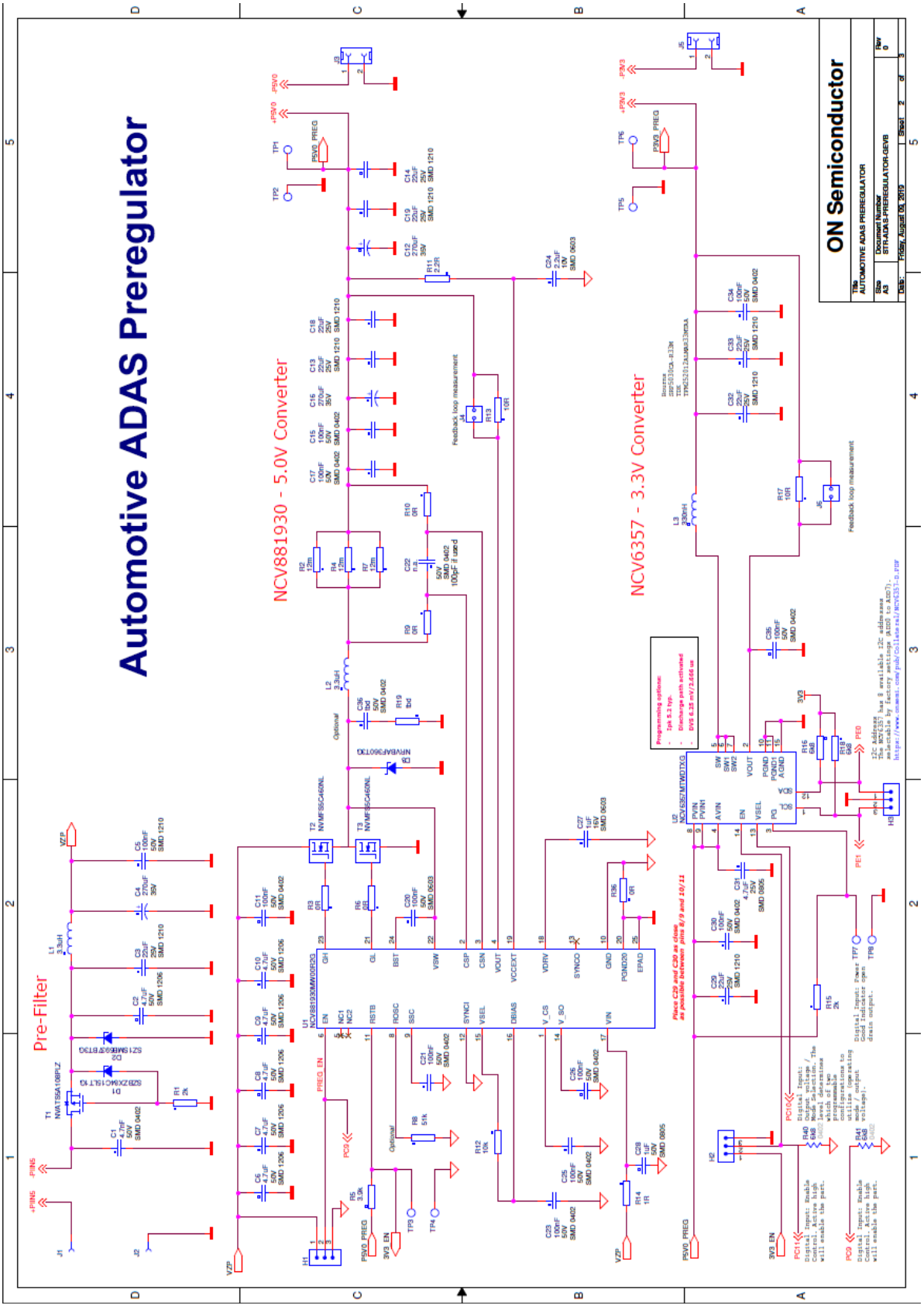
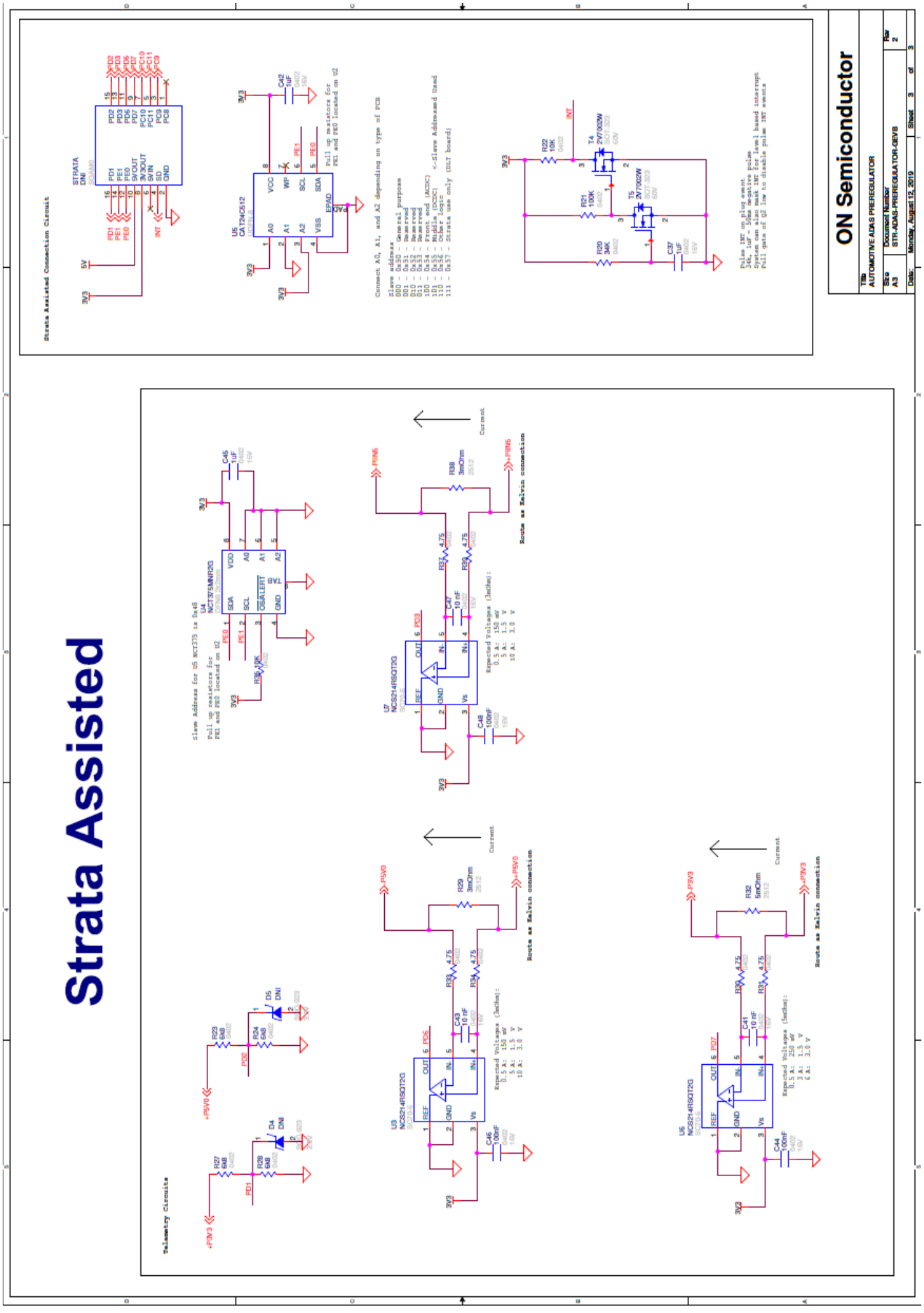


Figure 16b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