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STR-FUSB3307MPX-PPS-GEVK
Test Report

June 2020- Rev. 0

Contents

Introduction

The Strata enabled FUSB3307 EVB offers an easy to use User Interface (UI) within the Strata Developer Studio. Through the Strata UI, the developer can control some of the parts features as well as access the most up to date datasheets, BOMs, schematics and other collateral. This document will provide important measurements taken using the FUSB3307 EVB.

Device Features

- PD 3.0 v1.2 and Type-C r1.4 Compliant
- Constant Voltage (CV) and Constant Current Limit (CL) Regulation
- Small Current Sensing Resistor (5 m) for High Efficiency
- Gate Driver for N−Channel MOSFET as a Load Switch
- CC1/CC2 Pin Protection up to 26 V
- Built−in Cable−Drop Compensation
- Selectable Resistor Divider or Battery Charging (BC1.2) Modes
- Built−in Output Capacitor Bleeding Function for Fast Discharge
- Adaptive UVP, Adaptive OVP, OTP and VBUS Fault Detection

Applications

- Battery Wall Chargers for Tablet PC’s and Laptops
- AC-DC PD3.0 Compliant Adapters
- DC-DC Car Chargers for Individual Port Power Control

Descriptions for the evaluation board test points

VBAT
VBAT is the input DC voltage to power the evaluation board. It must be between 4.5V and 32V.

V_IN
V_IN is the same as VBAT after the input filter.

VCC
VCC on the evaluation board is VCC for the NCV81599. It is not the same as VCC for the FUSB3307. This is a constant 5V output from the NCV81599 when VBAT is applied.

VBUS
VBUS, which is also the same as VCC for the FUSB3307, is the device operating power from primary side. The default initial VCC of the FUSB3307 is 5V (typical), with a valid range of 4.5V to 5.5V. The CATH pin is controlled to keep VCC in the valid range. The FUSB3307 VCC voltage sensing is used for OVP and UVP with an internal 1:9 resistor divider. The FUSB3307 VCC is also used for the FUSB3307 VCC current discharge function through an internal resistance, 22~25 ohms, when it's needed. After an explicit contract is established, the valid FUSB3307 VCC can be in the range of 3.3V-5% (3.135V) up to 21V+5% (22.05V) for the case of USB PD PPS contracts.

VDD
VDD is the internal 5V regulator output from the FUSB3307, and an external 1uF capacitor is required. The VDD is used for internal device power as well as VCONN supply when needed.

VBUSOUT
VBUSOUT is VBUS between the external NFET load switch and the Type-C receptacle and is also where a recommended external resistor, typically 39 ohms, is tied to the DISC pin for the VBUS discharge path. An internal path has 22 to 23 ohms in series with a switch.

GND
Evaluation board and device GND which is tied together with IS-. The IS- pin is tied to the FUSB3307 side of the current sense resistor. IS+ connects to ground sense return path, GND_SNS, from the Type-C receptacle.

GND_SNS
This is the return ground sense path from the Type-C receptacle. IS+ connects to this ground sense return path for sensing the sink load current.

IFB
This is a constant current amplifying signal. The voltage level on this point is the amplified current sense signal. This pin connects to the internal CC loop amplifier's non-inverting input terminal. Externally, the pin connects to the FUSB3307 VCC through a capacitor and resistor network, which contributes to the CATH pin current ramp.

VFB
This is the output voltage sensing voltage. This pin is for CV regulation, and connects to the internal CV loop amplifier non-inverting input terminal. Externally, it is tied to the output voltage resistor divider (1:10) on the evaluation board, where there is a 120k ohm pull up to VCC and a 13.3k ohm pull down to GND, creating the 1:10 divider.

SFB
The SFB test point is the CATH pin for the FUSB3307. CATH is the feedback signal to the primary controller. It connects to the comp pin of the NCV81599. CATH pin is open-drain output and controlled by CV/CC logic in the FUSB3307.

CC1, CC2
Configuration Channel 1 and 2, these pins are used to detect USB Type-C devices and to communicate using USB PD communication protocol when applicable. Also used for VCONN supply. For USB PD, the maximum capacitance is limited to 600pF.

Descriptions of other FUSB3307 pins that do not have test points on the evaluation board

GATE

Gate drive signal to drive the gate of external NFET load switch. Using an internal charge pump, the external NFET gate is controlled using this pin. The source power of the charge pump is from FUSB3307 VCC.

IS+, IS-

Current sensing amplifier positive/negative terminals. IS+ is connected to the GND_SNS return path of the Type-C receptacle. IS- connects to the device GND pin. Charging current is calculated as: the voltage on IS+ is divided by Rsense (i.e. 5 milliohms) and then amplified 40 times, which will be actual sense current. The sense resistor needs to be 5 milliOhms.

D-, D+

D-, D+ can be used for multiple purposes by the FUSB3307. The default programmed function is for BC1.2 functionality, used for signaling of BC1.2 host operation. Another option for these pins' function is for maximum power control: PDIV0 and PDIV1. This mode is controlled by programming (fuse trimmed during production). The QFNW package has a PDIV2 pin which can limit the total power by 50%. See the FUSB3307 datasheet for a full description of the PDIV0, PDIV1, and PDIV2 functionality.

Descriptions of jumpers, connectors on the evaluation board

P3, P4, and P5

If the FUSB3307 device mounted on the evaluation board is programmed to support PDIV0, PDIV1, or PDIV2, then the P3, P4, and P5 jumpers permit shorting any of the three PDIVn signals to GND. Leaving the jumper open allows the signal to be pulled up to VDD via R52, R53, or R45. Note that R52 and R53 are not populated by default, so if a custom FUSB3307 device is used with PDIV0, PDIV1 functionality, R52 and R53 need to also be populated with 10k ohm resistors. See the FUSB3307 datasheet for a full description of the PDIV0, PDIV1, and PDIV2 functionality.

J3

This two pin connector is used for supplying VBAT and GND to the evaluation board.

J6

This 16 pin header is used for attaching the optional Strata controller daughter card to the evaluation board.

J1

The Type-C receptacle.

Descriptions of Key Features

VCC OVP (Over-Voltage Protection)

VCC voltage is measured by an ADC with $1/10^{th}$ VCC voltage. Since the VCC range is wide, between 3.3V ~ 21V, VCC OVP voltage threshold is defined in the datasheet as 121% of the PD contract voltage. There is a maximum OVP spec (23.8V Typ) which governs in general. So, in the case of a 5V PD contract, the OVP trigger point is 6.05V and so on for other PD contract voltages. For a 20V PD contract, the OVP will be triggered by either the 121% (24.2V) trigger point or the maximum OVP spec (23V min/23.8V Typ/24.8V max).

Once an OVP Fault is triggered, VBUS will be shut off (external NFET off) and so the sink will be disconnected. Also, the CATH signal will drop to GND to recover VCC back to 5V. There will be no PD Alert message transmitted to the sink device caused by the OVP Fault, which is different from OCP or OTP Faults. If an OTP or OCP Fault happens, there is a PD Alert message sent to the attached sink device.

When VBUS voltage is changing because of a PD contract change, the OVP is disabled during the transition time which is called OVP blanking time, typically 221ms.

CC OVP (Over-Voltage Protection)

In the Type-C receptacle, there could be a chance to short between VBUS and either CC signal. The FUSB3307 has high voltage protection for this case. The threshold is 6.5V Typ with 28us debounce.

VCC UVP (Under-Voltage Protection)

Like OVP, another protection is UVP which is the case when the VCC voltage drops blow the spec, which is 65% of contract voltage. For example, at VBUS of 5V, the UVP trigger point is 3.25V. There is the same blanking time of 221ms during any VBUS voltage transition. Once UVP occurs, there is a PD Alert message sent to the sink device.

VCC OCP (Over-Current Protection)

The FUSB3307 senses the VBUS load current via a small Rsense resistor (5 milliohm) as described in the datasheet. The OCP fault is triggered at 120% of the maximum current for the requested Power Data Object (PDO) for fixed supplies only, typically 3.6A for a 3A maximum fixed supply current.

For PPS APDOs (Augmented Power Data Objects), Constant Current Limiting (CL) is used as specified in the USB PD specification where the voltage will drop to a low value based on keeping the current constant and equal to the requested PPS current. More details can be found in the FUSB3307 datasheet.

Once an OCP Fault is triggered, VBUS will be shut off (external NFET off) and so the sink will be disconnected. Also, the CATH signal will drop to GND to recover VCC back to 5V. There will be an OCP Fault happens, there is a PD Alert message sent to the attached sink device upon the FUSB3307 establishing an explicit contract with the sink device.

OTP (Over-Temperature Protection)

OTP is measured internally for the SOIC package. There are two different threshods, 125C for a warning or 135C for a Fault. If the warning threshold is triggered longer then the OTP debounce time, typically 80ms, a PD Alert message for the temperature warning will be sent to the sink. Once the Fault threshold is triggered, the FUSB3307 will disable the Type-C connection, shut off VBUS (external NFET off), and monitor the Fault. Once the Fault has been cleared, the FUSB3307 will wait a recovery time, typically 2s, and then begin monitoring the CC lines for an attach. Upon re-establishing an explicit contract with the sink, a PD Alert message will be sent to let the sink know that the FUSB3307 previously experienced an OTP Fault.

The QFNW package also has an NTC pin to monitor the external temperature. In the case of the QFNW package, only the external temperature will trigger a PD Alert for a warning. The NTC pin is connected to an NTC resisitor (100k ohm ±1%, B25/50 = 4300k ±1%) in parallel with a 20k ohm resistor to GND. But, either the internal temperature threshold or the external temperature threshold can cause an OTP Fault.

CATH feedback

The CATH pin is used to provide feedback to the circuit providing VCC/VBUS to the FUSB3307. Typically an opto−coupler cathode on the secondary side is connected to the CATH pin to provide feedback signal to the primary side PWM controller. Alternatively, the CATH pin can be connected to the error amplifier output of a DC−DC regulator (often called the compensation pin) or with an inverting circuit to the DC−DC feedback (FB) pin. Once an explicit contract is established with the sink, this signal is used to control whatever VBUS voltage is required, from as little as 3.3V to 21V in the case of a USB PD PPS contract.

BMC eye diagram on CC1/CC2

The BMC eye diagram on CC, Figure and Figure 2, is used to guarantee the signal level/quality is passing the mask that is defined by USB-IF PD specifications. The voltage range of the BMC signal is between -100mV to 1.2V but it can be higher and lower depending on GND shift due to load or noise interference on the signal path.

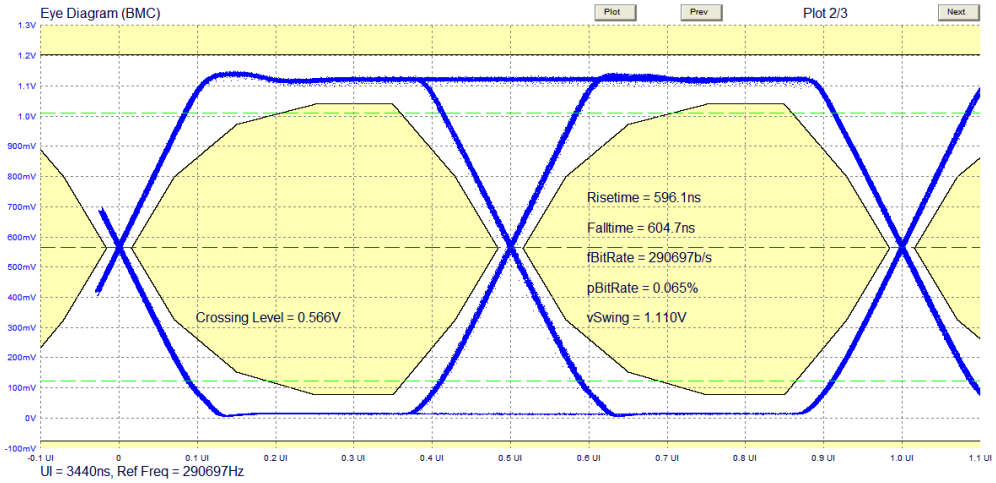


Figure 1 - BMC eye diagram on CC1

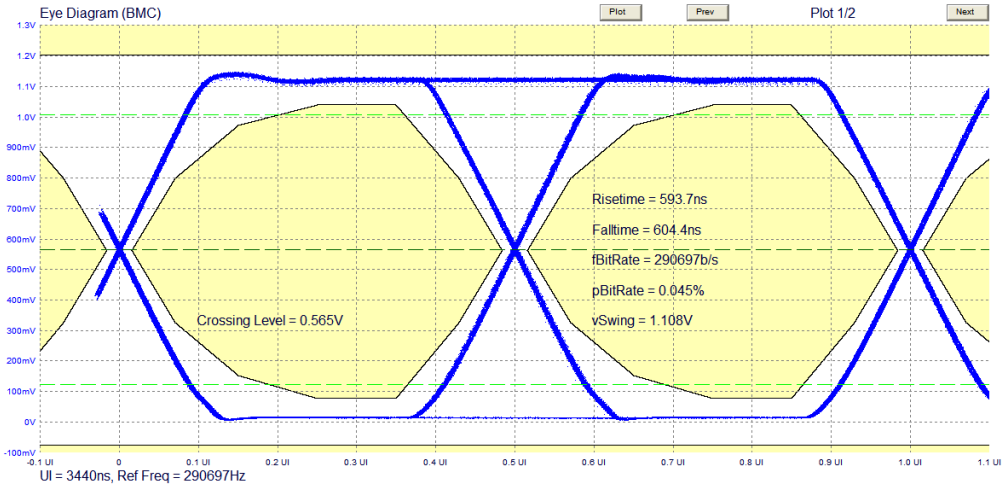


Figure 2 - BMC eye diagram on CC2

60W Efficiency

Figure 3 shows the efficiency curves for VBUS at 5V, 9V, 12V, 15V, and 20V with load varying from 0.5A to 3A.

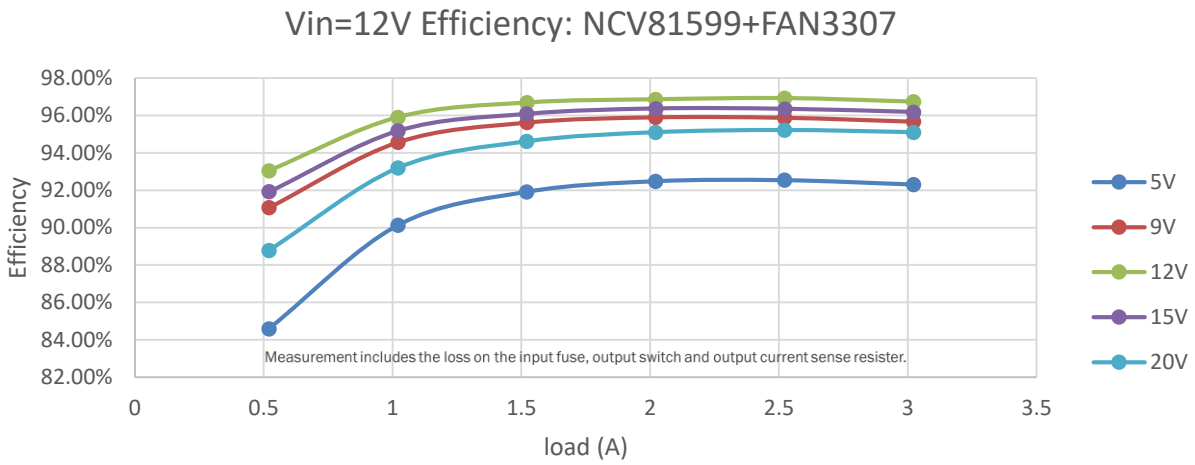


Figure 3 - Efficiency curves

Load Regulation

Figure 4 shows the load regulation curve for VBUS at 5V with load varying from 0.5A to 3A. Figure5 shows the 9V curve.

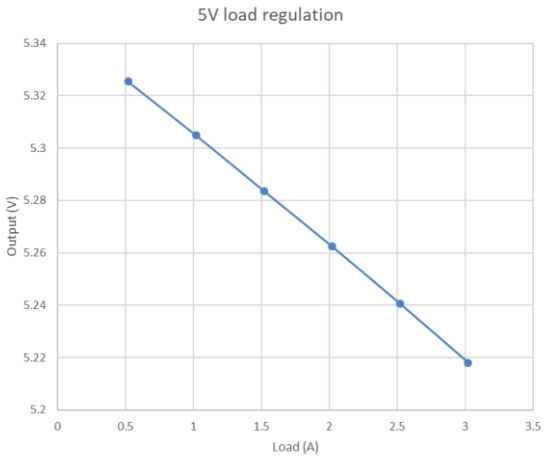


Figure 4 - 5V regulation

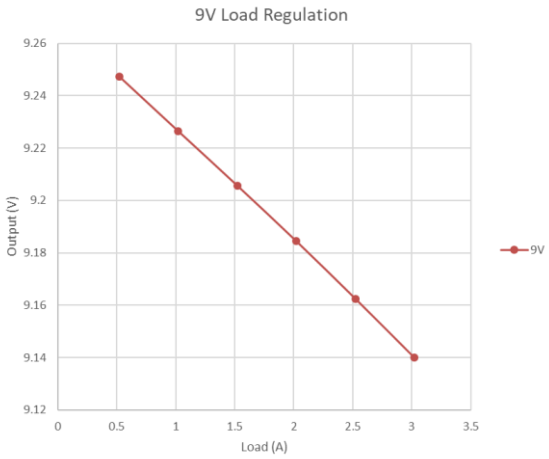


Figure 5 - 9V regulation

Figure 6 shows the load regulation curve for VBUS at 12V and Figure 7 shows the 15V curve.

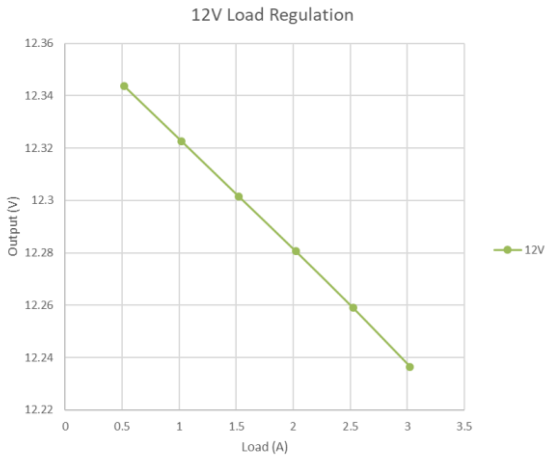


Figure 6 - 12V regulation

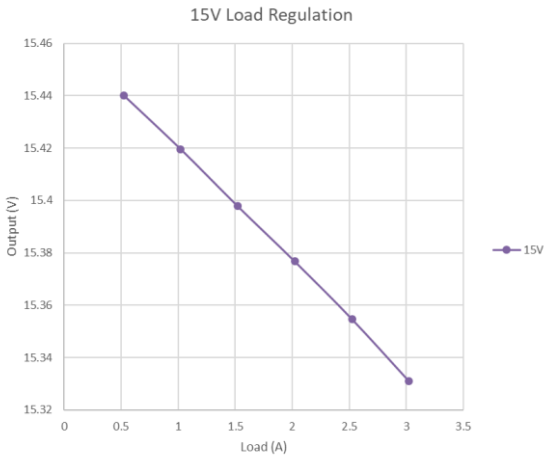


Figure 7 - 15V regulation

Figure shows the load regulation curve for VBUS at 20V.

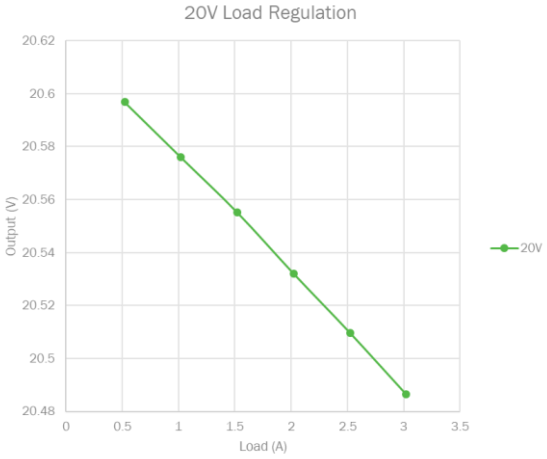


Figure 8 - 20V regulation

Figure 9 shows the load regulation curves for each value of VBUS with load varying from 0.5A to 3A.

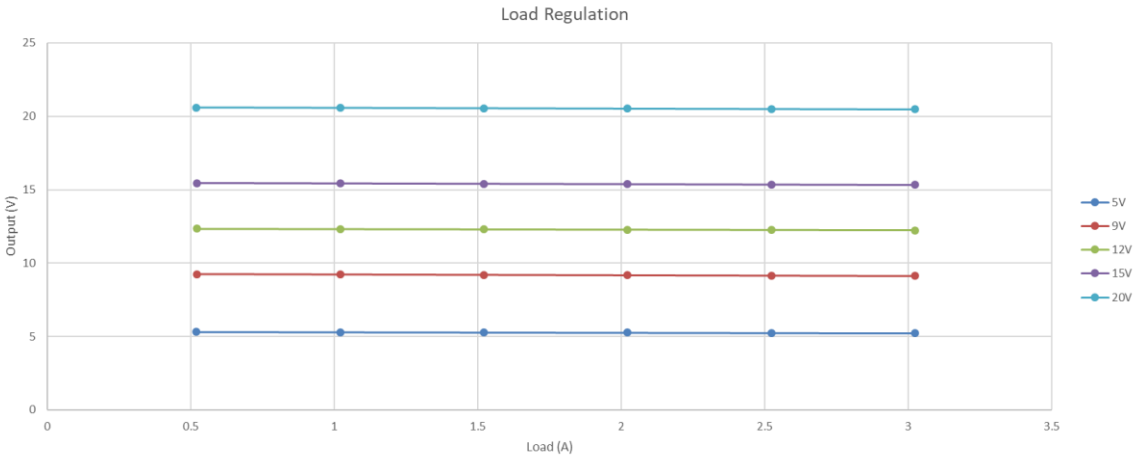


Figure 9 - Regulation curves

Voltage transitions with no load

Below are the waveforms of VBAT at 12V and VBUS voltage changing from 5V to 12V and back to 5V with no load. VBUS, SFB, and SWN1 waveforms are shown. VBUS change from 5V to 12V in Figure 10 and 12V to 5V in Figure 11.

Figure 10 - 5V to 12V transition with no load

Figure 11 - 12V to 5V transition with no load

Below are the waveforms of VBAT at 12V and VBUS voltage changing from 5V to 15V and back to 5V with no load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 5V to 15V in Figure 12 and 15V to 5V in Figure 13.

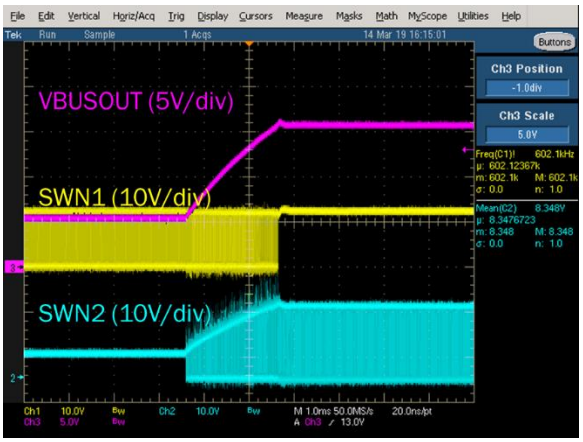


Figure 12 - 5V to 15V transition with no load

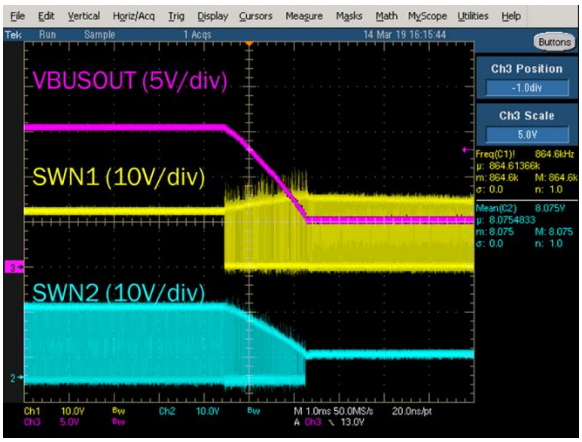


Figure 1 15V to 5V transition with no load

Below are the waveforms of VBAT at 12V and VBUS voltage changing from 5V to 20V and back to 5V with no load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 5V to 20V in Figure 14 and 20V to 5V in Figure 15.

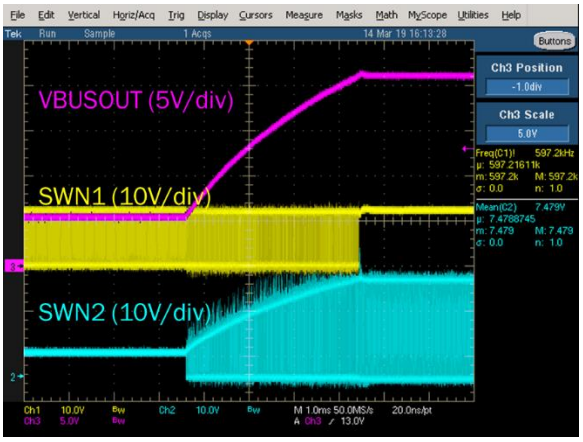


Figure 14 - 5V to 20V transition with no load

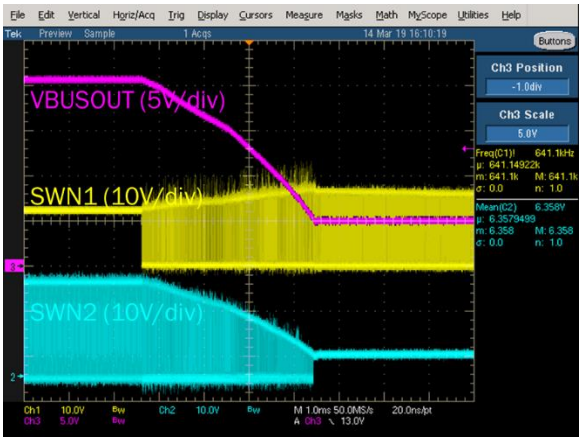


Figure 15 - 20V to 5V transition with no load

Voltage transitions with load

Below are the waveforms of VBAT at 12V and VBUS voltage changing from 20V to 3.3V with a 2.66A load and back to 20V with a 1A load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 20V to 3.3V in Figure 16 and 3.3V to 20V in Figure 17.

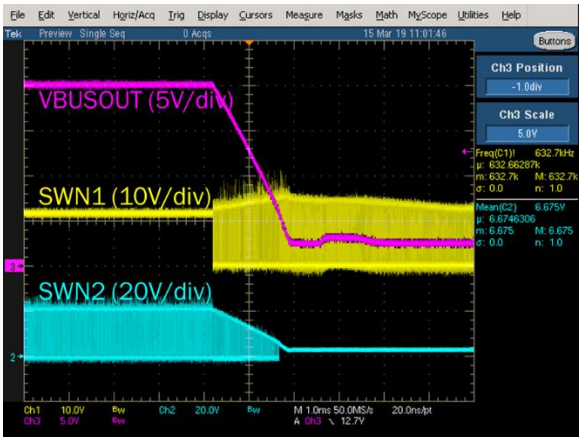


Figure 16 - 20V to 3.3V transition with 2.66A load

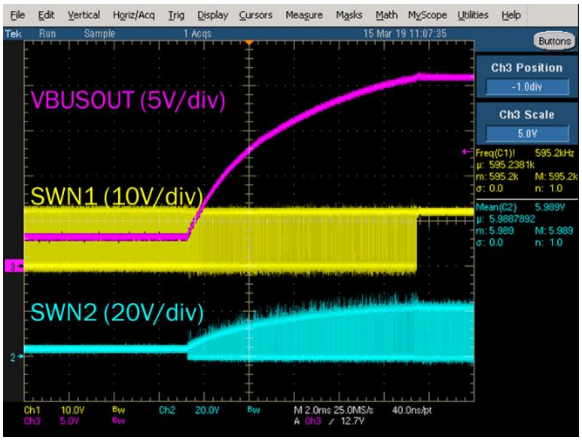


Figure 17 - 3.3V to 20V transition with 1A load

VBUSOUT Transient Load testing

Below are the waveforms with VBAT at 12V and VBUSOUT with a 0A load for 3ms and then a 3A load for 3ms. t_{RISE} and t_{FALL} are 3mA/µs. Transient waveforms for 5V and 9V are shown below in Figure 18 and Figure 19.

Figure 18 - Transient load on 5V VBUS

Figure 19 - Transient load on 9V VBUS

Transient waveforms for 12V and 15V are shown in Figure 20 and Figure 1.

Figure 20 - Transient load on 12V VBUS

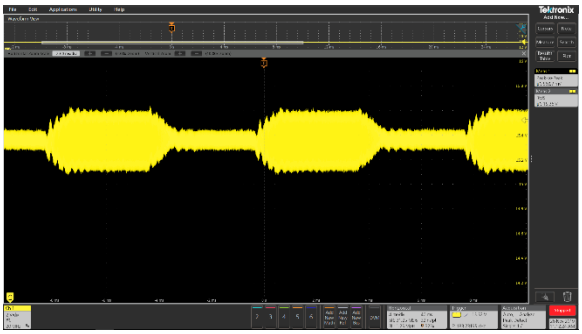


Figure 21 - Transient load on 15V VBUS

Transient waveform for 20V is shown in Figure 2.

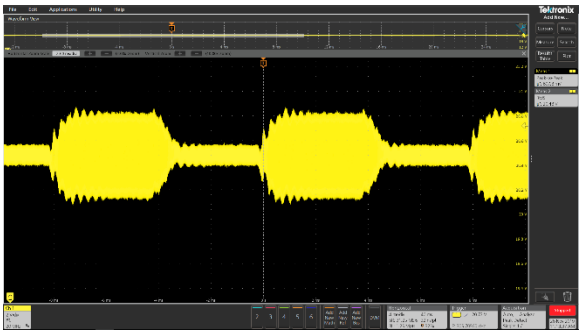


Figure 22 - Transient load on 20V VBUS

VBUSOUT Voltage Ripple with and without load

Below are the waveforms with VBAT at 12V and VBUSOUT voltage ripple for 5V, with a 3A load and no load. VBUSOUT waveforms are shown. Figure 3 is 5V with 3A load and Figure 24 is 5V with no load.

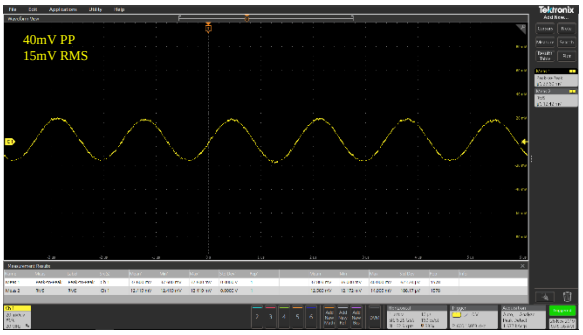


Figure 23 - VBUSOUT ripple for 5V/3A

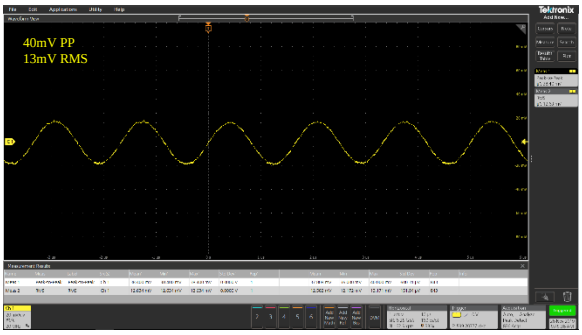


Figure 2 VBUSOUT ripple for 5V/0A

Below are the waveforms with VBAT at 12V and VBUSOUT voltage ripple for 9V, with a 3A load and no load. VBUSOUT waveforms are shown. Figure 25 is 9V with 3A load and Figure 26 is 9V with no load.

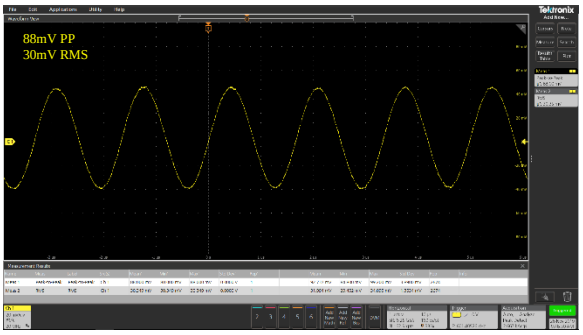


Figure 25 - VBUSOUT ripple for 9V/3A

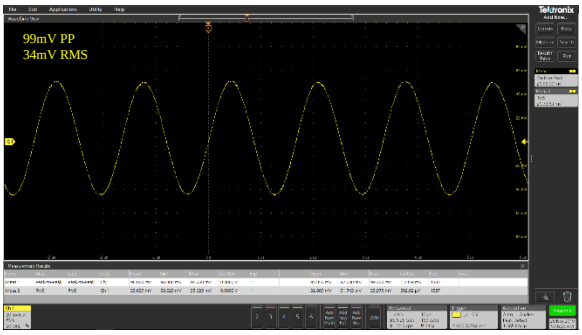


Figure 26 - VBUSOUT ripple for 9V/0A

Below are the waveforms with VBAT at 12V and VBUSOUT voltage ripple for 12V, with a 3A load and no load. VBUSOUT waveforms are shown. Figure 27 is 12V with 3A load and Figure 28 is 12V with no load.

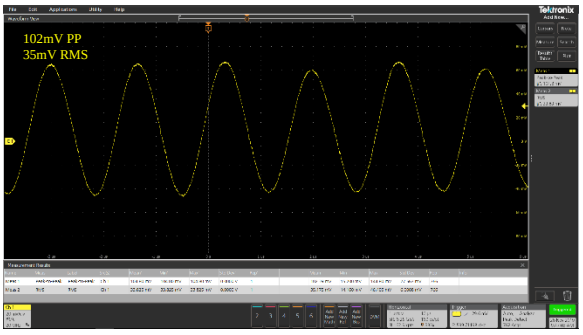


Figure 27 - VBUSOUT ripple for 12V/3A

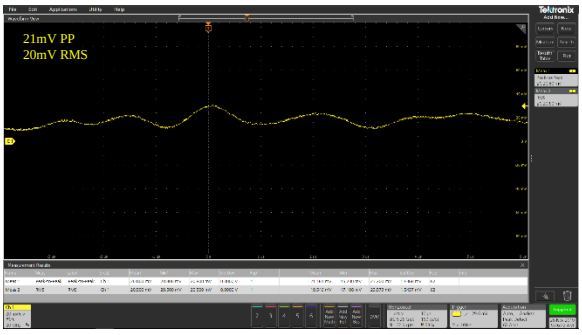


Figure 28 - VBUSOUT ripple for 12V/0A

Below are the waveforms with VBAT at 12V and VBUSOUT voltage ripple for 15V, with a 3A load and no load. VBUSOUT waveforms are shown. Figure29 is 15V with 3A load and Figure 30 is 15V with no load.

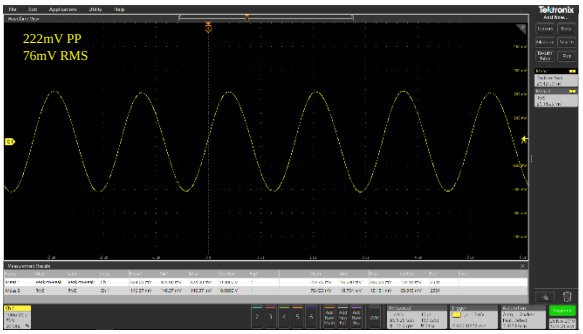


Figure 29 - VBUSOUT ripple for 15V/3A

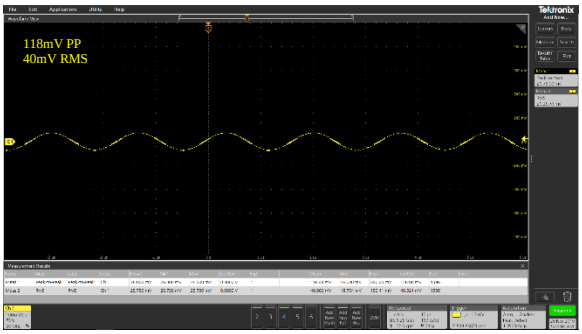


Figure 30 - VBUSOUT ripple for 15V/0A

Below are the waveforms with VBAT at 12V and VBUSOUT voltage ripple for 20V, with a 3A load and no load. VBUSOUT waveforms are shown. Figure 1 is 20V with 3A load and Figure 2 is 20V with no load.

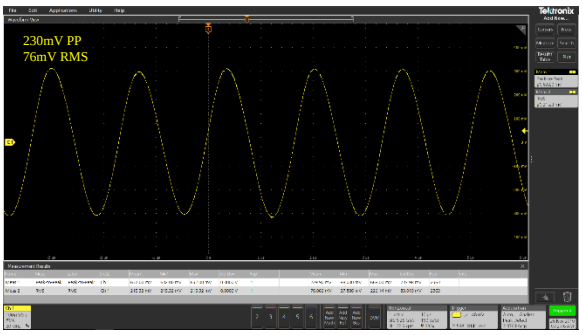


Figure 31 - VBUSOUT ripple for 20V/3A

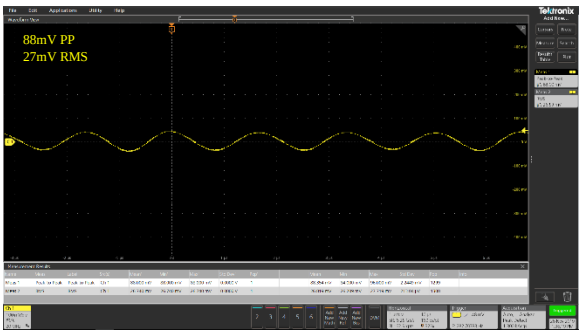


Figure 32 - VBUSOUT ripple for 20V/0A

VBUS discharge

VBUS discharge occurs when the VBUS voltage transitions to a lower target voltage, such as 20V down to 5V, when there is a light load, less than 450mA, or no load. If more of a load (tested 500mA and 2A) is present, there is no VBUS discharge during the transition as the load current itself discharges the VBUS. If a cable is unplugged (detach), there is VBUS discharge regardless of load presence unless VBUS is 5V when the cable is unplugged.

When the cable is unplugged, there is another VBUS discharge with the GATE (NFET) off to discharge from 1uF output capacitor. This applies even when VBUS was 5V previously.

The discharge timer is always the same at 210ms, but, the discharge current is not consistent because it depends on the VBUS voltage when the internal discharge FET is turned on.

The waveform in Figure 3 is when VBUS changes from 20V to 5V and the waveform in Figure 4 is when the Type-C cable is unplugged. For both cases, there is a VBUS discharge because there was no load on this test. When the cable is unplugged, there is another discharge along with the VBUS shut off.

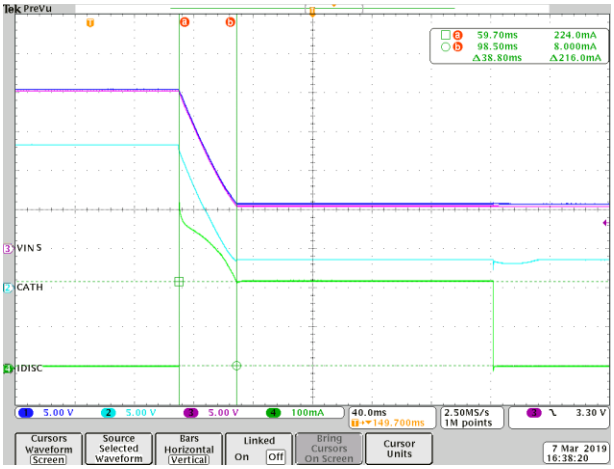


Figure 33 - VBUS discharge, from 20V to 5V, without a load

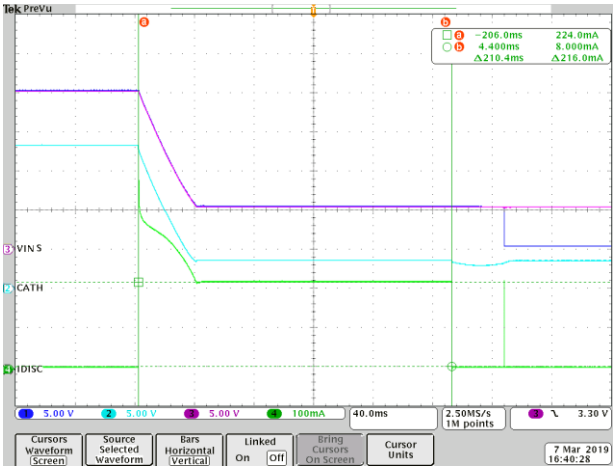


Figure 34 - VBUS discharge, from 20V to 0V, when Type-C cable is unplugged

Figure 35 is when VBUS changes from 20V to 15V without a load, and the Figure 36 waveform is the same voltage change, but, with a 500mA load.

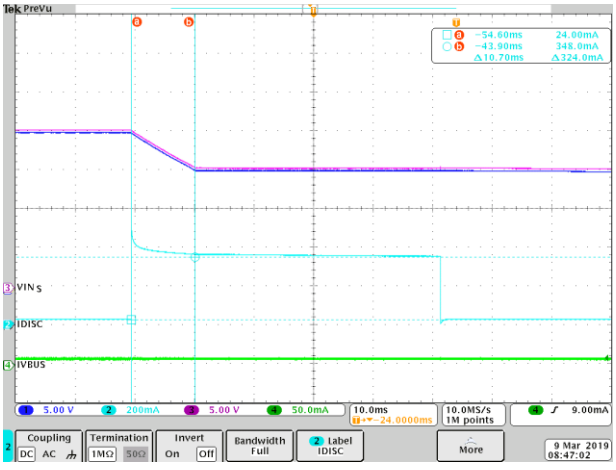


Figure 35 - VBUS discharge, from 20V to 15V, without a load

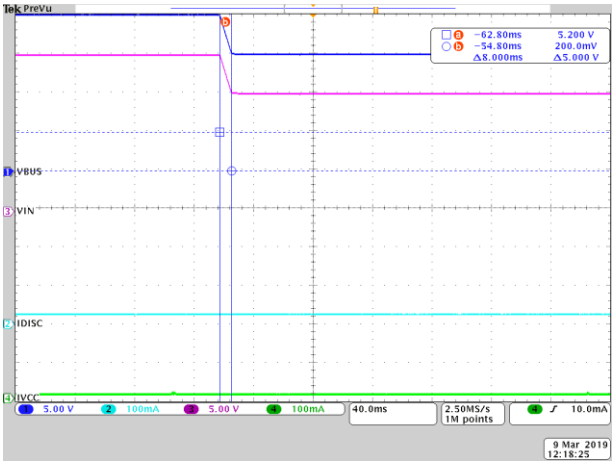


Figure 36 - VBUS discharge, from 20V to 15V, with a 500mA load

Figure 37 shows a waveform when VBUS changes from 20V to 5V without a load, Figure 38 shows a waveform with the same transition with a 500mA load. If there is load above 250mA, there is no VBUS discharge.

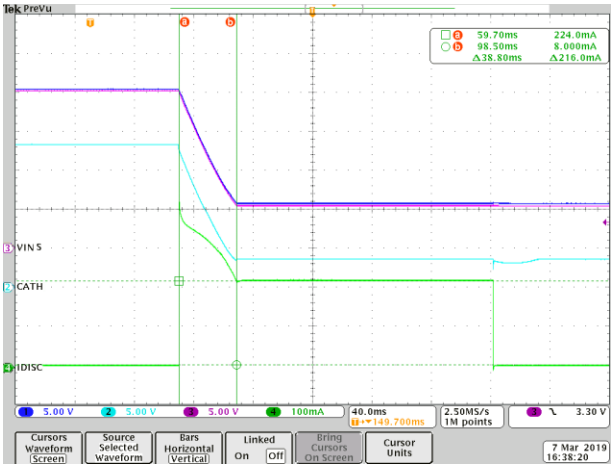


Figure 37 - VBUS discharge, from 20V to 5V, without a load

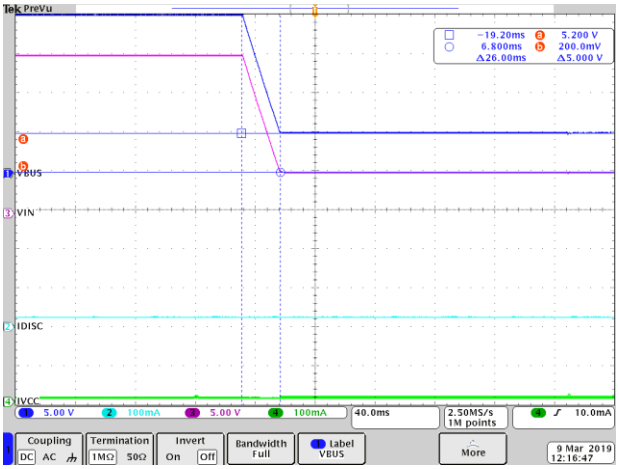


Figure 38 - VBUS discharge, from 20V to 5V, with a 500 mA load

Figure 39 shows a waveform when VBUS changes from 20V to 5V with 2A load and Figure 40 shows a waveform when VBUS changes from 20V to 15V with 2A load as well. Due to the load, there is no VBUS discharge for either case.

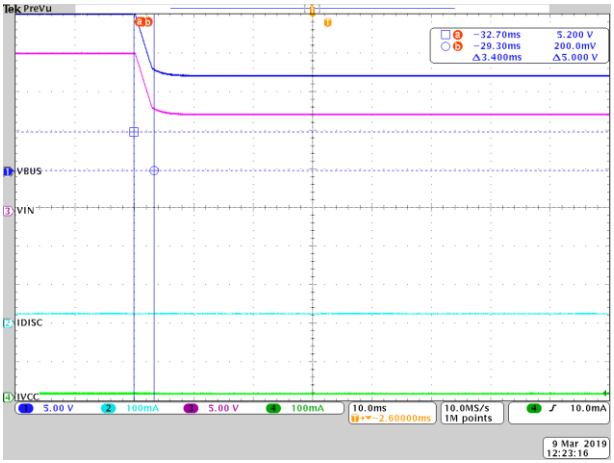


Figure 39 - VBUS discharge, from 20V to 5V, with a 2A load

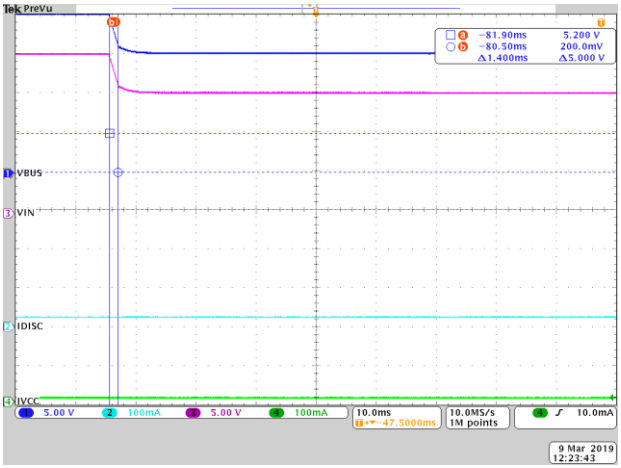


Figure 40 - VBUS discharge, from 20V to 15V, with a 2A load

VCC discharge

VCC discharge occurs along with GATE off (external NFET off) for cases such as cable plug out or if a fault happens (OVP/OCP/OTP/UVP), so if cable is unplugged with VBUS at 9V to 20V, there will be both discharge on VBUS and VCC. VCC discharge occurs later than VBUS discharge. VCC discharge occurs after the NFET is open and after VBUS discharge is turned off, so the sink is not connected when VCC discharge occurs. VCC discharge timing is the same as VBUS discharge, 210ms, but, the discharge current is constant because VCC discharge occurs when the VCC drops down to 5V. The exception is VCC discharge at Fault, such as OCP, where VBUS discharge doesn't occur, so VCC voltage can be greater than 5V, creating a larger VCC discharge current.

The waveform in Figure 411 is when the Type-C cable is unplugged with 5V VBUS. As mentioned above, there is no VBUS discharge when the cable is unplugged at 5V VBUS, but, there is VCC discharge. The waveform in Figure 2 is when the cable is unplugged at 9V, VBUS discharge drops the VBUS voltage down to 5V and then the external NFET opens followed by turning on VCC discharge.

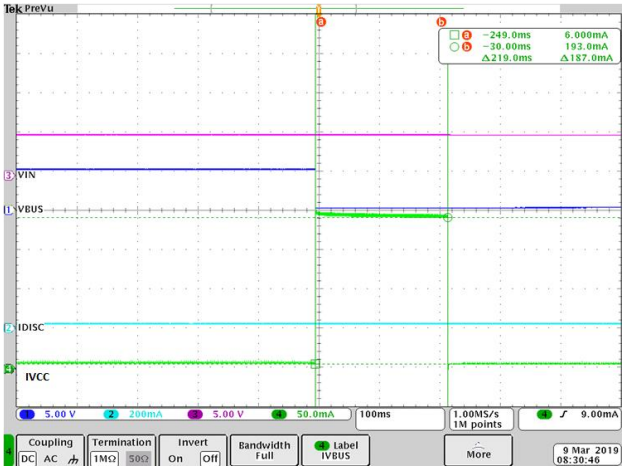


Figure 41 - VCC discharge, from 5V, when Type-C cable is unplugged

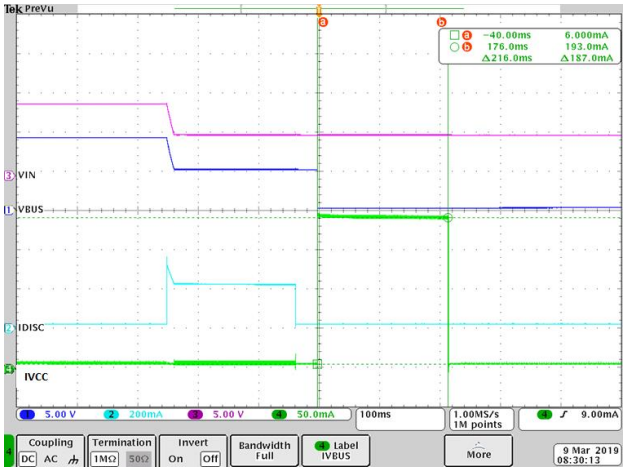


Figure 42 - VCC discharge, from 9V, when Type-C cable is unplugged

The next 2 waveforms are the same, Figure 3 is a cable unplug at 15V, and Figure 444 is a cable unplug at 20V. Both VBUS and VCC discharges occur in series.

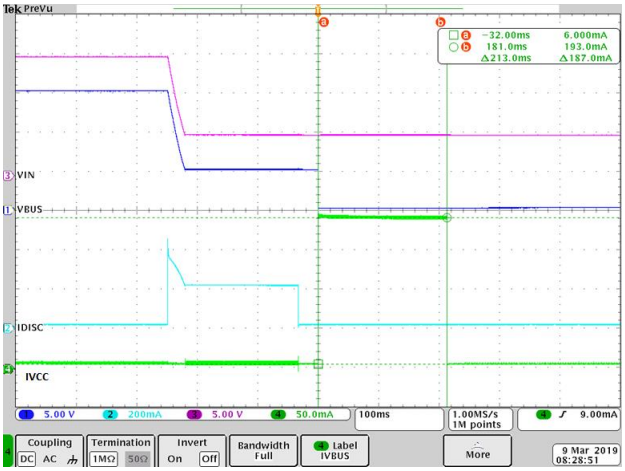


Figure 43 - VCC discharge, from 15V, when Type-C cable is unplugged

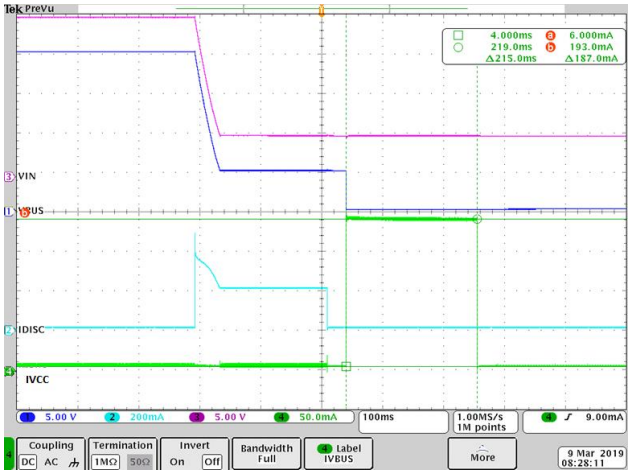


Figure 44 - VCC discharge, from 20V, when Type-C cable is unplugged

BC1.2

The FUSB3307 supports BC1.2 (USB Battery Charging) along with proprietary charger support. Once a Type-C sink is attached, both D+/D- voltages increase to 2.75V and stay at that voltage unless VDP (D+ voltage) or VDM (D- voltage) move above or below that threshold, then D+ and D- are shorted together so that a sink device having BC1.2 detection can detect the FUSB3307 as a DCP (Dedicated Charging Port). The waveform in Figure 45 shows D+/D- are the same voltage after atttach.

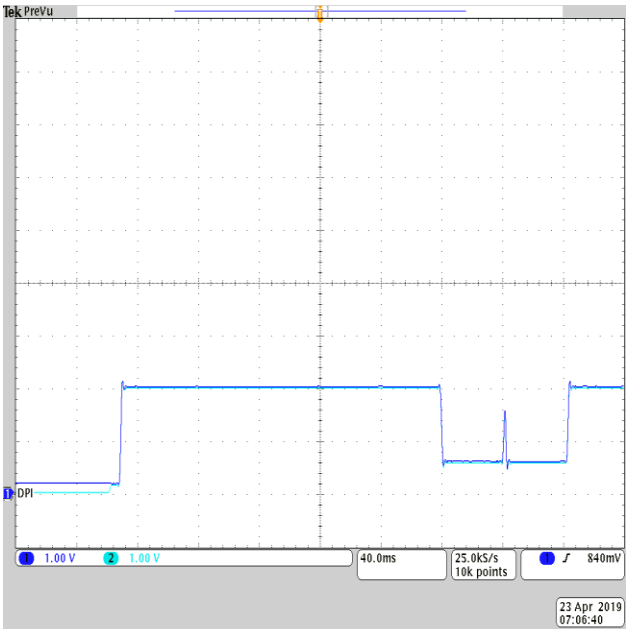


Figure 45 - D+/D- voltage after attach

VCONN Supply

The FUSB3307 supports VCONN power to verify the cable type when sink is attached. It is enabled along with VBUS. But, VCONN is only supplied when the FUSB3307 is programmed (fuse trimmed during production) as 5A (maximum VBUS current) capable and a cable marker IC is present in the Type-C cable. If the FUSB3307 is 3A capable, VCONN is not enabled. If the FUSB3307 is programmed to support 5A, VCONN is not always turned on. It is only turned on when there is Ra (1k ohm) present on the non-communication CC channel (VCONN). In the 2 waveforms below, the waveform in Figure 46 shows a non-cable marker cable attach, while the waveform in Figure 47 shows a cable marker cable attach. There is no VCONN on the CC2 (the non-communication channel or VCONN) regardless of cable type because the FUSB3307 device used was only 3A capable.

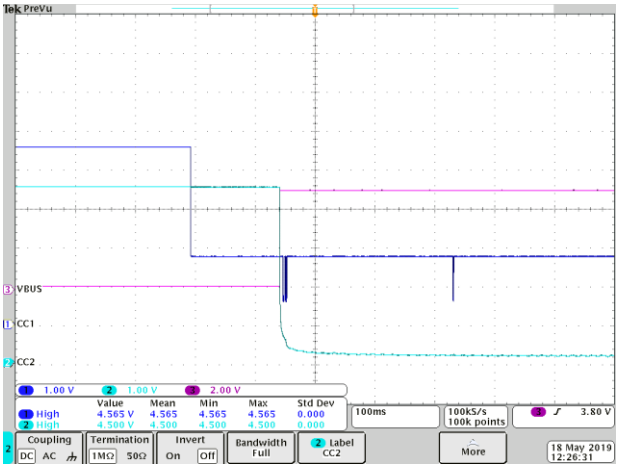


Figure 46 - VCONN when non-cable marker cable is attached (FUSB3307 w/3A support)

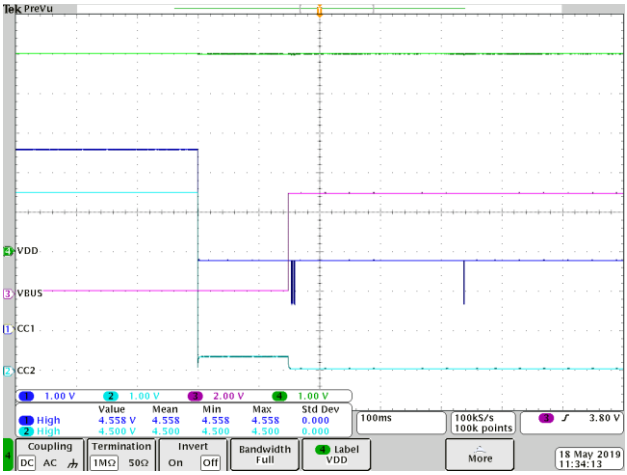


Figure 47 - VCONN when cable marker cable is attached (FUSB3307 w/3A support)

The two waveforms below are when the FUSB3307 is programmed to support 5A. The waveform in Figure 48 is with a non-cable marker cable. If Ra is not present, VCONN gets turned off when Vbus is supplied. The waveform in Figure 49, where Ra is present (cable marker cable), VCONN is enabled on CC2 and valid until the cable ID is verified which takes about 50msec.

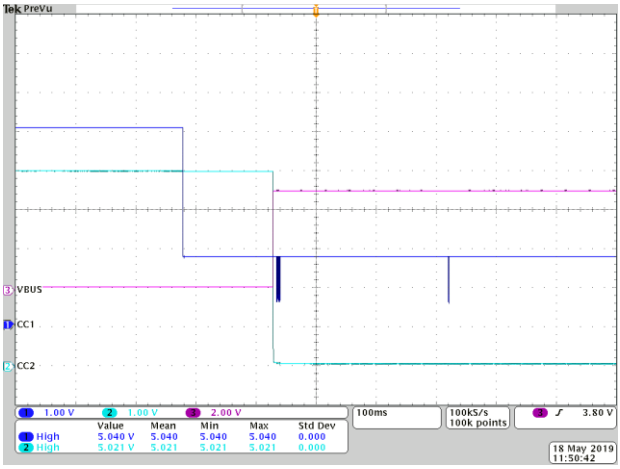


Figure 48 - VCONN when non-cable marker cable is attached (FUSB3307 w/5A support)

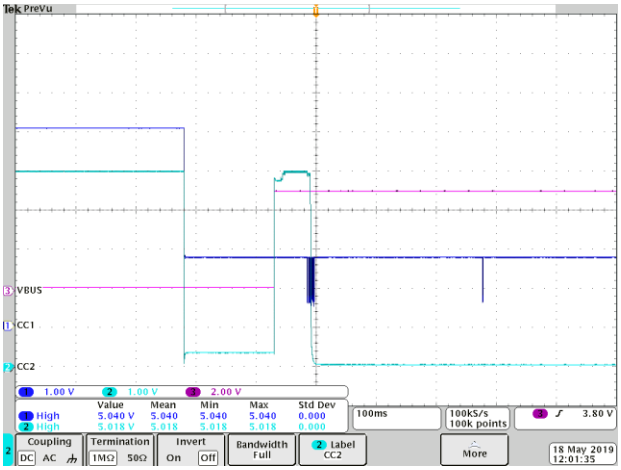
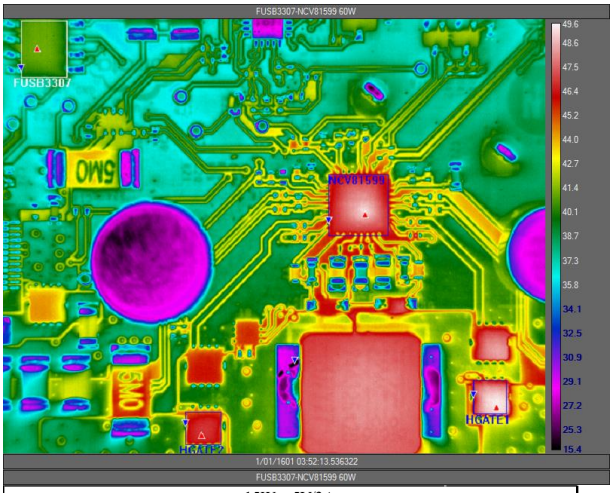


Figure 49 - VCONN when cable marker cable is attached (FUSB3307 w/5A support)

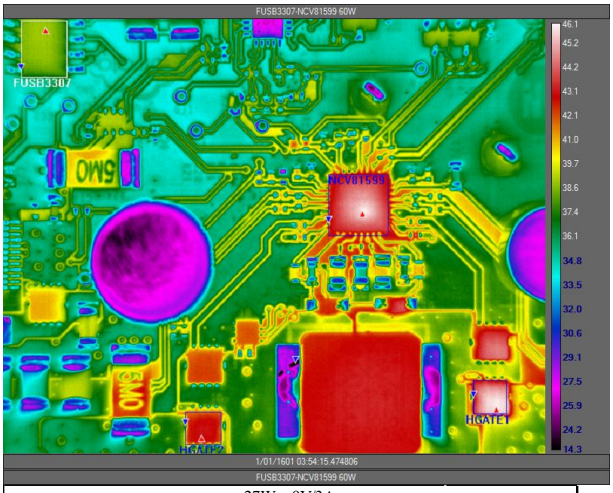
Thermal Measurements

Figure 50 shows the thermals for 15W (5V/3A) and Figure 1 shows the thermals for 27W (9V/3A).



15W – 5V/3A	
Region	Max (°C)
FUSB3307	40
NCV81599	47
BUCK FET (HGATE1)	48
BOOST FET (HGATE2)	46

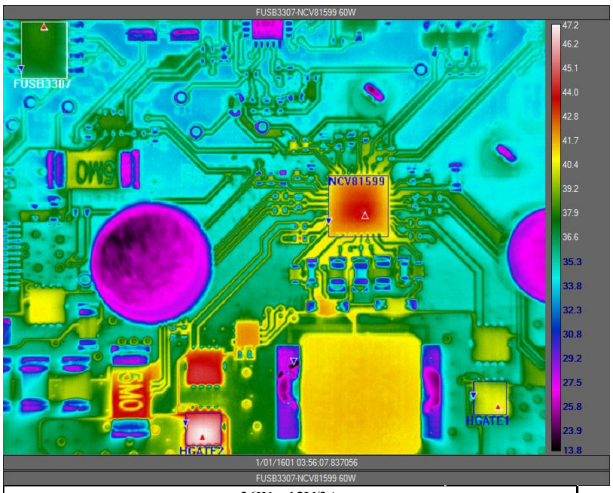
Figure 50 - Thermal image and data for 15W (5V/3A)



27W – 9V/3A	
Region	Max (°C)
FUSB3307	38
NCV81599	44
BUCK FET (HGATE1)	45
BOOST FET (HGATE2)	42

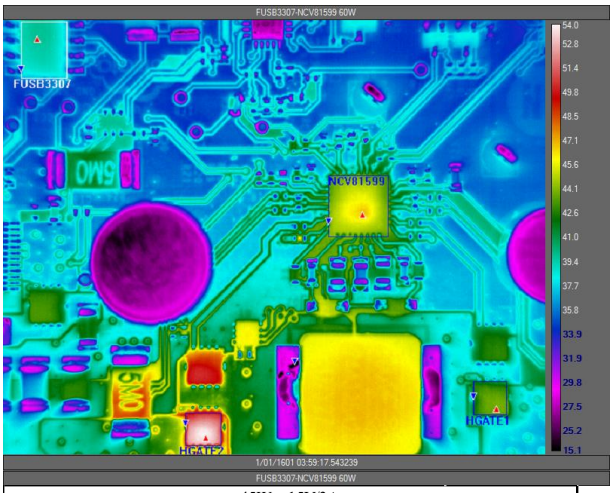
Figure 51 - Thermal image and data for 27W (9V/3A)

Figure 2 shows the thermals for 36W (12V/3A) and Figure 3 shows the thermals for 45W (15V/3A).



36W – 12V/3A	
Region	Max (°C)
FUSB3307	37
NCV81599	42
BUCK FET (HGATE1)	40
BOOST FET (HGATE2)	46

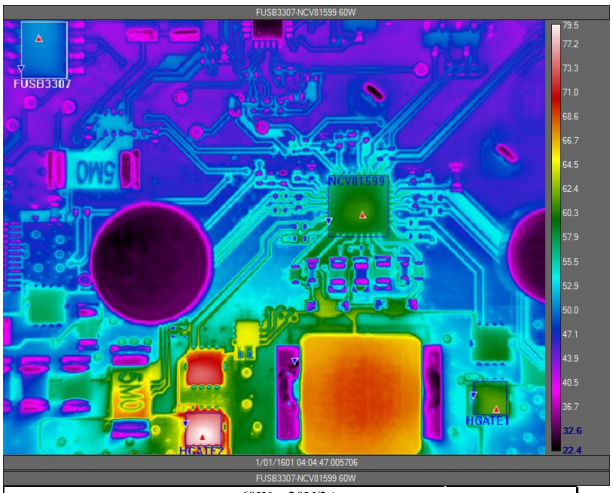
Figure 52 - Thermal image and data for 36W (12V/3A)



45W – 15V/3A	
Region	Max (°C)
FUSB3307	39
NCV81599	45
BUCK FET (HGATE1)	43
BOOST FET (HGATE2)	52

Figure 53 - Thermal image and data for 45W (15V/3A)

Figure 4 shows the thermals for 60W (20V/3A).



60W – 20V/3A	
Region	Max (°C)
FUSB3307	49
NCV81599	58
BUCK FET (HGATE1)	60
BOOST FET (HGATE2)	76

Figure 54 - Thermal image and data for 60W (20V/3A)

USB-IF PD Compliance Testing Results

The FUSB3307D6MX passed testing for USB PD3.0 with PPS at the USB-IF PD Compliance Workshop #114 the week of June 10, 2019, using the STR-FUSB3307MX-PPS-GEVB. TID: 1430.

QuadraMAX - v0.8.7074

- **PASSED**

LeCroy - v3.81 build 836

- **PASSED**

GRL - SW v1.3.14.0 / FW v1.3.14.0.324

- **PASSED**

MQP - v6.06.08

- **PASSED**

USB2.0 Electricals

- **PASSED**

Type-C and PD IOP

- test against Google phone, Google laptop, and Macbook
- **PASSED**

Ellisys - v3.1.7095

- **PASSED**

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