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Configurable Multifunction Gate

NL7SZ97

The NL7SZ97 is an advanced high−speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt−trigger inputs, thereby enhancing noise immunity.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 3.3 ns t_{PD} at V_{CC} = 5 V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Available in SC−88, SC-74 and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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MARKING DIAGRAMS

SC−88/SC70−6/
SOT−363
CASE 419B−02

XXXM■

SC−74
CASE 318F−05

XXX M■

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ

XM

UDFN6
1.2 x 1.0
CASE 517AA

X M

UDFN6, 1x1, 0.35P
CASE 517BX

X M
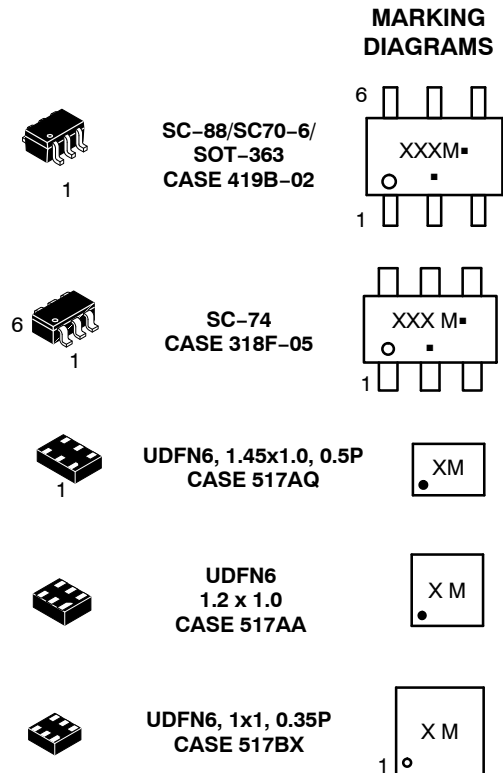
XXX = Specific Device Code
M = Date Code*
■ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NL7SZ97
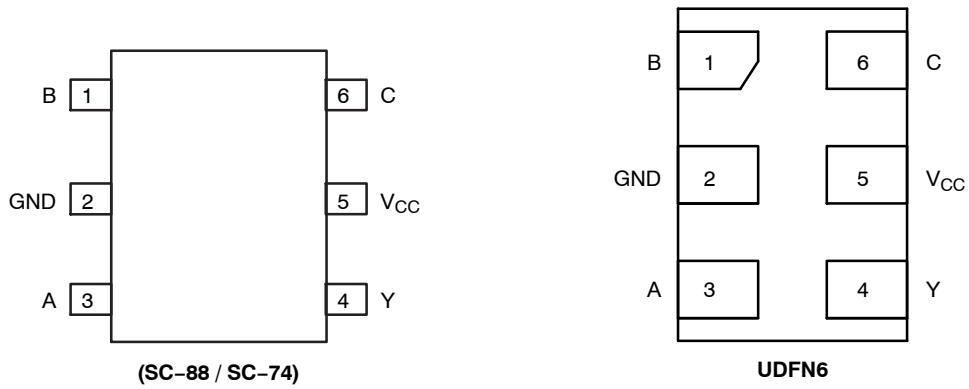
Figure 1. Pinout (Top View)
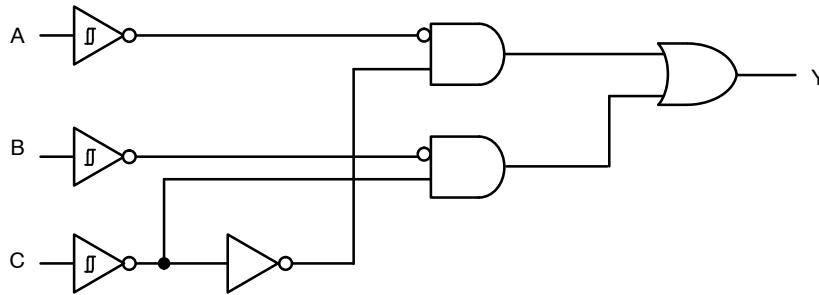
Figure 2. Function Diagram

PIN ASSIGNMENT

Pin	Function
1	B
2	GND
3	A
4	Y
5	V_{CC}
6	C

FUNCTION TABLE*

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

*To select a logic function, please refer to "Logic Configurations section".

NL7SZ97

LOGIC CONFIGURATIONS

Figure 3. 2−Input MUX

Figure 4. 2−Input AND (When B = "L")

Figure 5. 2−Input OR with Input C Inverted (When B = "H")

Figure 6. 2−Input AND with Input C Inverted (When A = "L")

Figure 7. 2−Input OR (When A ="H")

Figure 8. Inverter (When A = "L" and B = "H")

Figure 9. Buffer (When A = C = "L")

NL7SZ97

MAXIMUM RATINGS

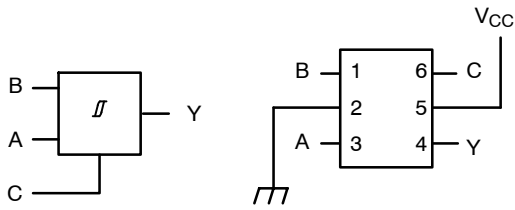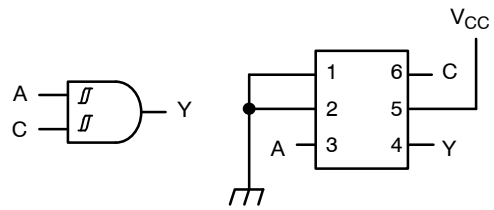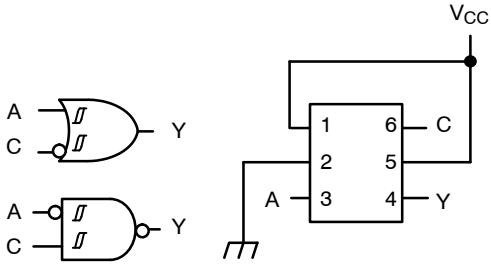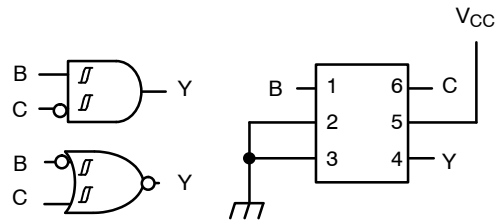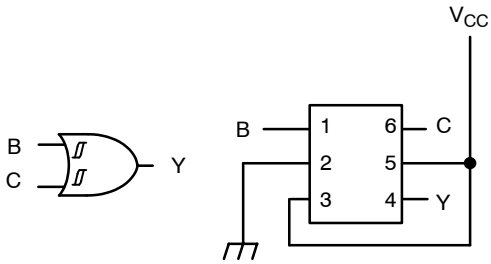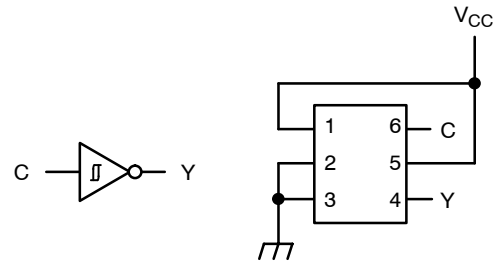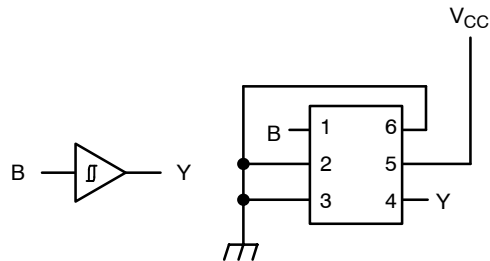| Symbol	Parameter		Value	Unit
V$_{CC}$	DC Supply Voltage	SC−88 (NLV) SC−88, SC−74, UDFN6	−0.5 to +7.0 −0.5 to +6.5	V
V$_{IN}$	DC Input Voltage	SC−88 (NLV) SC−88, SC−74, UDFN6	−0.5 to +7.0 −0.5 to +6.5	V
V$_{OUT}$	DC Output Voltage SC−88 (NLV)	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V$_{CC}$ = 0 V)	−0.5 to V$_{CC}$ + 0.5 −0.5 to +7.0 −0.5 to +7.0	V
	DC Output Voltage SC−88, SC−74, UDFN6	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V$_{CC}$ = 0 V)	−0.5 to V$_{CC}$ + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I$_{IK}$	DC Input Diode Current	V$_{IN}$ < GND	−50	mA
I$_{OK}$	DC Output Diode Current	V$_{OUT}$ < GND	−50	mA
I$_{OUT}$	DC Output Source/Sink Current		±50	mA
I$_{CC}$ or I$_{GND}$	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T$_{STG}$	Storage Temperature Range		−65 to +150	°C
T$_L$	Lead Temperature, 1 mm from Case for 10 Secs		260	°C
T$_J$	Junction Temperature Under Bias		+150	°C
θ$_{JA}$	Thermal Resistance (Note 2)	SC−88 SC−74 UDFN6	377 320 154	°C/W
P$_D$	Power Dissipation in Still Air	SC−88 SC−74 UDFN6	332 390 812	mW
MSL	Moisture Sensitivity		Level 1	
F$_R$	Flammability Rating Oxygen	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V$_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Mode Charged Device Model (NLV) Charged Device Model	>2000 >200 N/A	V
I$_{LATCHUP}$	Latchup Performance (Note 4)	(NLV)	±500 ±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V$_{CC}$	Positive DC Supply Voltage		1.65	5.5	V
V$_{IN}$	DC Input Voltage		0	5.5	V
V$_{OUT}$	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V$_{CC}$ = 0 V)	0 0 0	V$_{CC}$ 5.5 5.5	V
T$_A$	Operating Free−Air Temperature		−55	+125	°C
t$_r$, t$_f$	Input Rise or Fall Rate	V$_{CC}$ = 1.65 V to 1.95 V V$_{CC}$ = 2.3 V to 2.7 V V$_{CC}$ = 3.0 V to 3.6 V V$_{CC}$ = 4.5 V to 5.5 V	0 0 0 0	No Limit No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25°C$			$-40°C \leq T_A \leq 85°C$		$-55°C \leq T_A \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	Positive Input Threshold Voltage		1.65	–	–	1.4	–	1.4	–	1.4	V
			2.3	–	–	1.8	–	1.8	–	1.8	
			3.0	–	–	2.2	–	2.2	–	2.2	
			4.5	–	–	3.1	–	3.1	–	3.1	
			5.5	–	–	3.6	–	3.6	–	3.6	
V_{T-}	Negative Input Threshold Voltage		1.65	0.2	–	–	0.2	–	0.2	–	V
			2.3	0.4	–	–	0.4	–	0.4	–	
			3.0	0.6	–	–	0.6	–	0.6	–	
			4.5	1.0	–	–	1.0	–	1.0	–	
			5.5	1.2	–	–	1.2	–	1.2	–	
V_H	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	–	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	–	
			3	0.4	0.93	1.2	0.4	1.2	0.4	–	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	–	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	–	
V_{OH}	High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.65 to 5.5	$V_{CC} - 0.1$	V_{CC}	–	$V_{CC} - 0.1$	–	$V_{CC} - 0.1$	–	V
		$I_{OH} = -4$ mA	1.65	1.20	1.52	–	1.20	–	1.20	–	
		$I_{OH} = -8$ mA	2.3	1.9	2.1	–	1.9	–	1.9	–	
		$I_{OH} = -16$ mA	3	2.4	2.7	–	2.4	–	2.4	–	
		$I_{OH} = -24$ mA	3	2.3	2.5	–	2.3	–	2.3	–	
		$I_{OH} = -32$ mA	4.5	3.8	4	–	3.8	–	3.8	–	
V_{OL}	Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	1.65 to 5.5	–	–	0.1	–	0.1	–	0.1	V
		$I_{OL} = 4$ mA	1.65	–	0.08	0.45	–	0.45	–	0.45	
		$I_{OL} = 8$ mA	2.3	–	0.2	0.3	–	0.3	–	0.4	
		$I_{OL} = 16$ mA	3	–	0.28	0.4	–	0.4	–	0.5	
		$I_{OL} = 24$ mA	3	–	0.38	0.55	–	0.55	–	0.55	
		$I_{OL} = 32$ mA	4.5	–	0.42	0.55	–	0.55	–	0.65	
I_{IN}	Input Leakage Current	$V_{IN} = 5.5$ V or GND	1.65 to 5.5	–	–	+0.1	–	+1.0	–	+1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5$ V or $V_{OUT} = 5.5$ V	0	–	–	1.0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = 5.5$ V or GND	5.5	–	–	1.0	–	10	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_CC (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B or C) to Y (Figures 10 and 11)	R_L = 1 kΩ, C_L = 30 pF	1.65 to 1.95	–	8.6	14.4	–	14.4	–	14.4	ns
		R_L = 500 Ω, CL = 30 pF	2.3 to 2.7	–	5.1	8.3	–	8.3	–	8.3	
		R_L = 500 Ω, C_L = 50 pF	3.0 to 3.6	–	3.9	6.3	–	6.3	–	6.3	
			4.5 to 5.5	–	3.3	5.1	–	5.1	–	5.1	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_{IN} = 0 V or V_{CC} 10 MHz, V_{CC} = 5.0 V, V_{IN} = 0 V or V_{CC}	16 19.5	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NL7SZ97
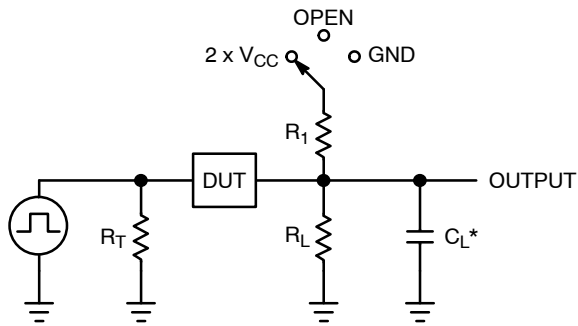
C_L includes probe and jig capacitance
R_T is Z_OUT of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 10. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω	R_1, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	2 x V_CC	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care
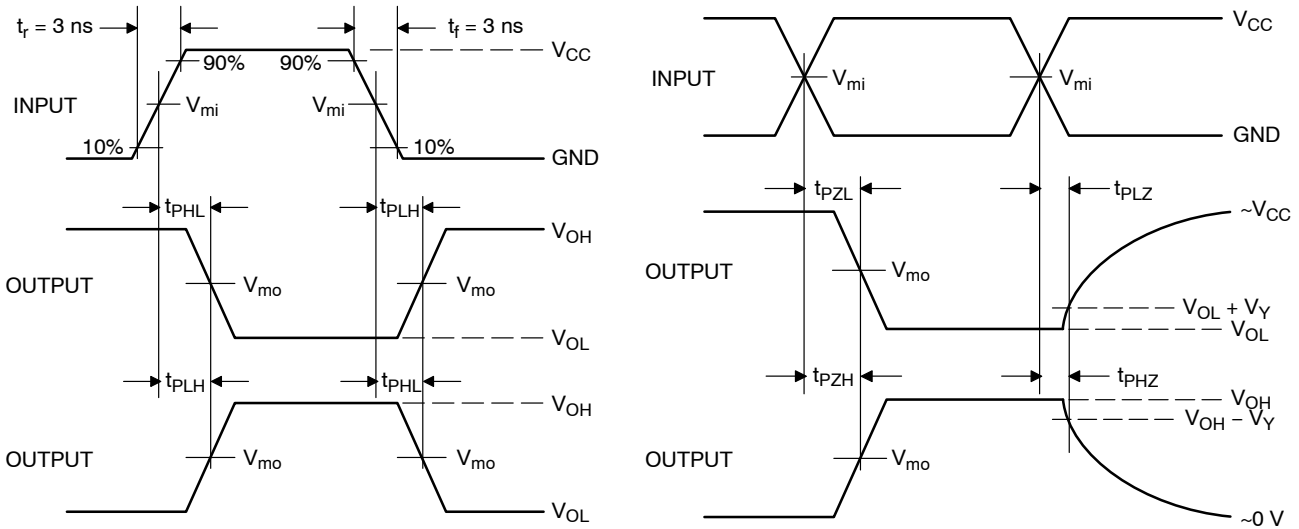
Figure 11. Switching Waveforms

		V_{mo}, V		
V_{CC}, V	**V_{mi}, V**	**t_{PLH}, t_{PHL}**	**t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}**	**V_Y, V**
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.3
4.5 to 5.5	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.3

NL7SZ97

ORDERING INFORMATION

Device	Package			Shipping†
NL7SZ97DFT2G	SC−88 (Pb−Free)	MK	Q4	3000 / Tape & Reel
NLV7SZ97DFT2G*	SC−88 (Pb−Free)	MK	Q4	3000 / Tape & Reel
NL7SZ97DBVT1G	SC−74 (Pb−Free)	AN	Q4	3000 / Tape & Reel
NL7SZ97MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb−Free)	5 (Rotated 270° CW)	Q4	3000 / Tape & Reel
NL7SZ97MU2TCG (In Development)	UDFN6, 1.2 x 1.0, 0.4P	D (Rotated 270° CW)	Q4	3000 / Tape & Reel
NL7SZ97MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb−Free)	TBD	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.
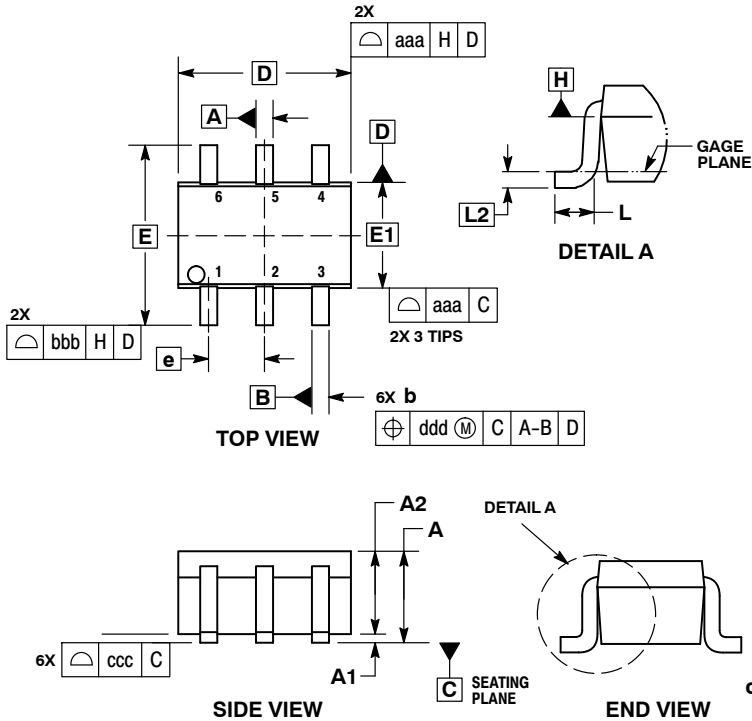
## Pin 1 Orientation in Tape and Reel
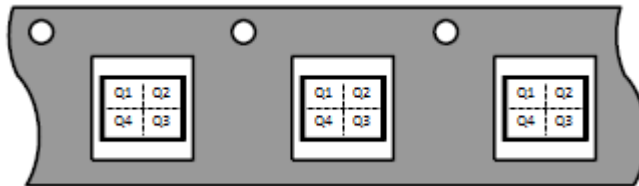
PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

TOP VIEW

2X aaa H D

H

DETAIL A

GAGE PLANE

L2 L

2X aaa C

2X 3 TIPS

2X bbb H D

6X b

B

⊕ ddd Ⓜ C A−B D

SIDE VIEW

A2
A
A1
DETAIL A
6X ccc C
C SEATING PLANE

END VIEW

c

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*
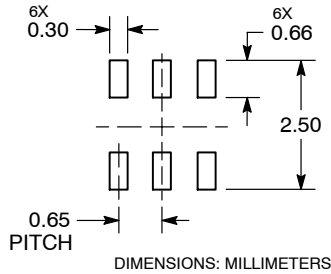
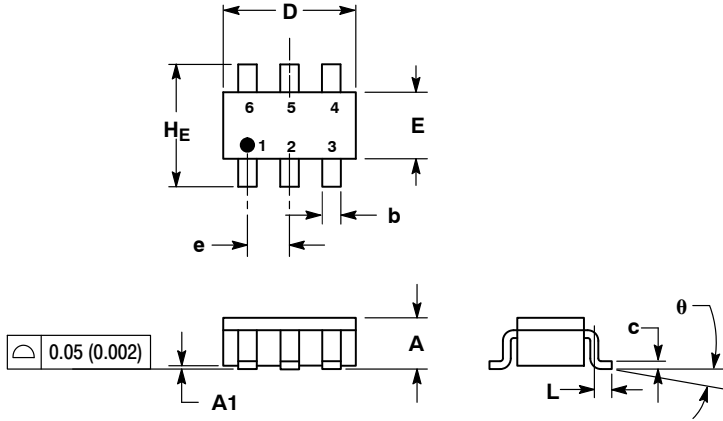6X 0.30
6X 0.66
2.50
0.65 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL7SZ97

PACKAGE DIMENSIONS

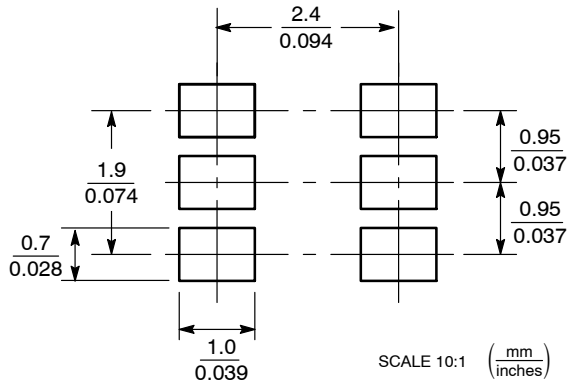**SC−74**
CASE 318F−05
ISSUE N

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

0.05 (0.002)

SOLDERING FOOTPRINT*

$\frac{2.4}{0.094}$

$\frac{1.9}{0.074}$

$\frac{0.7}{0.028}$

$\frac{0.95}{0.037}$

$\frac{0.95}{0.037}$

$\frac{1.0}{0.039}$

SCALE 10:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
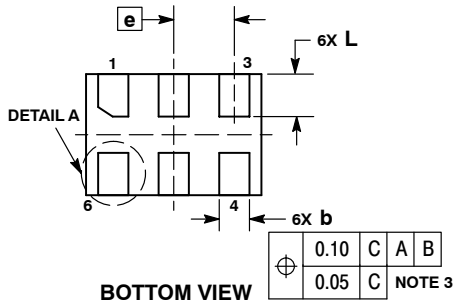
NL7SZ97

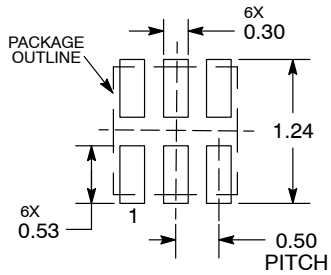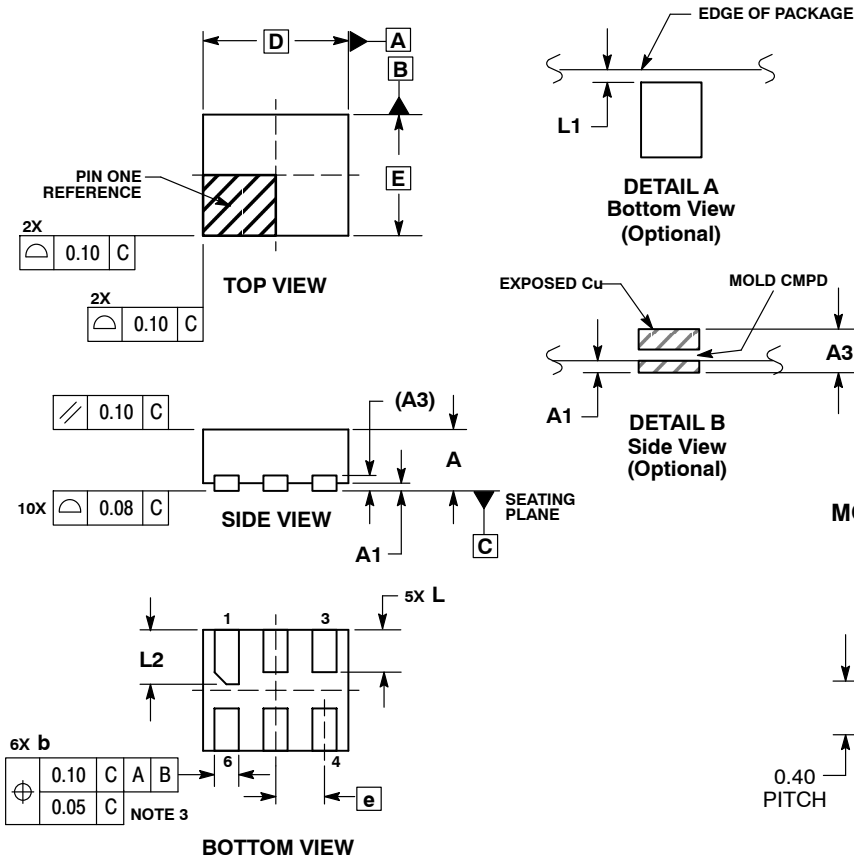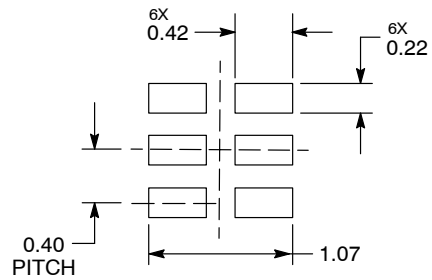## PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O
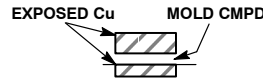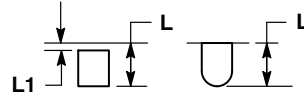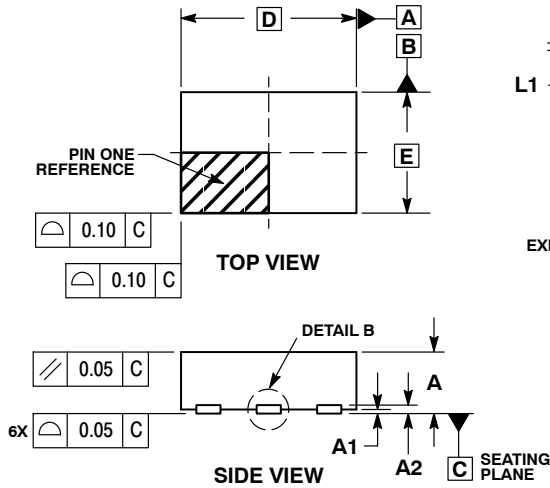
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	–––	0.15

TOP VIEW

PIN ONE REFERENCE

DETAIL A
OPTIONAL CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

DETAIL B
OPTIONAL CONSTRUCTIONS

SIDE VIEW

DETAIL B

SEATING PLANE

BOTTOM VIEW

DETAIL A

MOUNTING FOOTPRINT

PACKAGE OUTLINE

6X
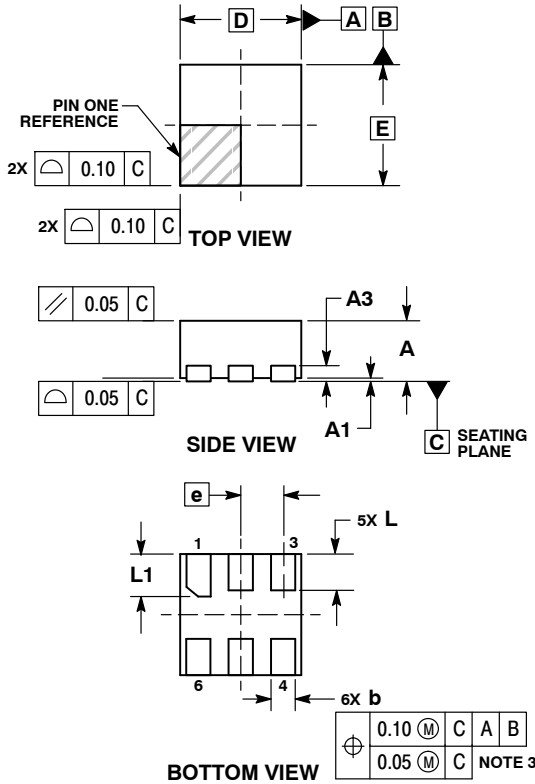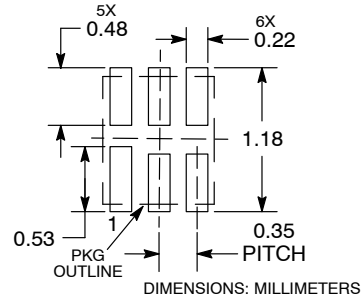0.30

1.24

6X
0.53

1

0.50
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

UDFN6, 1.2x1.0, 0.4P
CASE 517AA–01
ISSUE D

TOP VIEW

D
A
B
E
PIN ONE REFERENCE
2X | 0.10 | C
2X | 0.10 | C

SIDE VIEW

0.10 | C
(A3)
A
10X | 0.08 | C
A1
SEATING PLANE
C

BOTTOM VIEW

1   3
5X L
L2
6X b
6   4
0.10 | C | A | B
0.05 | C   NOTE 3
e

DETAIL A
Bottom View (Optional)

EDGE OF PACKAGE
L1

DETAIL B
Side View (Optional)

EXPOSED Cu
MOLD CMPD
A3
A1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

MOUNTING FOOTPRINT*

6X 0.42
6X 0.22
0.40 PITCH
1.07

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O

TOP VIEW

2X △ 0.10 C

2X △ 0.10 C

PIN ONE REFERENCE

D | A B

E

SIDE VIEW

// 0.05 C

△ 0.05 C

A3

A

A1

C SEATING PLANE

BOTTOM VIEW

e

5X L

L1

1 3

6 4

6X b

⊕ | 0.10 Ⓜ | C | A | B
⊕ | 0.05 Ⓜ | C | NOTE 3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

5X
0.48

6X
0.22

1.18

0.53

PKG OUTLINE

1

0.35
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

◊

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