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Power MOSFET

40 V, 33 A, Single N-Channel, DPAK/IPAK

Features

- Low R_{DS(on)}
- High Current Capability
- Avalanche Energy Specified
- NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- CCFL Backlight
- DC Motor Control
- Power Supply Secondary Side Synchronous Rectification

MAXIMUM RATINGS (T_{.I} = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltag	e – Contir	nuous	V_{GS}	±20	V
Gate-to-Source Voltage - Non-Repetitive (t _p < 10 μS)			V_{GS}	±30	V
Continuous Drain		T _C = 25°C	I _D	33	Α
Current (R _{0JC}) (Note 1)	Steady State	T _C = 100°C		23	
Power Dissipation (R _{θJC}) (Note 1)	State	T _C = 25°C	P _D	40	W
Pulsed Drain Current	t _p =	t _p = 10 μs		67	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			Is	33	Α
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 50 V, V_{GS} = 10 V, R_{G} = 25 Ω , $I_{L(pk)}$ = 28 A, L = 0.1 mH, V_{DS} = 40 V)			E _{AS}	39	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.7	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	57.5	

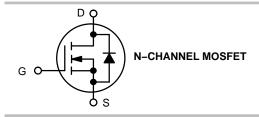
 Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces.



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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX	
40 V	26 mΩ @ 4.5 V	33 A	
	19 mΩ @ 10 V	33 A	



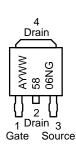


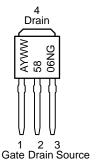
DPAK
CASE 369C
(Surface Mount)
STYLE 2



IPAK CASE 369D (Straight Lead DPAK) STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT





A = Assembly Location*

Y = Year
WW = Work Week
5806N = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

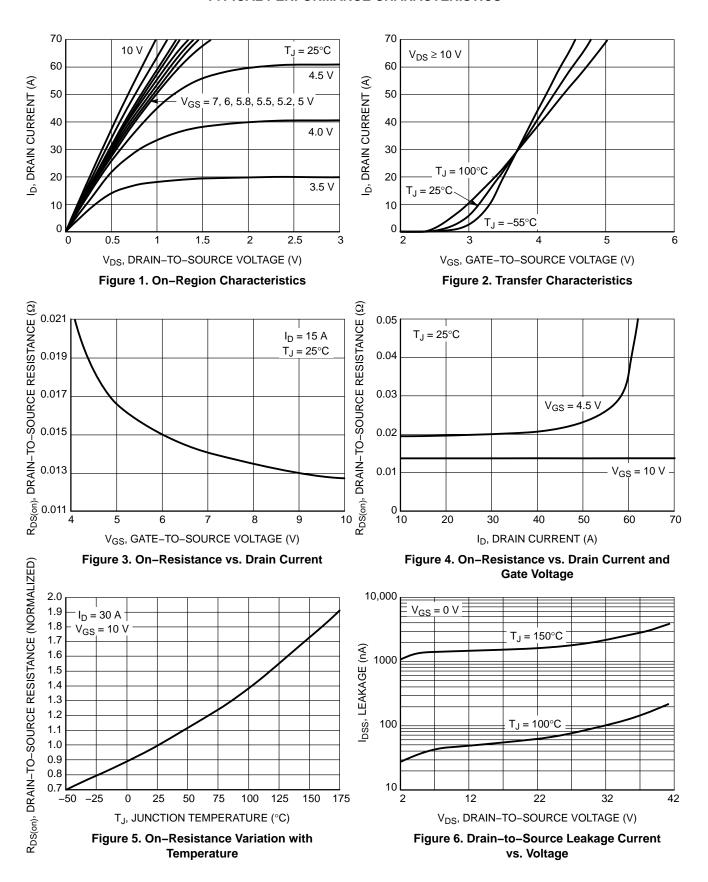
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Cond	ition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				•	•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40	45.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				29.5		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1.0	μΑ
		$V_{DS} = 40 \text{ V}$	T _J = 150°C			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	₃ = ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D}$	= 250 μΑ	1.4		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$			12.7	19	mΩ
					17.8	26	
CHARGES, CAPACITANCES AND GA	TE RESISTANCE	S			•	•	•
Input Capacitance	C _{iss}				860		pF
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V, f} = V_{DS} = 2^{t}$	1.0 MHz,		130		
Reverse Transfer Capacitance	C _{rss}	V _{DS} = 25 V			100		
Total Gate Charge	$Q_{G(TOT)}$				17	38	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V. V _G	s = 20 V.		0.95		
Gate-to-Source Charge	Q_{GS}	$V_{GS} = 10 \text{ V}, V_{DS} = 20 \text{ V},$ $I_{D} = 30 \text{ A}$			3.4		
Gate-to-Drain Charge	Q_{GD}				4.5		
SWITCHING CHARACTERISTICS (Not	e 3)				•	•	•
Turn-On Delay Time	t _{d(on)}				10.6		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{I}$	nn = 20 V.		93.7		
Turn-Off Delay Time	t _{d(off)}	$I_D = 30 \text{ A}, R_G$	$= 2.5 \Omega$		14.2		
Fall Time	t _f				4.3		
Turn-On Delay Time	t _{d(on)}				8.0		ns
Rise Time	t _r	V _{GS} = 10 V, V _D	n = 20 V.		49		
Turn-Off Delay Time	t _{d(off)}	$I_D = 30 \text{ A}, R_G$	= 2.5Ω		19.8		
Fall Time	t _f				2.6		
DRAIN-SOURCE DIODE CHARACTER	RISTICS				-	-	-
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V},$ $I_S = 10 \text{ A}$ $T_J = 25^{\circ}\text{C}$ $T_J = 150^{\circ}\text{C}$	T _J = 25°C		0.86	1.2	V
				0.69			
Reverse Recovery Time	t _{RR}		•		18.8		ns
Charge Time	ta	$V_{GS} = 0 \text{ V, dIs/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 30 \text{ A}$			11.8		
Discharge Time	tb				7.0		
Reverse Recovery Charge	Q_{RR}				10.9	<u> </u>	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%. 3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

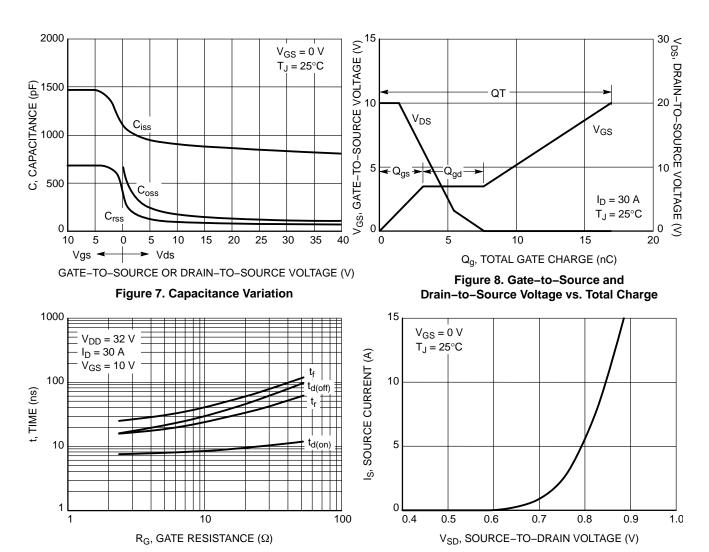


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

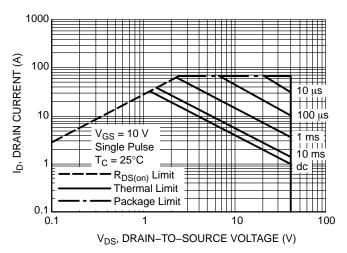


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CHARACTERISTICS

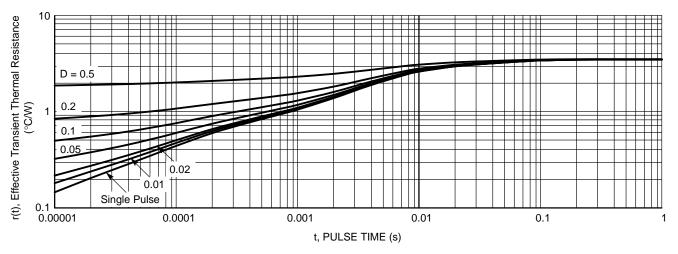


Figure 12. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD5806NG	IPAK (Straight Lead DPAK) (Pb-Free)	75 Units / Rail
NTD5806NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5806NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel
SVD5806NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

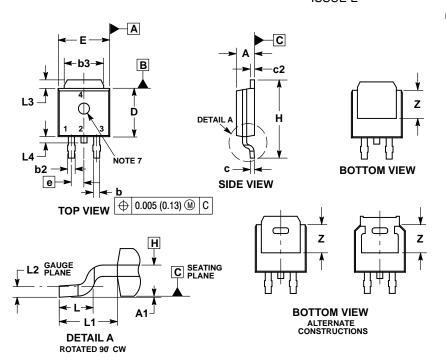
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C ISSUE E



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: INCHES.

 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

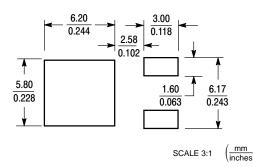
 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29 BSC		
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114 REF		2.90 REF		
L2	0.020 BSC		0.51 BSC		
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

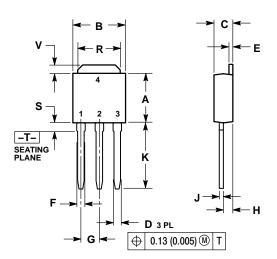
SOLDERING FOOTPRINT*

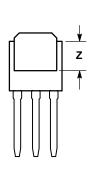


^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090 BSC		2.29 BSC		
Н	0.034	0.040	0.87	1.01	
ſ	0.018	0.023	0.46	0.58	
K	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

STYLE 2:

PIN 1. GATE

- 2. DRAIN
- SOURCE DRAIN

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