Low Voltage Precision Adjustable Shunt Regulator

TLV431, NCV431, SCV431

The TLV431A, B and C series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24 V to 16 V. The TLV431A series features a guaranteed reference accuracy of ±1.0% at 25°C and ±2.0% over the entire industrial temperature range of −40°C to 85°C. The TLV431B series features higher reference accuracy of ±0.5% and ±1.0% respectively. For the TLV431C series, the accuracy is even higher. It is ±0.2% and ±1.0% respectively. These devices exhibit a sharp low current turn−on characteristic with a low dynamic impedance of 0.20 Ω over an operating current range of 100 μA to 20 mA. This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise reference voltage. When combined with an optocoupler, the TLV431A/B/C can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (3.0 V to 3.3 V) switching power supplies. These devices are available in economical TO−92−3 and micro size TSOP−5 and SOT−23−3 packages.

Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance ±1.0% for A Series, ±0.5% for B Series and ±0.2% for C Series
- Sharp Low Current Turn−On Characteristic
- Low Dynamic Output Impedance of 0.20 Ω from 100 μA to 20 mA
- Wide Operating Current Range of 50 μA to 20 mA
- Micro Miniature TSOP−5, SOT−23−3 and TO−92−3 Packages
- NCV and SCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free and Halide−Free Devices

Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements

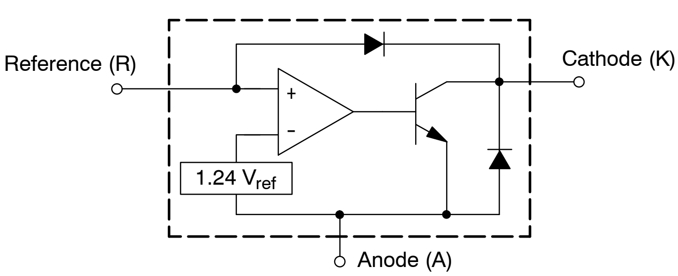

Figure 1. Representative Block Diagram

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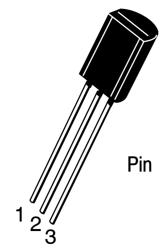
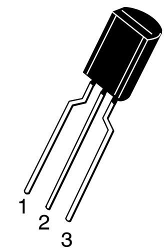


Pin 1. Reference
2. Anode
3. Cathode

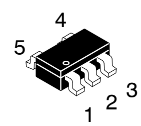


STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

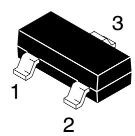
TO−92
LP SUFFIX
CASE 29−10

TO−92
LPRA, LPRE, LPRM, LPRP SUFFIX
CASE 29−10



Pin 1. NC
2. NC
3. Cathode
4. Reference
5. Anode

TSOP−5
SN SUFFIX
CASE 483



Pin 1. Reference
2. Cathode
3. Anode

SOT−23
SN1 SUFFIX
CASE 318

ORDERING INFORMATION

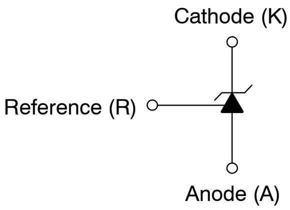
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

DEVICE MARKING INFORMATION AND PIN CONNECTIONS

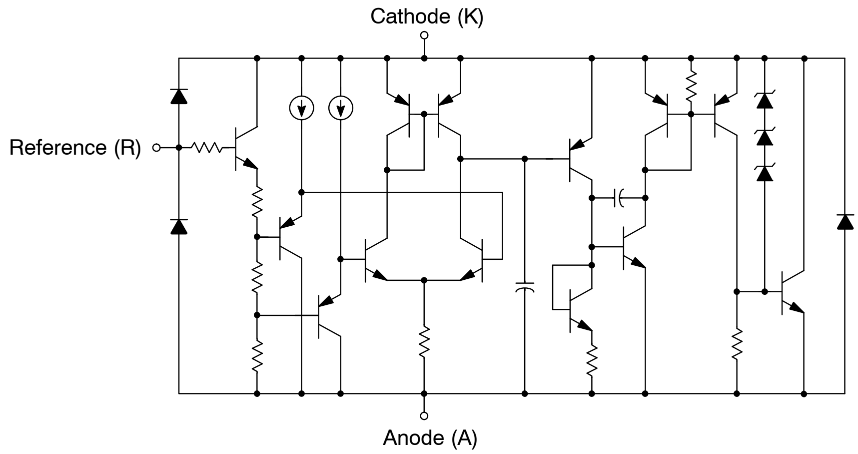
See general marking information in the device marking section on page 13 of this data sheet.

April, 2021 − Rev. 27

Publication Order Number:
TLV431A/D



Device Symbol



The device contains 13 active transistors.

Figure 2. Representative Device Symbol and Schematic Diagram

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	18	V
Cathode Current Range, Continuous	I_K	−20 to 25	mA
Reference Input Current Range, Continuous	I_{ref}	− 0.05 to 10	mA
Thermal Characteristics LP Suffix Package, TO−92−3 Package Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case SN Suffix Package, TSOP−5 Package Thermal Resistance, Junction−to−Ambient SN1 Suffix Package, SOT−23−3 Package Thermal Resistance, Junction−to−Ambient	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 178 83 226 491	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TLV431 NCV431, SCV431	T_A	− 40 to 85 − 40 to 125	°C
Storage Temperature Range	T_{stg}	− 65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per JEDEC JESD22−A114F, Machine Model Method 200 V per JEDEC JESD22−A115C,
Charged Device Method 1000 V per JEDEC JESD22−C101E. This device contains latch−up protection and exceeds ±100 mA per JEDEC standard JESD78.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

RECOMMENDED OPERATING CONDITIONS

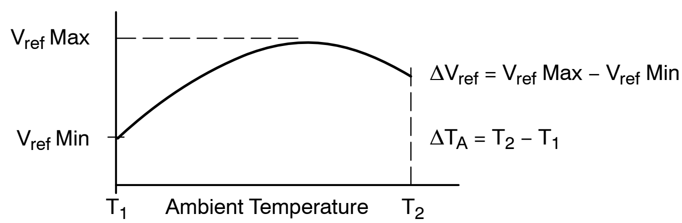
Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	16	V
Cathode Current	I_K	0.1	20	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	TLV431A			TLV431B			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage (Figure 3) (V_{KA} = V_{ref}, I_K = 10 mA, T_A = 25°C) (T_A = T_{low} to T_{high}, Note 1)	V_{ref}	1.228 1.215	1.240 –	1.252 1.265	1.234 1.228	1.240 –	1.246 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V_{KA} = V_{ref}, I_K= 10 mA, T_A = T_{low} to T_{high}, Notes 1, 2, 3)	ΔV_{ref}	–	7.2	20	–	7.2	20	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V_{KA} = V_{ref} to 16 V, I_K= 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–0.6	–1.5	–	–0.6	–1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open)	I_{ref}	–	0.15	0.3	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, Notes 1, 2, 3)	ΔI_{ref}	–	0.04	0.08	–	0.04	0.08	μA
Minimum Cathode Current for Regulation (Figure 3)	$I_{K(min)}$	–	30	80	–	30	80	μA
Off–State Cathode Current (Figure 5) (V_{KA} = 6.0 V, V_{ref} = 0) (V_{KA} = 16 V, V_{ref} = 0)	$I_{K(off)}$	– –	0.01 0.012	0.04 0.05	– –	0.01 0.012	0.04 0.05	μA
Dynamic Impedance (Figure 3) (V_{KA} = V_{ref}, I_K =0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 4)	$\lvert Z_{KA} \rvert$	–	0.25	0.4	–	0.25	0.4	Ω

1. Ambient temperature range: T_{low} = −40°C, T_{high} = 85°C.
2. Guaranteed but not tested.
3. The deviation parameters ΔV_{ref} and ΔI_{ref} are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{(\Delta V_{ref})}{V_{ref}\ (T_A = 25°C)} \times 10^6\right)}{\Delta T_A}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV_{ref} = 7.2 mV and the slope is positive,
V_{ref} @ 25°C = 1.241 V
ΔT_A = 125°C

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\frac{0.0072}{1.241} \times 10^6}{125} = 46\ ppm/°C$$

4. The dynamic impedance Z_{KA} is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

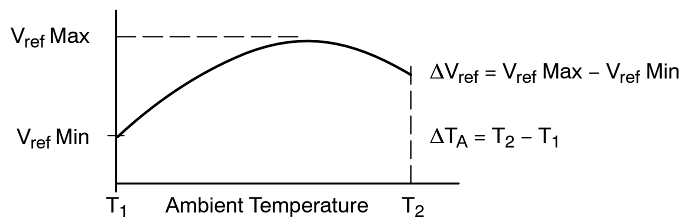
When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left(1 + \frac{R1}{R2}\right)$$

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	TLV431C			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) ($V_{KA} = V_{ref}$, I_K = 10 mA, T_A = 25°C) ($T_A = T_{low}$ to T_{high}, Note 5)	V_{ref}	 1.237 1.228	 1.240 –	 1.243 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) ($V_{KA} = V_{ref}$, I_K = 10 mA, $T_A = T_{low}$ to T_{high}, Notes 5, 6, 7)	ΔV_{ref}	–	7.2	20	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) ($V_{KA} = V_{ref}$ to 16 V, I_K = 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–0.6	–1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open)	I_{ref}	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, Notes 5, 6, 7)	ΔI_{ref}	–	0.04	0.08	μA
Minimum Cathode Current for Regulation (Figure 3)	$I_{K(min)}$	–	30	80	μA
Off−State Cathode Current (Figure 5) (V_{KA} = 6.0 V, V_{ref} = 0) (V_{KA} = 16 V, V_{ref} = 0)	$I_{K(off)}$	 – –	 0.01 0.012	 0.04 0.05	μA
Dynamic Impedance (Figure 3) ($V_{KA} = V_{ref}$, I_K = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 8)	$\lvert Z_{KA}\rvert$	–	0.25	0.4	Ω

5. Ambient temperature range: T_{low} = −40°C, T_{high} = 85°C.
6. Guaranteed but not tested.
7. The deviation parameters ΔV_{ref} and ΔI_{ref} are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{(\Delta V_{ref})}{V_{ref}\ (T_A = 25°C)} \times 10^6\right)}{\Delta T_A}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV_{ref} = 7.2 mV and the slope is positive,
V_{ref} @ 25°C = 1.241 V
ΔT_A = 125°C

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\frac{0.0072}{1.241} \times 10^6}{125} = 46\ ppm/°C$$

8. The dynamic impedance Z_{KA} is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

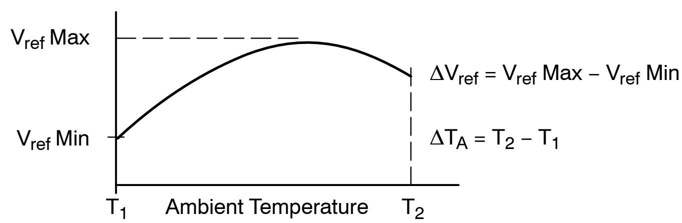
When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left(1 + \frac{R1}{R2}\right)$$

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT−23 package device.)

Characteristic	Symbol	NCV431A, SCV431A			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) (V_{KA} = V_{ref}, I_K = 10 mA, T_A = 25°C) (T_A = −40°C to 85°C) (T_A = −40°C to 125°C)	V_{ref}	 1.228 1.215 1.211	 1.240 – –	 1.252 1.265 1.265	V
Reference Input Voltage Deviation Over Temperature (Figure 3) (V_{KA} = V_{ref}, I_K= 10 mA, T_A = −40°C to 85°C, Notes 9, 10) (V_{KA} = V_{ref}, I_K= 10 mA, T_A = −40°C to 125°C, Notes 9, 10)	ΔV_{ref}	 – –	 7.2 7.2	 20 24	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) (V_{KA} = V_{ref} to 16 V, I_K= 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	−0.6	−1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open)	I_{ref}	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, T_A = −40°C to 85°C, Notes 9, 10) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, T_A = −40°C to 125°C, Notes 9, 10)	ΔI_{ref}	 – –	 0.04 –	 0.08 0.10	μA
Minimum Cathode Current for Regulation (Figure 3)	$I_{K(min)}$	–	30	80	μA
Off−State Cathode Current (Figure 5) (V_{KA} = 6.0 V, V_{ref} = 0) (V_{KA} = 16 V, V_{ref} = 0)	$I_{K(off)}$	 – –	 0.01 0.012	 0.04 0.05	μA
Dynamic Impedance (Figure 3) (V_{KA} = V_{ref}, I_K =0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 11)	$\lvert Z_{KA} \rvert$	–	0.25	0.4	Ω

9. Guaranteed but not tested.
10. The deviation parameters ΔV_{ref} and ΔI_{ref} are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{(\Delta V_{ref})}{V_{ref}\ (T_A = 25°C)} \times 10^6\right)}{\Delta T_A}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV_{ref} = 7.2 mV and the slope is positive,
V_{ref} @ 25°C = 1.241 V
ΔT_A = 125°C

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\frac{0.0072}{1.241} \times 10^6}{125} = 46\ ppm/°C$$

11. The dynamic impedance Z_{KA} is defined as:

$$\lvert Z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$$

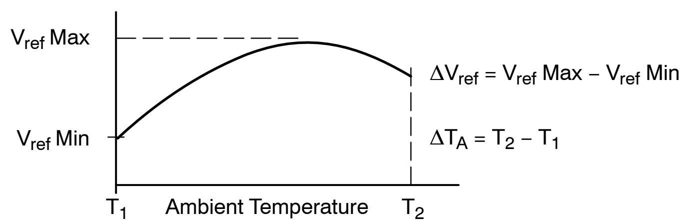
When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$\lvert Z_{KA}' \rvert = \lvert Z_{KA} \rvert \times \left(1 + \frac{R1}{R2}\right)$$

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT−23 package device.)

Characteristic	Symbol	NCV431B, SCV431B			Unit
		Min	Typ	Max	
Reference Voltage (Figure 3) ($V_{KA} = V_{ref}$, I_K = 10 mA, T_A = 25°C) (T_A = −40°C to 85°C) (T_A = −40°C to 125°C)	V_{ref}	 1.234 1.228 1.224	 1.240 – –	 1.246 1.252 1.252	V
Reference Input Voltage Deviation Over Temperature (Figure 3) ($V_{KA} = V_{ref}$, I_K= 10 mA, T_A = −40°C to 85°C, Notes 9, 10) ($V_{KA} = V_{ref}$, I_K= 10 mA, T_A = −40°C to 125°C, Notes 9, 10)	ΔV_{ref}	 – –	 7.2 7.2	 20 24	mV
Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4) ($V_{KA} = V_{ref}$ to 16 V, I_K= 10 mA)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	−0.6	−1.5	$\frac{mV}{V}$
Reference Terminal Current (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open)	I_{ref}	–	0.15	0.3	μA
Reference Input Current Deviation Over Temperature (Figure 4) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, T_A = −40°C to 85°C, Notes 12, 13) (I_K = 10 mA, R1 = 10 kΩ, R2 = open, T_A = −40°C to 125°C, Notes 12, 13)	ΔI_{ref}	 – –	 0.04 –	 0.08 0.10	μA
Minimum Cathode Current for Regulation (Figure 3)	$I_{K(min)}$	–	30	80	μA
Off−State Cathode Current (Figure 5) (V_{KA} = 6.0 V, V_{ref} = 0) (V_{KA} = 16 V, V_{ref} = 0)	$I_{K(off)}$	 – –	 0.01 0.012	 0.04 0.05	μA
Dynamic Impedance (Figure 3) ($V_{KA} = V_{ref}$, I_K =0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 14)	$\lvert Z_{KA}\rvert$	–	0.25	0.4	Ω

12. Guaranteed but not tested.
13. The deviation parameters ΔV_{ref} and ΔI_{ref} are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{(\Delta V_{ref})}{V_{ref}\ (T_A = 25°C)} \times 10^6\right)}{\Delta T_A}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV_{ref} = 7.2 mV and the slope is positive,
V_{ref} @ 25°C = 1.241 V
ΔT_A = 125°C

$$\alpha V_{ref}\left(\frac{ppm}{°C}\right) = \frac{\frac{0.0072}{1.241} \times 10^6}{125} = 46\ ppm/°C$$

14. The dynamic impedance Z_{KA} is defined as:

$$\lvert Z_{KA}\rvert = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$\lvert Z_{KA}'\rvert = \lvert Z_{KA}\rvert \times \left(1 + \frac{R1}{R2}\right)$$

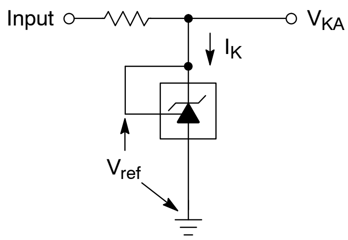


Figure 3. Test Circuit for $V_{KA} = V_{ref}$

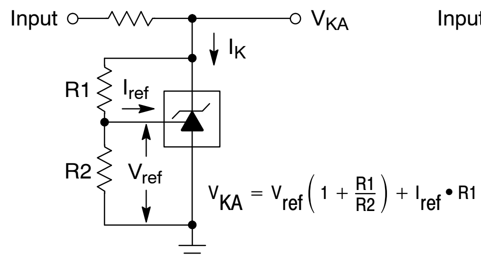


Figure 4. Test Circuit for $V_{KA} > V_{ref}$

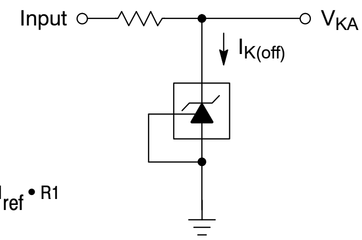


Figure 5. Test Circuit for $I_{K(off)}$

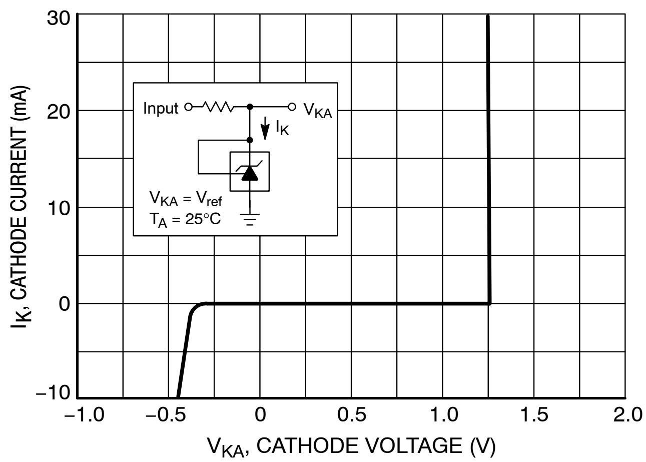


Figure 6. Cathode Current vs. Cathode Voltage

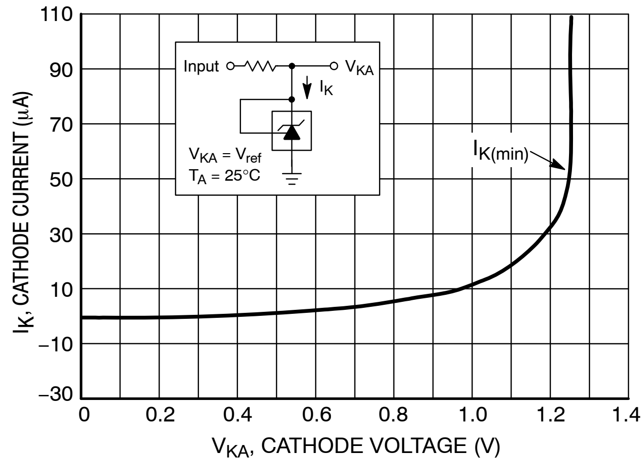


Figure 7. Cathode Current vs. Cathode Voltage

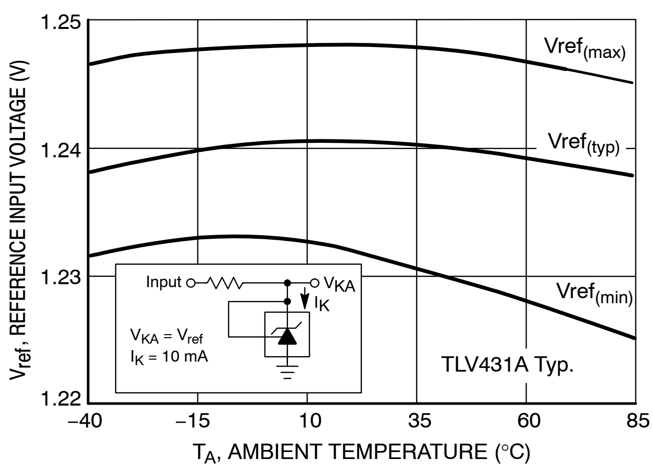


Figure 8. Reference Input Voltage versus Ambient Temperature

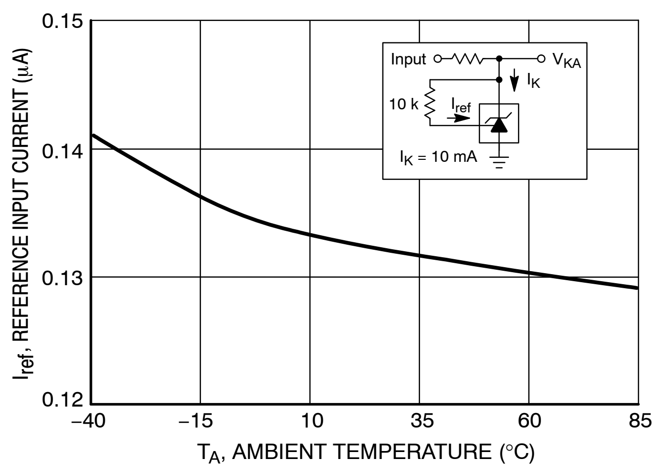


Figure 9. Reference Input Current versus Ambient Temperature

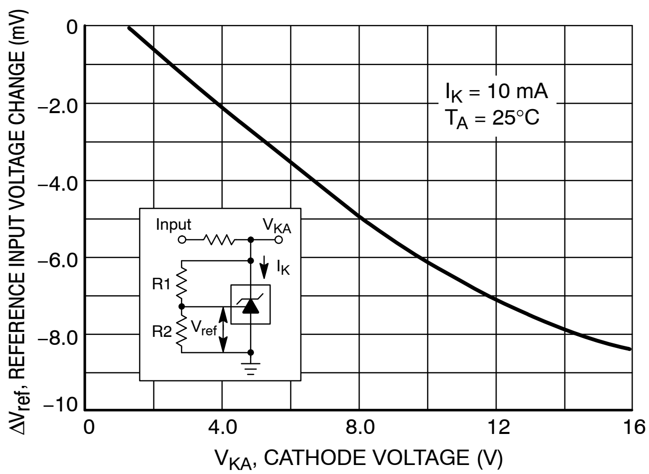


Figure 10. Reference Input Voltage Change versus Cathode Voltage

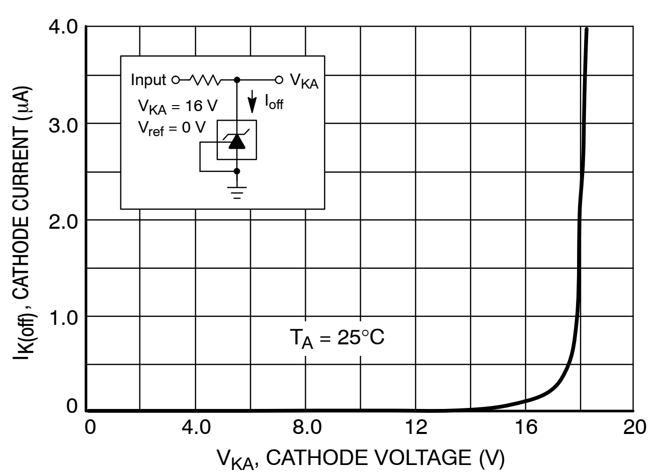


Figure 11. Off-State Cathode Current versus Cathode Voltage

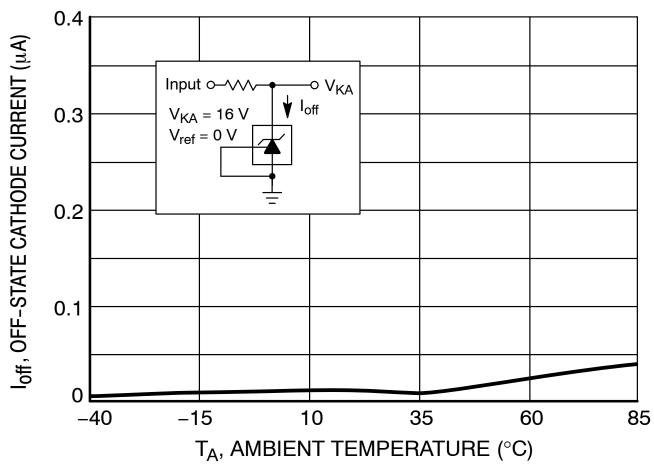


Figure 12. Off-State Cathode Current versus Ambient Temperature

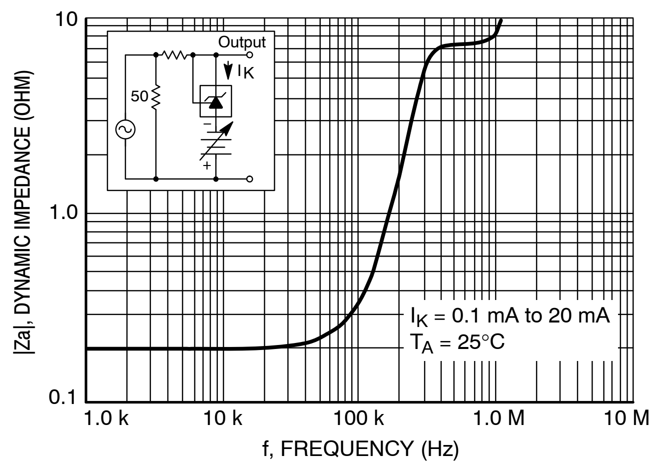


Figure 13. Dynamic Impedance versus Frequency

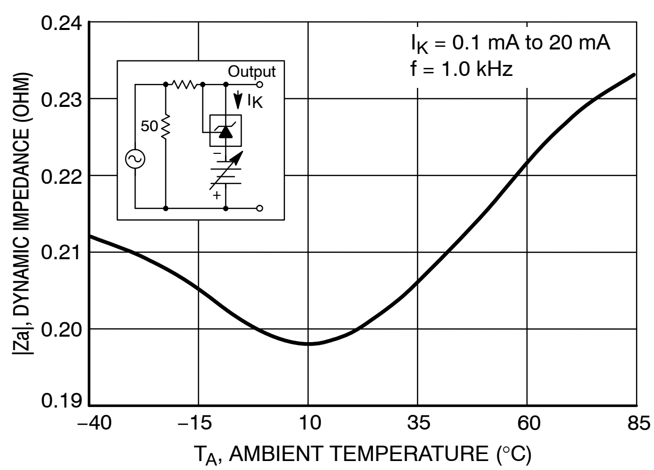


Figure 14. Dynamic Impedance versus Ambient Temperature

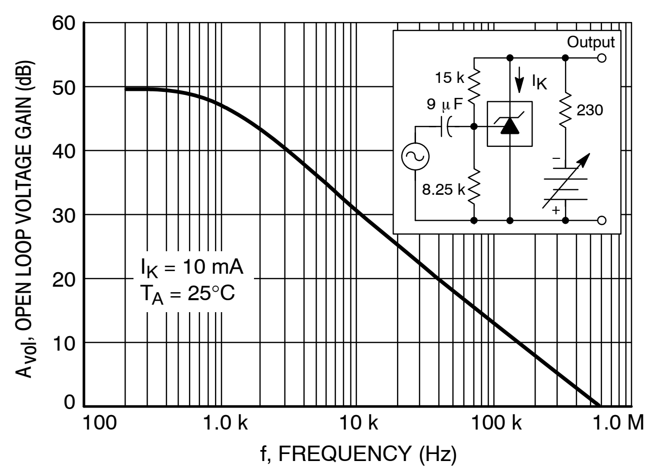


Figure 15. Open-Loop Voltage Gain versus Frequency

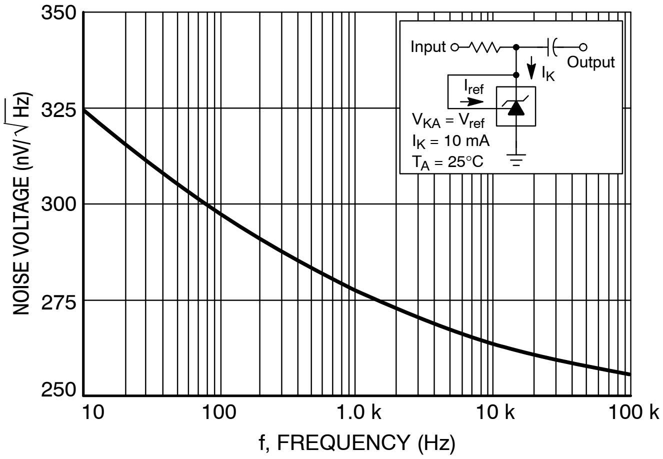


Figure 16. Spectral Noise Density

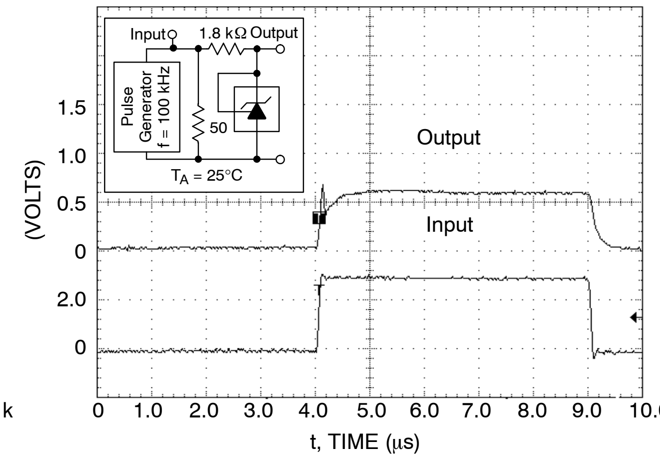


Figure 17. Pulse Response

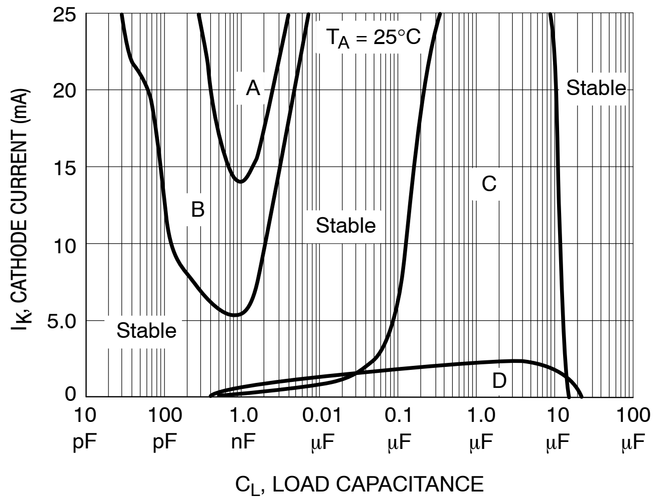
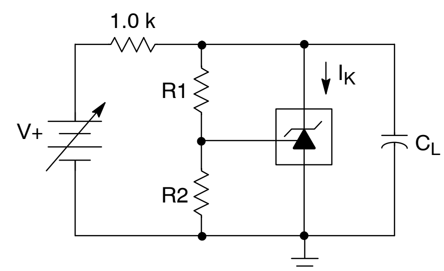


Figure 18. Stability Boundary Conditions



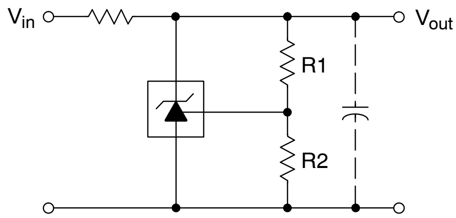
Unstable Regions	V_{KA} (V)	R1 (kΩ)	R2 (kΩ)
A, C	V_{ref}	0	∞
B, D	5.0	30.4	10

Figure 19. Test Circuit for Figure 18

Stability

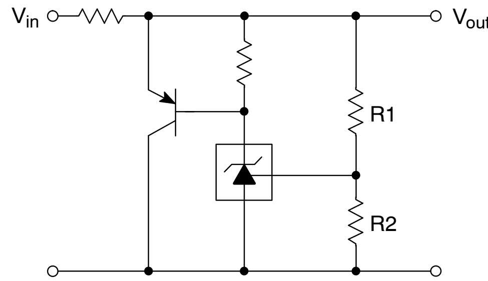
Figures 18 and 19 show the stability boundaries and circuit configurations for the worst case conditions with the load capacitance mounted as close as possible to the device. The required load capacitance for stable operation can vary depending on the operating temperature and capacitor equivalent series resistance (ESR). Ceramic or tantalum surface mount capacitors are recommended for both temperature and ESR. The application circuit stability should be verified over the anticipated operating current and temperature ranges.

TYPICAL APPLICATIONS



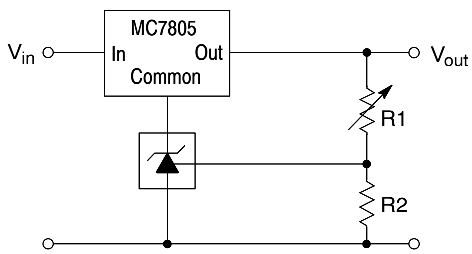
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 20. Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

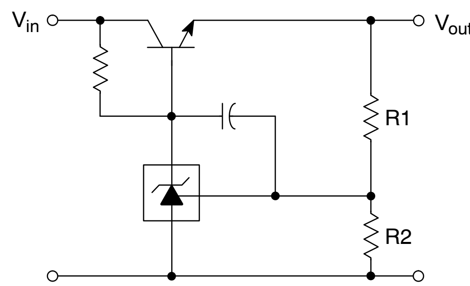
Figure 21. High Current Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{out(min)} = V_{ref} + 5.0\ V$$

Figure 22. Output Control for a Three Terminal Fixed Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{in(min)} = V_{out} + V_{be}$$

$$V_{out(min)} = V_{ref}$$

Figure 23. Series Pass Regulator

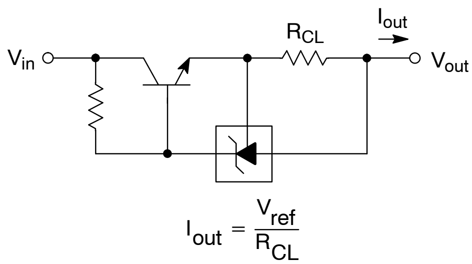


Figure 24. Constant Current Source

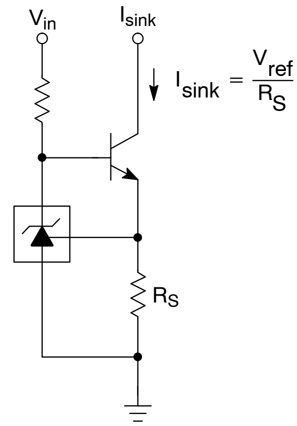


Figure 25. Constant Current Sink

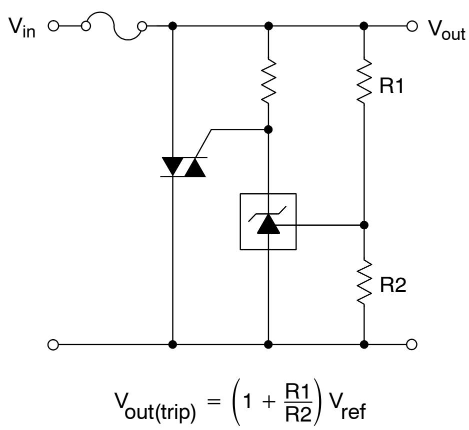


Figure 26. TRIAC Crowbar

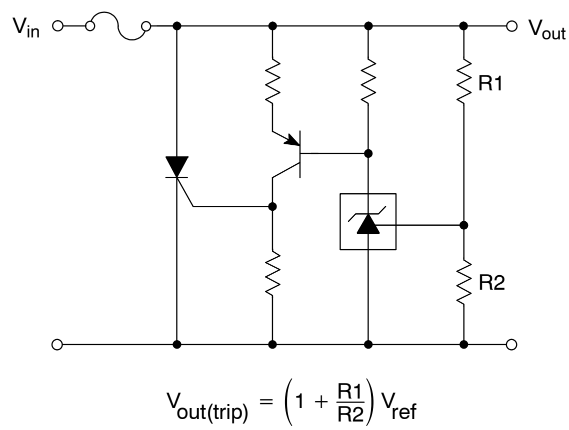
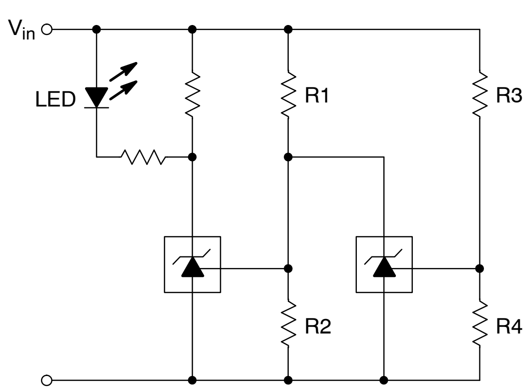


Figure 27. SCR Crowbar



L.E.D. indicator is ‘ON’ when V_{in} is between the upper and lower limits,

$$\text{Lower limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 28. Voltage Monitor

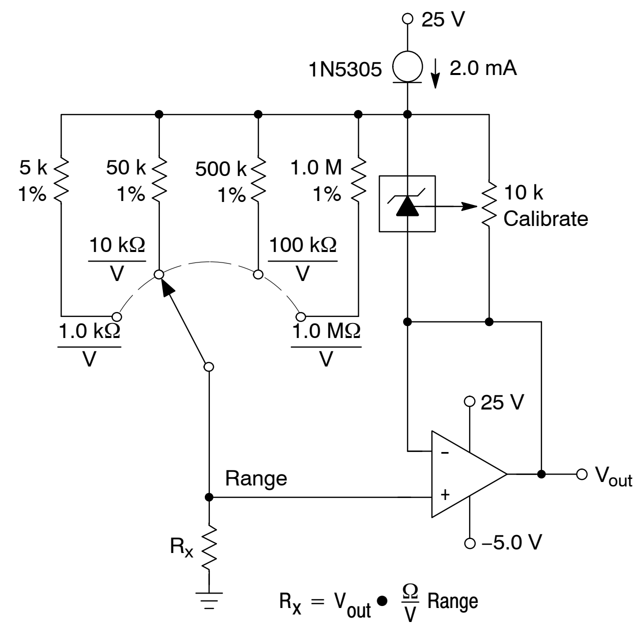


Figure 29. Linear Ohmmeter

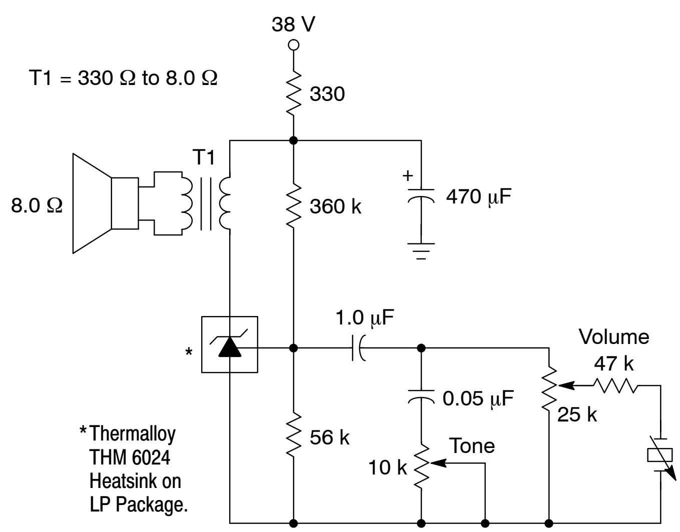


Figure 30. Simple 400 mW Phono Amplifier

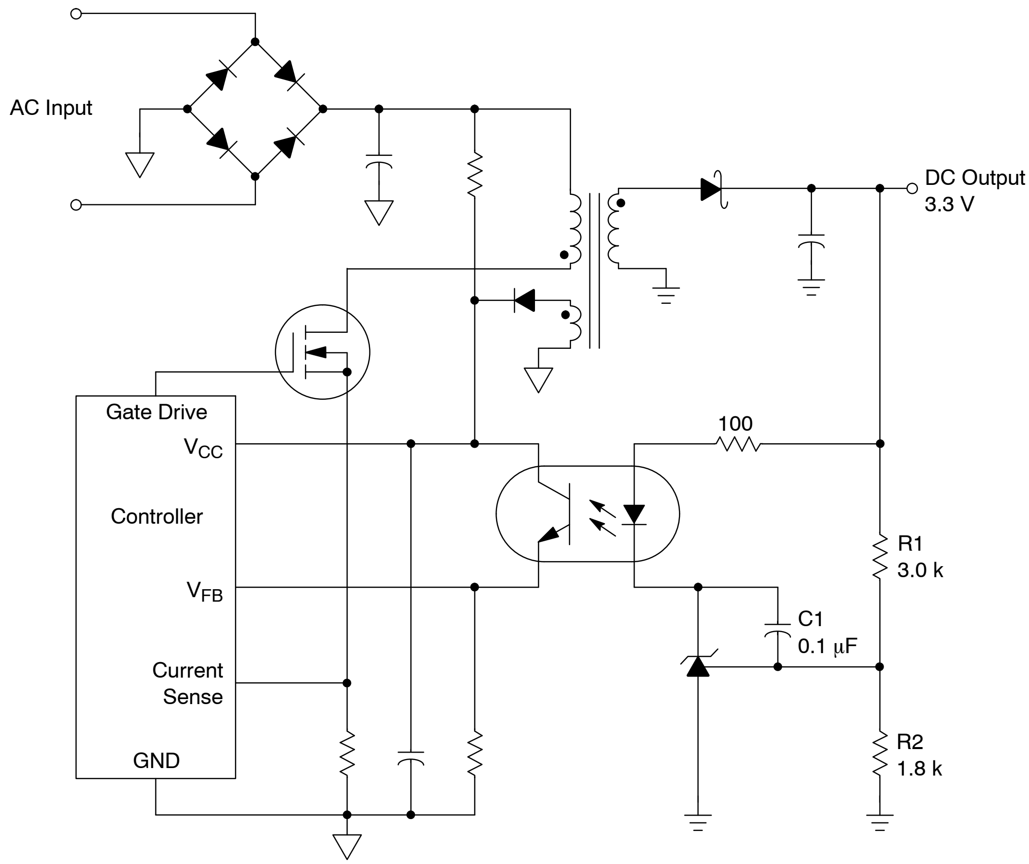
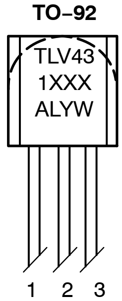


Figure 31. Isolated Output Line Powered Switching Power Supply

The above circuit shows the TLV431A/B/C as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resistors values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V, and is limited by the sum of the reference voltage (1.24 V) and the forward drop of the optocoupler light emitting diode (1.4 V). Capacitor C1 provides loop compensation.

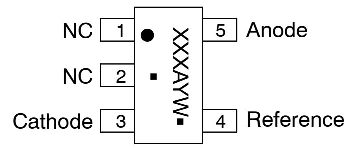
PIN CONNECTIONS AND DEVICE MARKING

TO−92



1. Reference
2. Anode
3. Cathode

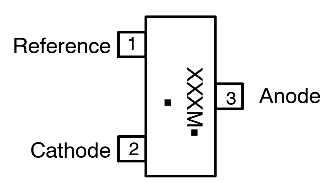
TSOP−5



(Top View)

XXX = Specific Device Code
A = Assembly Location
Y = Year
L = Wafer Lot
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

SOT−23−3



(Top View)

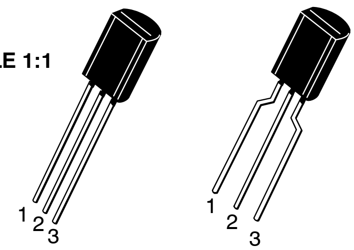
XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Device Code	Package	Shipping†
TLV431ALPG	ALP	TO−92−3 (Pb−Free)	6000 / Box
TLV431ALPRAG	ALP	TO−92−3 (Pb−Free)	2000 / Tape & Reel
TLV431ALPREG	ALP	TO−92−3 (Pb−Free)	2000 / Tape & Reel
TLV431ALPRMG	ALP	TO−92−3 (Pb−Free)	2000 / Ammo Pack
TLV431ALPRPG	ALP	TO−92−3 (Pb−Free)	2000 / Ammo Pack
TLV431ASNT1G	RAA	TSOP−5 (Pb−Free, Halide−Free)	3000 / Tape & Reel
TLV431ASN1T1G	RAF	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel
TLV431BLPG	BLP	TO−92−3 (Pb−Free)	6000 / Box
TLV431BLPRAG	BLP	TO−92−3 (Pb−Free)	2000 / Tape & Reel
TLV431BLPREG	BLP	TO−92−3 (Pb−Free)	2000 / Tape & Reel
TLV431BLPRMG	BLP	TO−92−3 (Pb−Free)	2000 / Ammo Pack
TLV431BLPRPG	BLP	TO−92−3 (Pb−Free)	2000 / Ammo Pack
TLV431BSNT1G	RAH	TSOP−5 (Pb−Free, Halide−Free)	3000 / Tape & Reel
TLV431BSN1T1G	RAG	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel
TLV431CSN1T1G	AAN	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel
SCV431ASN1T1G*	RAE	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel
SCV431BSN1T1G*	RAC	SOT−23−3 (Pb−Free, Halide−Free)	3000 / Tape & Reel
NCV431ASNT1G*	ACH	TSOP−5 (Pb−Free, Halide−Free)	3000 / Tape & Reel
NCV431BSNT1G*	AD6	TSOP−5 (Pb−Free, Halide−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*SCV, NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SCALE 1:1

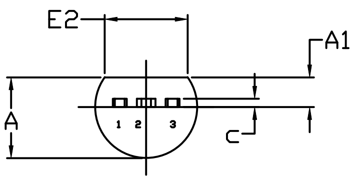


STRAIGHT LEAD BENT LEAD

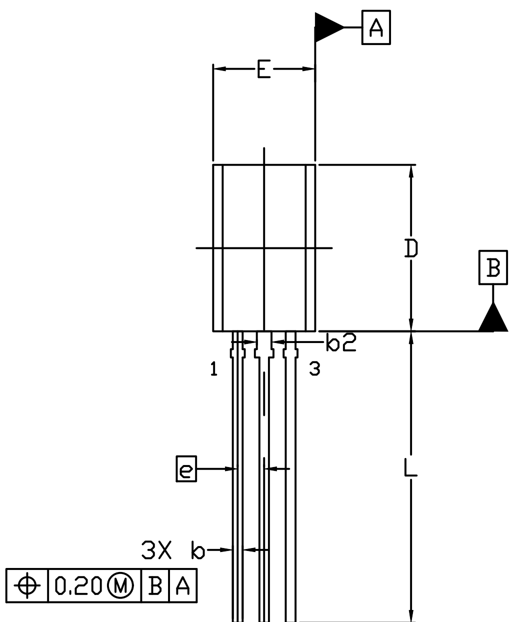
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

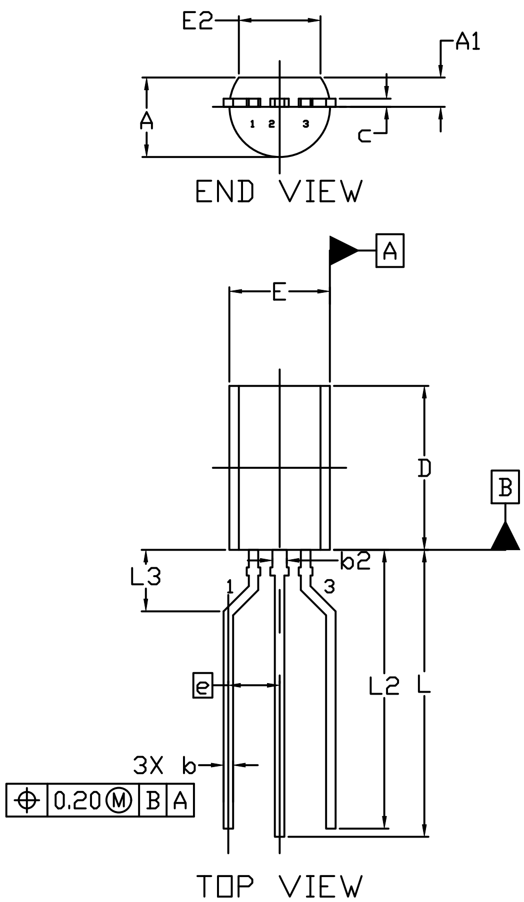
STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−92 (TO−226) 1 WATT	PAGE 1 OF 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 2 OF 3**

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC MARKING DIAGRAM*

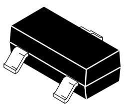
XXXXX
XXXXX
ALYW▪
▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

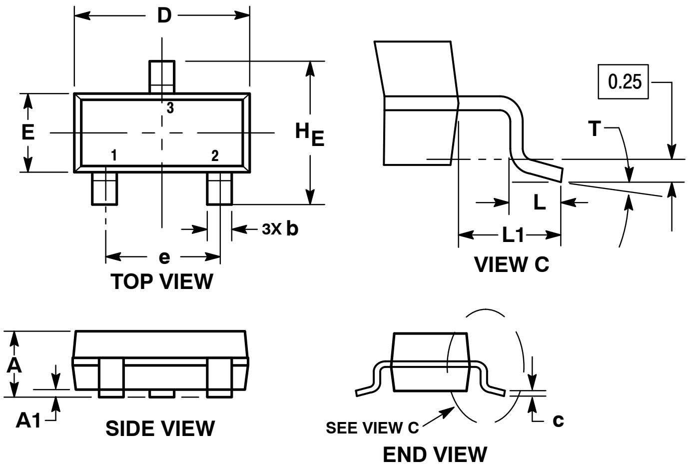
DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−92 (TO−226) 1 WATT	PAGE 3 OF 3



SCALE 4:1

SOT−23 (TO−236)
CASE 318−08
ISSUE AS

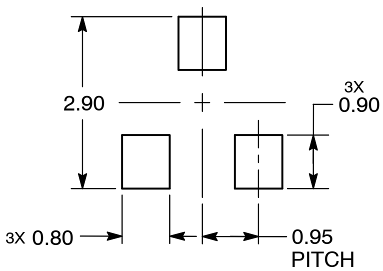
DATE 30 JAN 2018



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

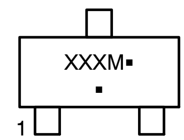
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

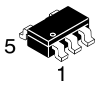
STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

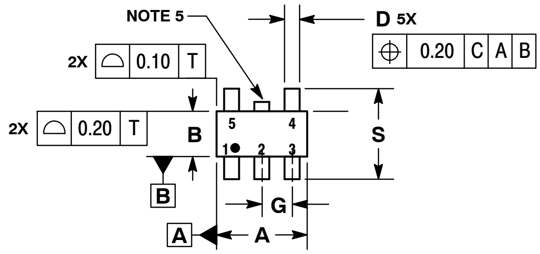
DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−23 (TO−236)	PAGE 1 OF 1



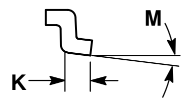
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

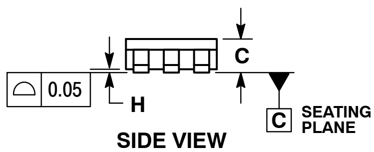
DATE 12 AUG 2020



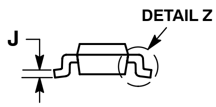
TOP VIEW



DETAIL Z



SIDE VIEW

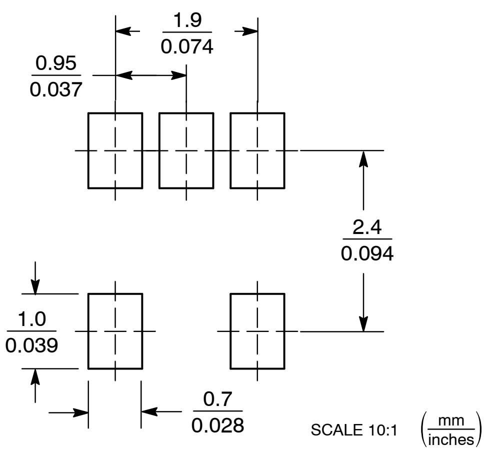


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

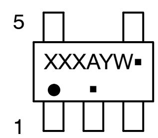
	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*

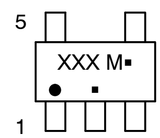


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	TSOP−5	PAGE 1 OF 1

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