



# FCAB21520L1

## Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

### ■ Features

- Source-source ON resistance:RSS(on) typ. = 1.6 mΩ (VGS = 3.8 V)
- CSP(Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1)

### ■ Marking Symbol: 7T

### ■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

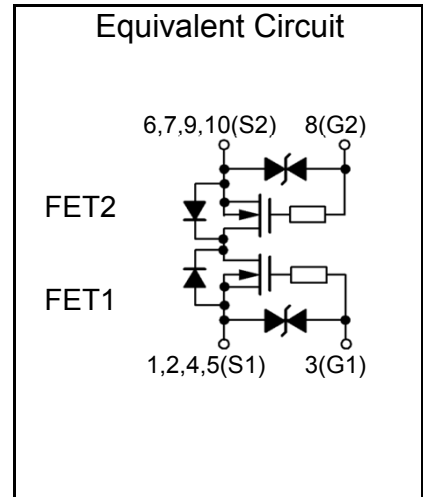
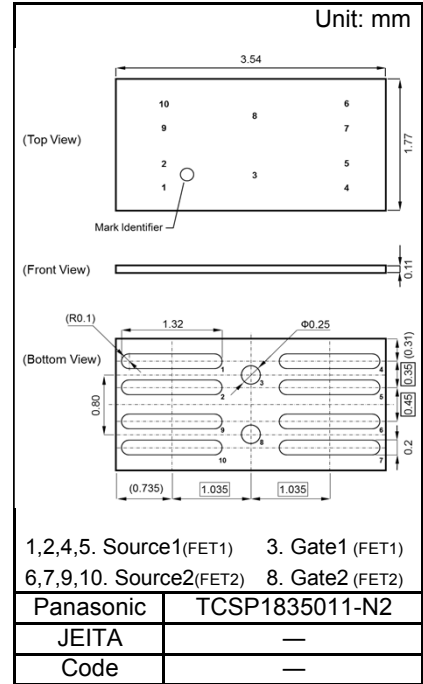
### ■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	±8	V
Source Current	DC <sup>*1</sup>	IS1	16
	DC <sup>*2</sup>	IS2	35
	Pulse <sup>*3</sup>	ISp	160
Total Power Dissipation	DC <sup>*1</sup>	PD1	0.54
	DC <sup>*2</sup>	PD2	3.8
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Thermal Resistance (ch-a)	Rth <sup>*1</sup>	232	°C/W
	Rth <sup>*2</sup>	33	°C/W

Note \*1 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm )  
using the minimum recommended pad size (36 μm Copper ).

\*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).

\*3 t = 10 μs, Duty Cycle ≤ 1 %



■ Electrical Characteristics Ta = 25 °C ± 3 °C

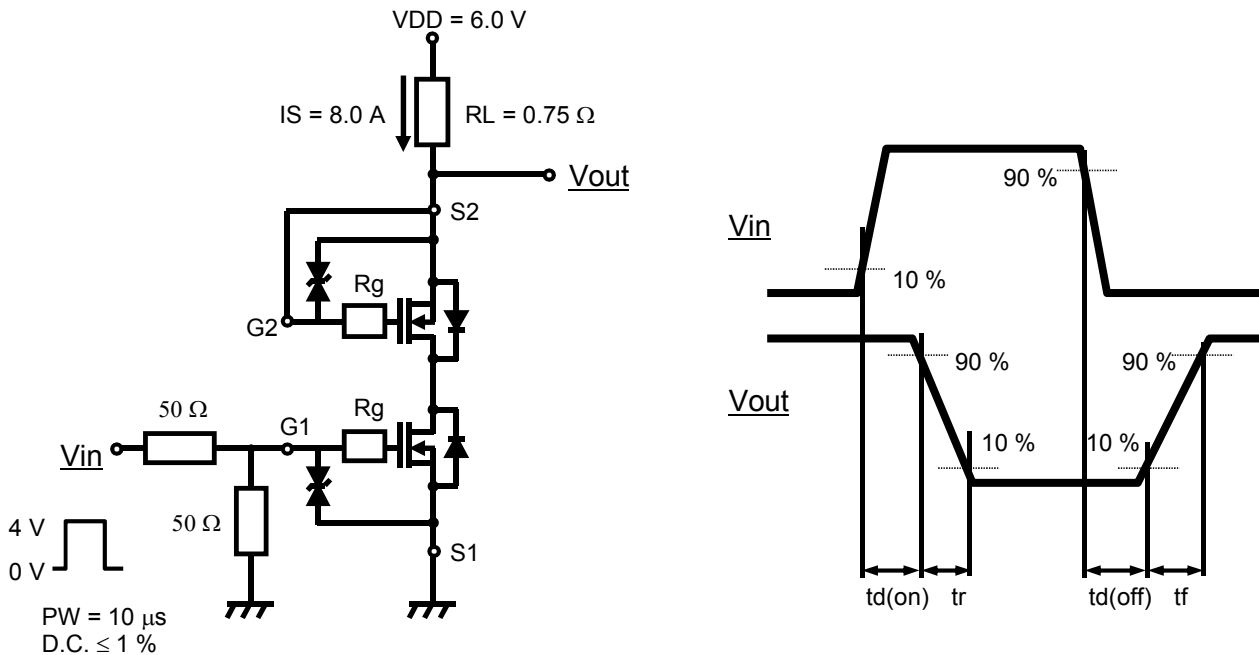
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1.0 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
		VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 1.64 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 8.0 A, VGS = 4.5 V	1.1	1.45	2.0	mΩ
	RSS(on)2	IS = 8.0 A, VGS = 3.8 V	1.15	1.6	2.1	
	RSS(on)3	IS = 8.0 A, VGS = 3.1 V	1.2	1.8	3.0	
	RSS(on)4	IS = 8.0 A, VGS = 2.5 V	1.4	2.3	4.5	
Body Diode Forward Voltage	VF(s-s)	IF = 8.0 A, VGS = 0 V		0.7	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		5250		pF
Output Capacitance *1	Coss			700		
Reverse Transfer Capacitance *1	Crss			630		
Turn-on Delay Time *1,*2	td(on)	VDD = 6.0 V, VGS = 0 to 4.0 V		1.5		μs
Rise Time *1,*2	tr	IS = 8.0 A		2.6		
Turn-off Delay Time *1,*2	td(off)	VDD = 6.0 V, VGS = 4.0 to 0 V		6.8		μs
Fall Time *1,*2	tf	IS = 8.0 A		4.1		
Total Gate Charge *1	Qg	VDD = 6.0 V		38		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4.0 V		20		
Gate-drain Charge *1	Qgd	IS = 8.0 A		10		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

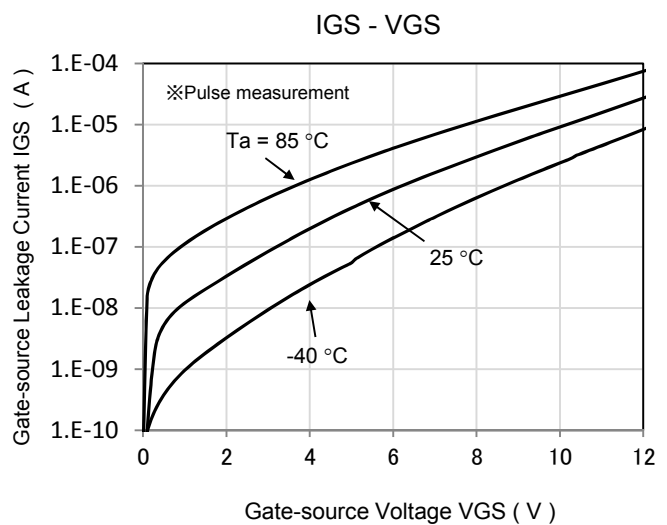
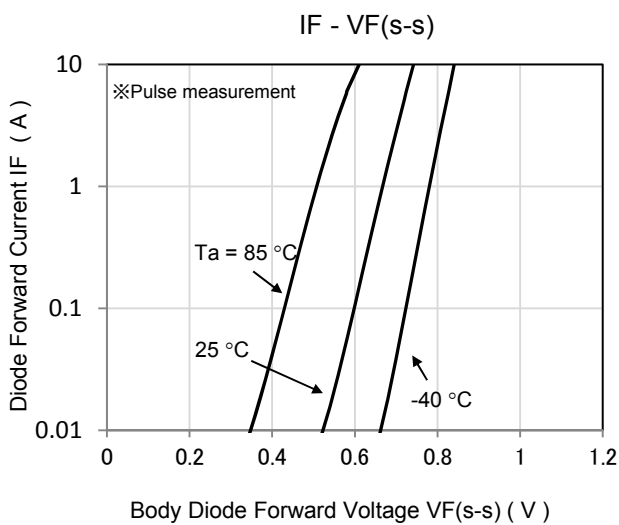
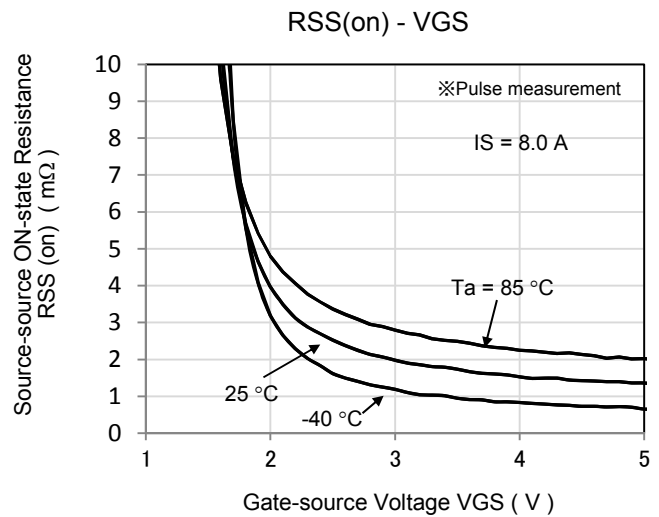
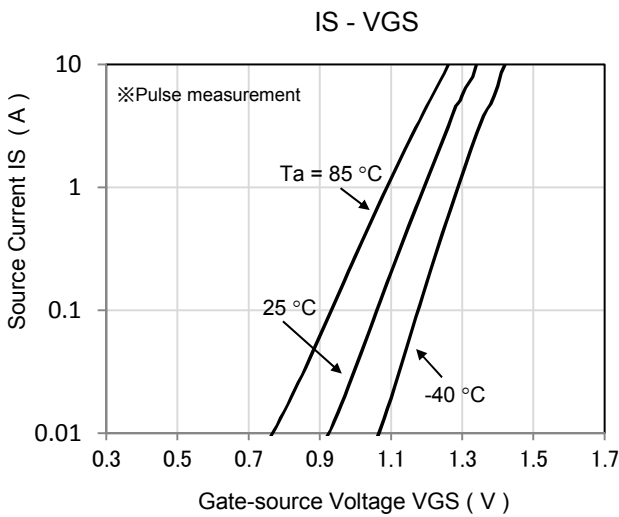
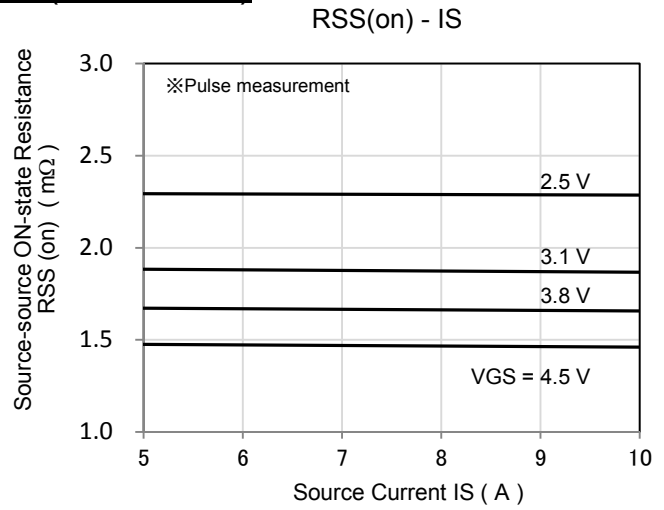
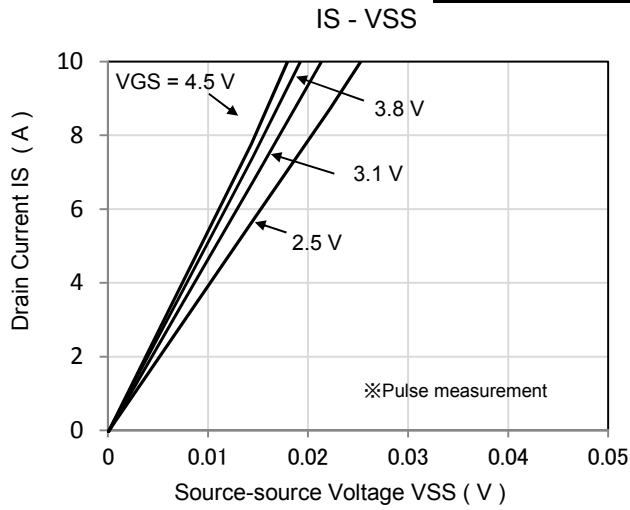
\*1 Guaranteed by design, not subject to production testing

\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

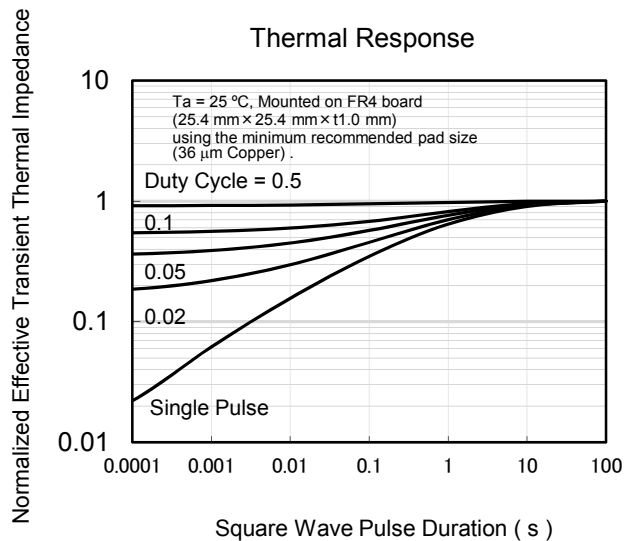
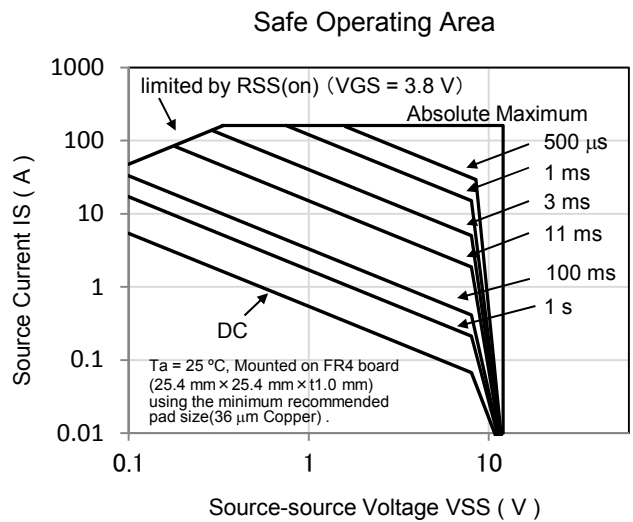
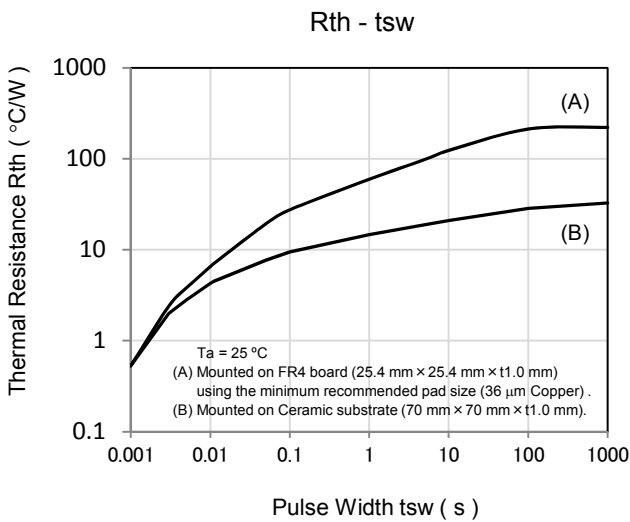
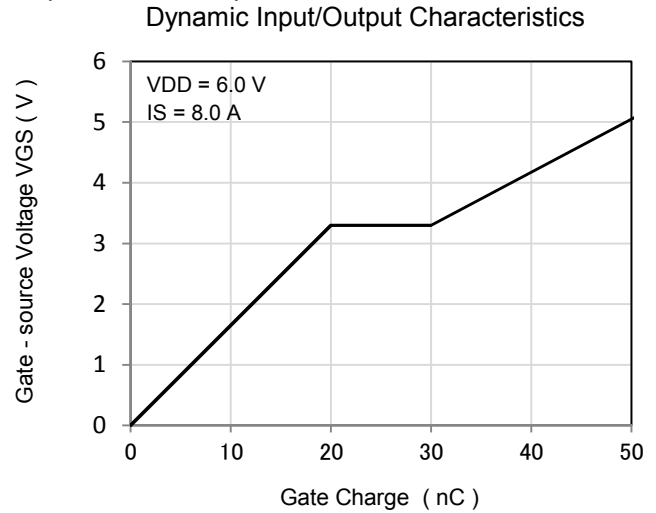
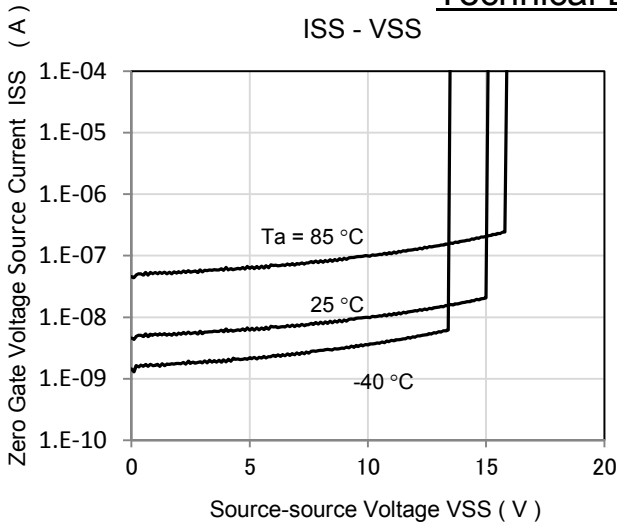
Note2: Measurement circuit



Technical Data ( reference )

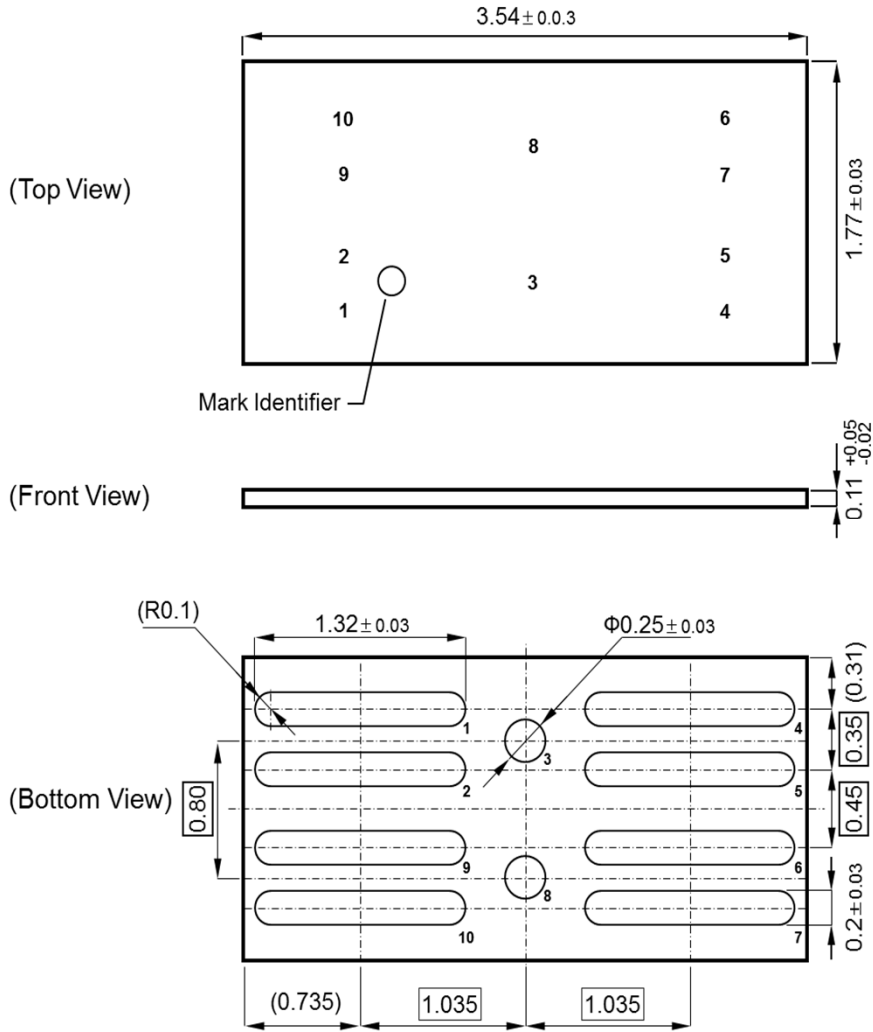


Technical Data ( reference )



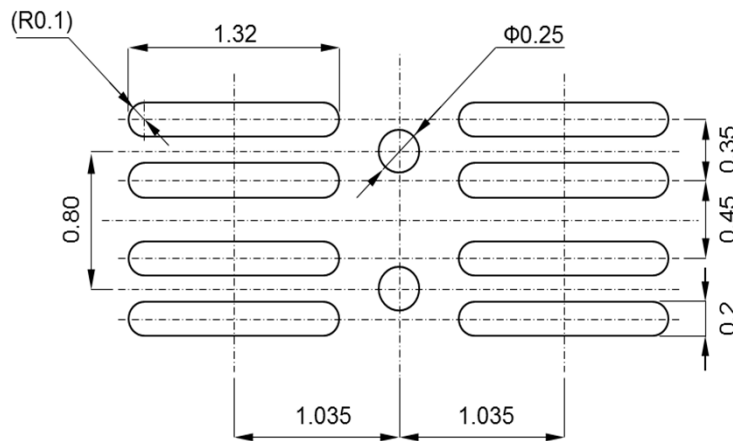
■ Outline

Unit : mm



■ Land Pattern (Reference)

Unit : mm



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