MN101EA8/A7/A3/A2 Series

8-bit Single-chip Microcontroller

■ Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EFA7G/A8G/A2G/A3G have an internal 128 KB of ROM and 6 KB of RAM. MN101EFA7D/A8D/A2D/A3D have an internal 64 KB of ROM and 4 KB of RAM. Peripheral functions include 5 external interrupts, including NMI, 10 timer counters, 4 types of serial interfaces, A/D converter, watchdog timer and buzzer output. The system configuration is suitable for system control microcontroller.

With 3 oscillation systems (internal frequency: 16 MHz, high-speed crystal/ceramic frequency: max. 10 MHz, low-speed crystal/ceramic frequency: 32.768 kHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode), or low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Capacitive Touch Detection Circuit	Package
MN101EFA8D	64 KB	4 KB	Flash EEPROM version	○	LQFP080-P-1414E TQFP080-P-1212F
MN101EFA8G	128 KB	6 KB			
MN101EFA3D	64 KB	4 KB		—	
MN101EFA3G	128 KB	6 KB			
MN101EFA7D	64 KB	4 KB		○	LQFP064-P-1414 TQFP064-P-1010D
MN101EFA7G	128 KB	6 KB			
MN101EFA2D	64 KB	4 KB		—	
MN101EFA2G	128 KB	6 KB			

■ Features

- Memory Capacity:
  ROM 128 KB / 64 KB
  RAM 6 KB / 4 KB

- Package:
  MN101EFA8/A3
    80-Pin TQFP (12 mm × 12 mm / 0.50 mm pitch)
    80-Pin LQFP (14 mm × 14 mm / 0.65 mm pitch)

  MN101EFA7/A2
    64-Pin TQFP (10 mm × 10 mm / 0.50 mm pitch)
    64-Pin LQFP (14 mm × 14 mm / 0.80 mm pitch)

- Machine Cycle:
  High-speed mode 0.05 µs / 20 MHz (4.0 V to 5.5 V)
  Low-speed mode 62.5 µs / 32 kHz (4.0 V to 5.5 V)

- Oscillation circuit: 3 channel oscillation circuit
  Internal oscillation (frc): 16 MHz
  Crystal/ceramic (fosc): Maximum 10 MHz
  Crystal/ceramic (fx): Maximum 32.768 kHz

- Clock Multiplication circuit (PLL Circuit)
  PLL circuit output clock (fpll): fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
  1/2 × frc multiplication by 4, 5 enable

- Clock Gear for System Clock
  System Clock (fs): fpll divided by 1, 2, 4, 16, 32, 64, 128

- Clock Gear for control clock of peripheral function
  Control clock of peripheral function (fpll-div): stop or fpll divided by 1, 2, 4, 8, 16

- Memory Bank:
  Expands data memory space by the bank system (by 64 KB, 16 banks)
  Source address bank / Destination address bank

- Operation Mode:
  NORMAL mode (High-speed mode)
  SLOW mode (Low-speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)

- Operating Voltage:
  4.0 V to 5.5 V

- Operation ambient temperature:
  –40 °C to + 85 °C

■ Features (continued)

- Interrupt:

MN101EFA8: 36 interrupts
MN101EFA3: 28 interrupts
MN101EFA7: 32 interrupts
MN101EFA2: 28 interrupts

<Non-maskable interrupt>
Non-maskable interrupt and Watchdog timer overflow interrupt

<Timer interrupts>
Timer 0 interrupt
Timer 1 interrupt
Timer 2 interrupt
Timer 3 interrupt
Timer 6 interrupt
Time base timer interrupt
Timer 7 interrupt
Timer 7 compare register 2 match interrupt
Timer 8 interrupt
Timer 8 compare register 2 match interrupt
Timer 9 overflow interrupt
Timer 9 underflow interrupt
Timer 9 compare register 2 match interrupt

<Serial Interface interrupts>
Serial interface 0 interrupt
Serial interface 0 UART reception interrupt
Serial interface 1 interrupt
Serial interface 1 UART reception interrupt
Serial interface 2 interrupt
Serial interface 2 UART reception interrupt
Serial interface 4 interrupt
Serial interface 4 stop condition interrupt

<A/D interrupt>
A/D conversion interrupt

<External interrupts>
IRQ0: Edge selectable, noise filter connection available
IRQ1: Edge selectable, noise filter connection available
IRQ2: Edge selectable, noise filter connection available, both edges interrupt
IRQ3: Edge selectable, noise filter connection available, both edges interrupt
IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

■ Features (continued)

- Interrupt (Continued)

<Touch Detect interrupts>

Touch 0 : (MN101EFA3/A2 don't have this function)
- Touch 0 detect interrupt
- Touch 0 detect error interrupt
- Touch 0 round interrupt
- Touch 0 data transmission interrupt

Touch 1 : (MN101EFA3/A2 don't have this function)
- Touch 1 detect interrupt
- Touch 1 detect error interrupt
- Touch 1 round interrupt
- Touch 1 data transmission interrupt

- Timer counter: 10 timers

8-bit timer for general use × 4 sets
16-bit timer for general use × 2 sets
Motor control 16-bit timer × 1 set
8-bit free-run timer × 1 set
Time base timer × 1 set
Baud rate timer × 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM0IOA
- Event count
- Simple pulse measurement
- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 1 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM1IOA
- Event count
- 16-bit cascade connected (with Timer 0)
- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 2 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOA
- Event count
- Simple pulse measurement
- 24-bit cascade connected (with Timer 0 and Timer 1)
- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 3 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM3IOA
- Event count
- 16-bit cascade connected (with Timer 2)
- 32-bit cascade connected (with Timer 0 and Timer 1 and Timer 2)
- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

■ Features (continued)

- Timer counter (continued)

Timer 6 (8-bit free-run timer, Time base timer)

8-bit free-run timer

Clock source: fpll-div, fpll-div/2^{12}, fpll-div/2^{13}, fs, fx, fx/2^2, fx/2^3, fx/2^{12}, fx/2^{13}

Time base timer

Interrupt generation cycle: fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fx/2^7, fx/2^8, fx/2^9, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)

Square wave output (Timer pulse output)

High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOA

Event count

Input capture function (Both edges can be operated)

Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16, Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 8 (16-bit timer for general use)

Square wave output (Timer pulse output)

High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOA

Event count

Input capture function (Both edges can be operated)

Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16, Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 9 (Motor control 16-bit timer)

Square wave output (Timer pulse output) can be output to large current pin TM9IOA

Event count

Complementary 3-phase PWM output can be output to large current pin TM9OD0 to TM9OD5

(Triangle wave and saw tooth wave are supported, dead time insertion available)

Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16, Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer A (Baud rate timer)

Clock output for peripheral functions

Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

- Watchdog timer

Time-out cycle can be selected from fs/2^{16}, fs/2^{18}, fs/2^{20}

On detection of 2 errors, forcibly hard reset inside LSI.

Operation start timing is selectable. (At reset release or write to register)

- Buzzer Output/ Reverse Buzzer Output

Output frequency can be selected from fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{11}, fpll-div/2^{12}, fpll-div/2^{13}, fpll-div/2^{14}, fx/2^3, fx/2^4

- A/D Converter:

10-bit × 16 channels (MN101EFA8/A3)

10-bit × 12 channels (MN101EFA7/A2)

■ Features (continued)

- Serial Interface: 4 channels

Serial 0: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
Sequence transmission, reception or both are available
Full duplex UART
Baud rate timer, selected from Timer 0 to 3 or Timer A
Parity check, overrun error/ framing error detection
Transfer size 7 to 8 bits can be selected

Serial 1: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
Sequence transmission, reception or both are available.
Full duplex UART
Baud rate timer, selected from Timer 0 to 3 or Timer A
Parity check, overrun error/ framing error detection
Transfer size 7 to 8 bits can be selected

Serial 2: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
Sequence transmission, reception or both are available.
Full duplex UART
Baud rate timer, selected from Timer 0 to 3 or Timer A
Parity check, overrun error/ framing error detection
Transfer size 7 to 8 bits can be selected

Serial 4: Multi master IIC/ Clock synchronous
Clock synchronous serial interface
Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/32, fs/2, fs/4,
Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
Sequence transmission, reception or both are available.
Multi master IIC
7-bit slave address is settable.
General call communication mode is supported.

- Automatic Reset:

Power detection level: 4.3 V (at rising), 4.2 V (at falling)

- LED Driver:

8 pins (Port A)

- Touch Sensor TImer:

2 unit/ 12 channels (MN101EFA8 only)
1 unit/ 8 channels (MN101EFA7 only)

■ Features (continued)

- Ports

(MN101EFA8/A3)

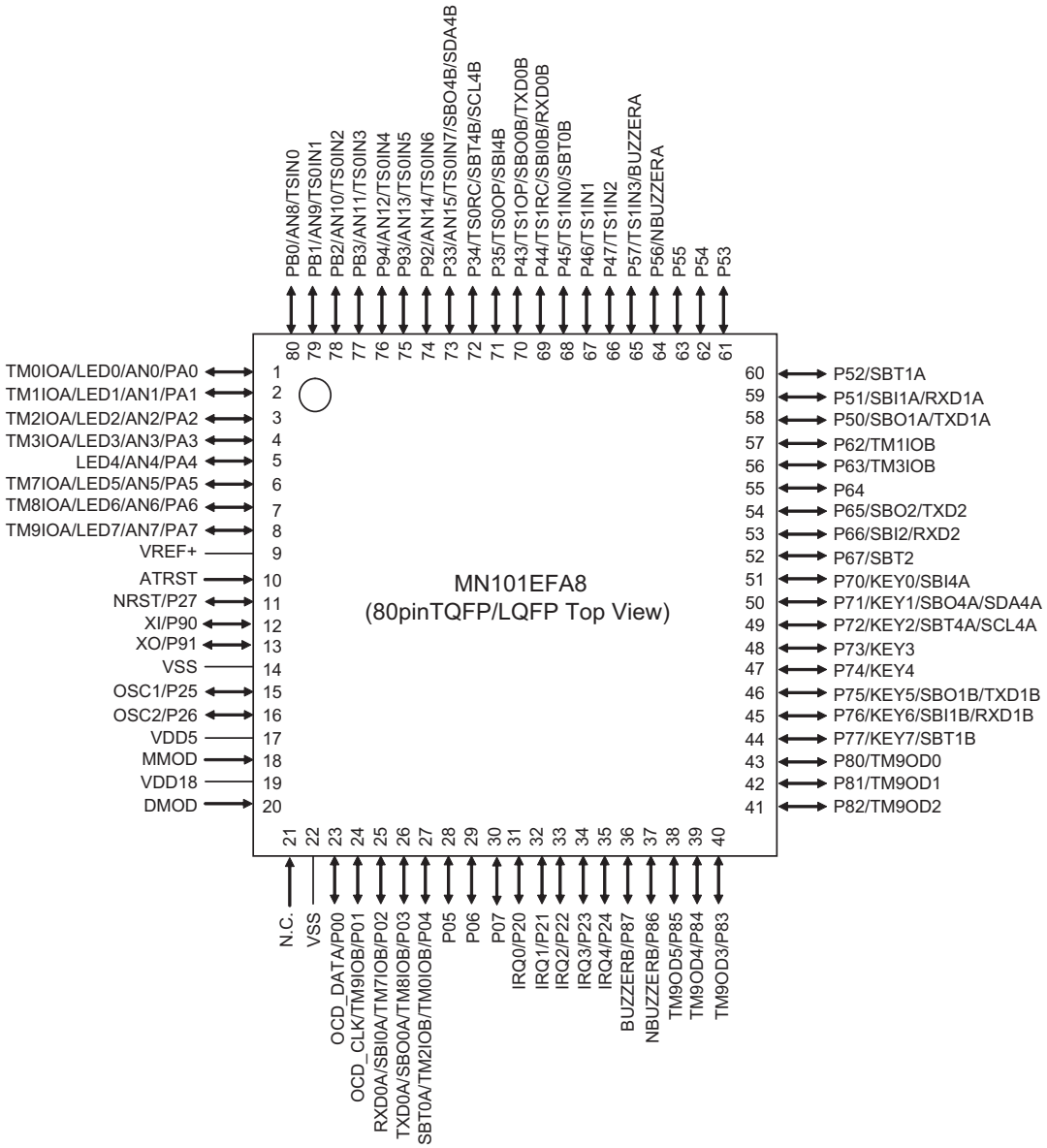
I/O ports	70 pins
Serial Interface pins	21 pins
Timer I/O	19 pins
Buzzer output pins	4 pins
A/D input pins	16 pins
External Interrupt pins	5 pins
LED (large current) driver	8 pins
Touch sensor input pins	12 pins (MN101EFA3 does not have this function)
Touch sensor resistor connect pins	4 pins (MN101EFA3 does not have this function)
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	9 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	4 pins

(MN101EFA7/A2)

I/O ports	55 pins
Serial Interface pins	15 pins
Timer I/O	9 pins
Buzzer output	4 pins
A/D input pins	12 pins
External Interrupt pins	5 pins
LED (large current) driver	8 pins
Touch sensor input pins	8 pins (MN101EFA2 does not have this function)
Touch sensor resistor connect pins	2 pins (MN101EFA2 does not have this function)
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	3 pins

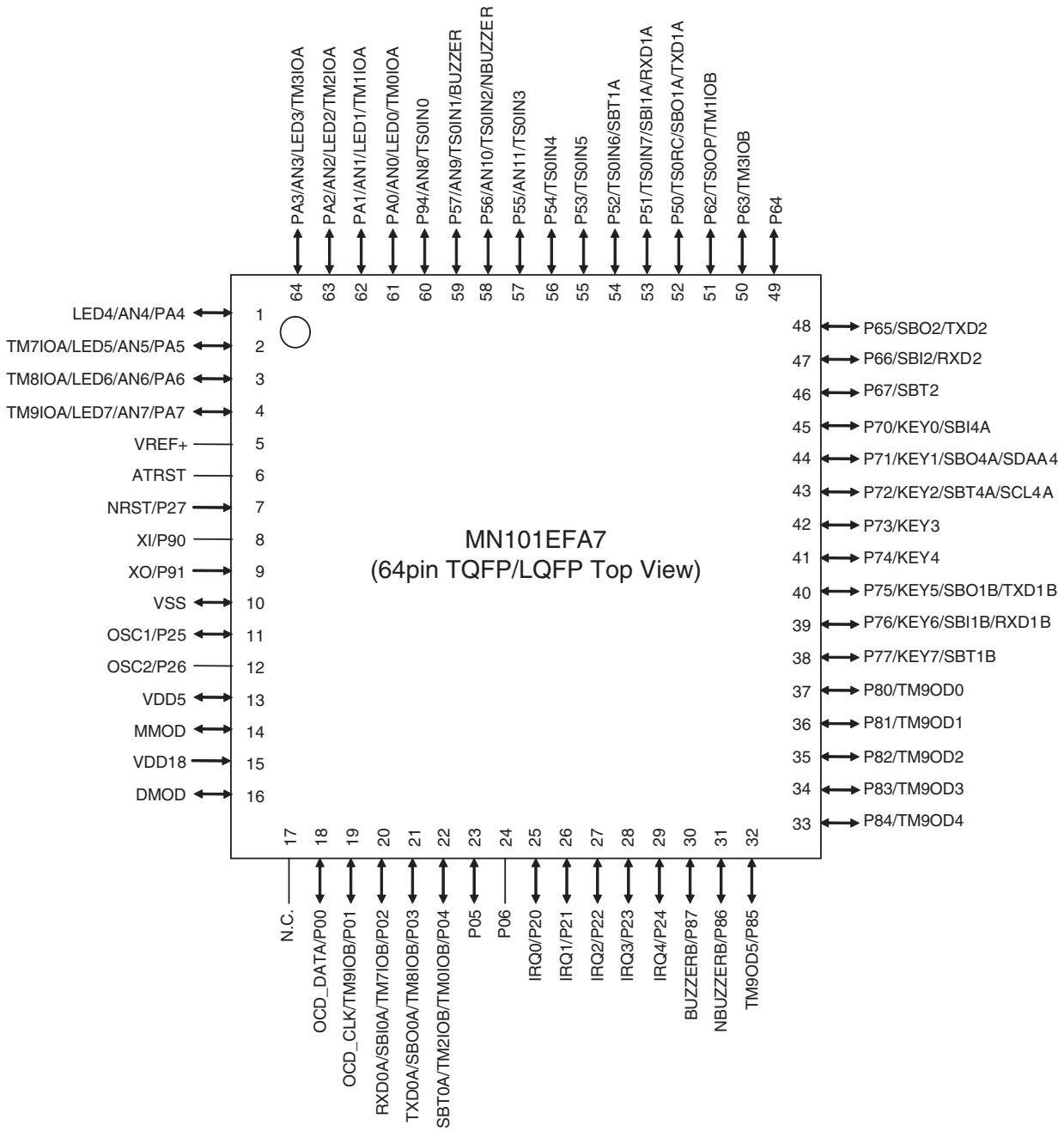
■ Pin Description

- MN101EFA8 (TQFP080-P-1212F, LQFP080-P-1414E)



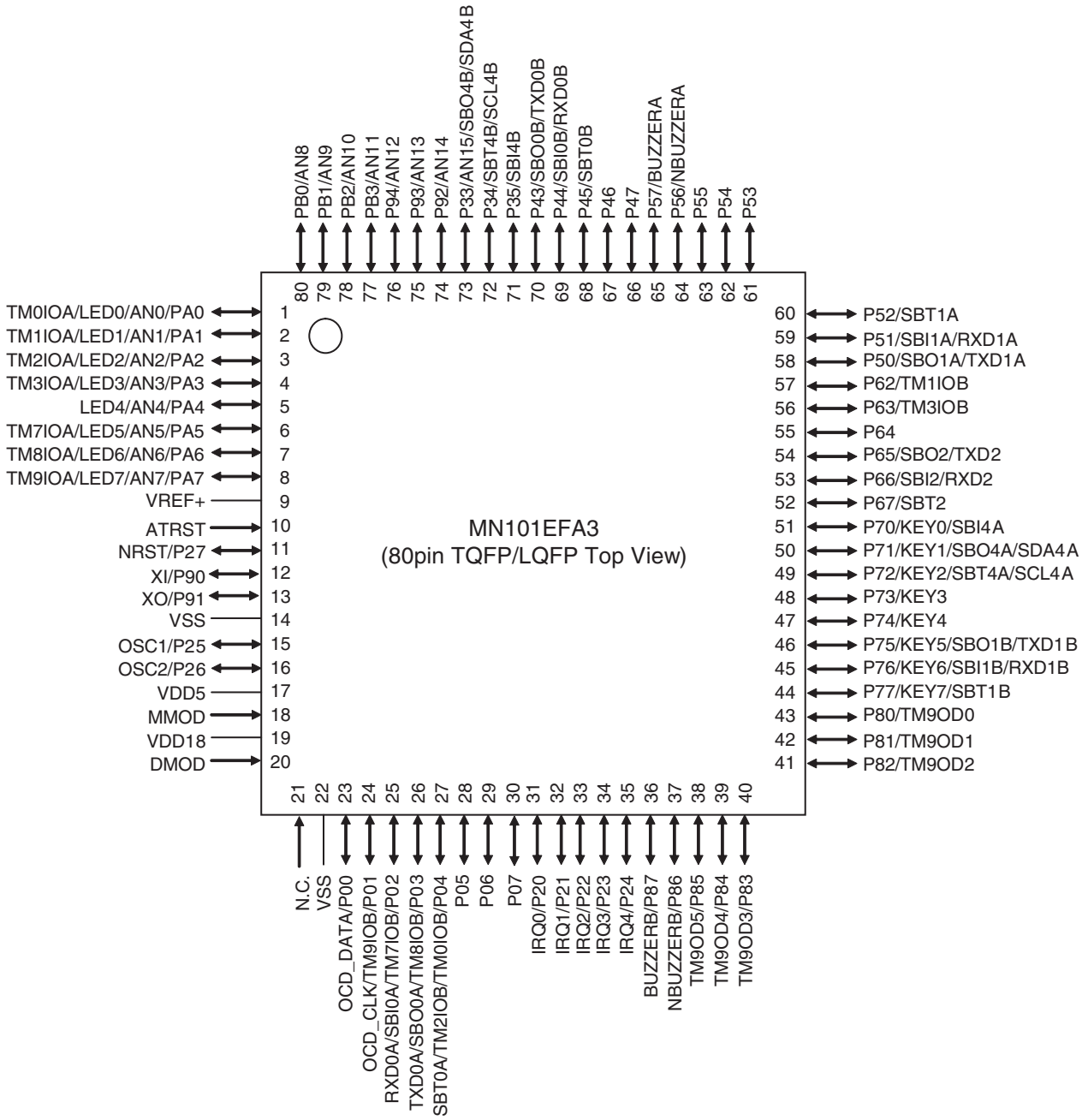
■ Pin Description (continued)

• MN101EFA7 (TQFP064-P-1010D, LQFP064-P-1414)



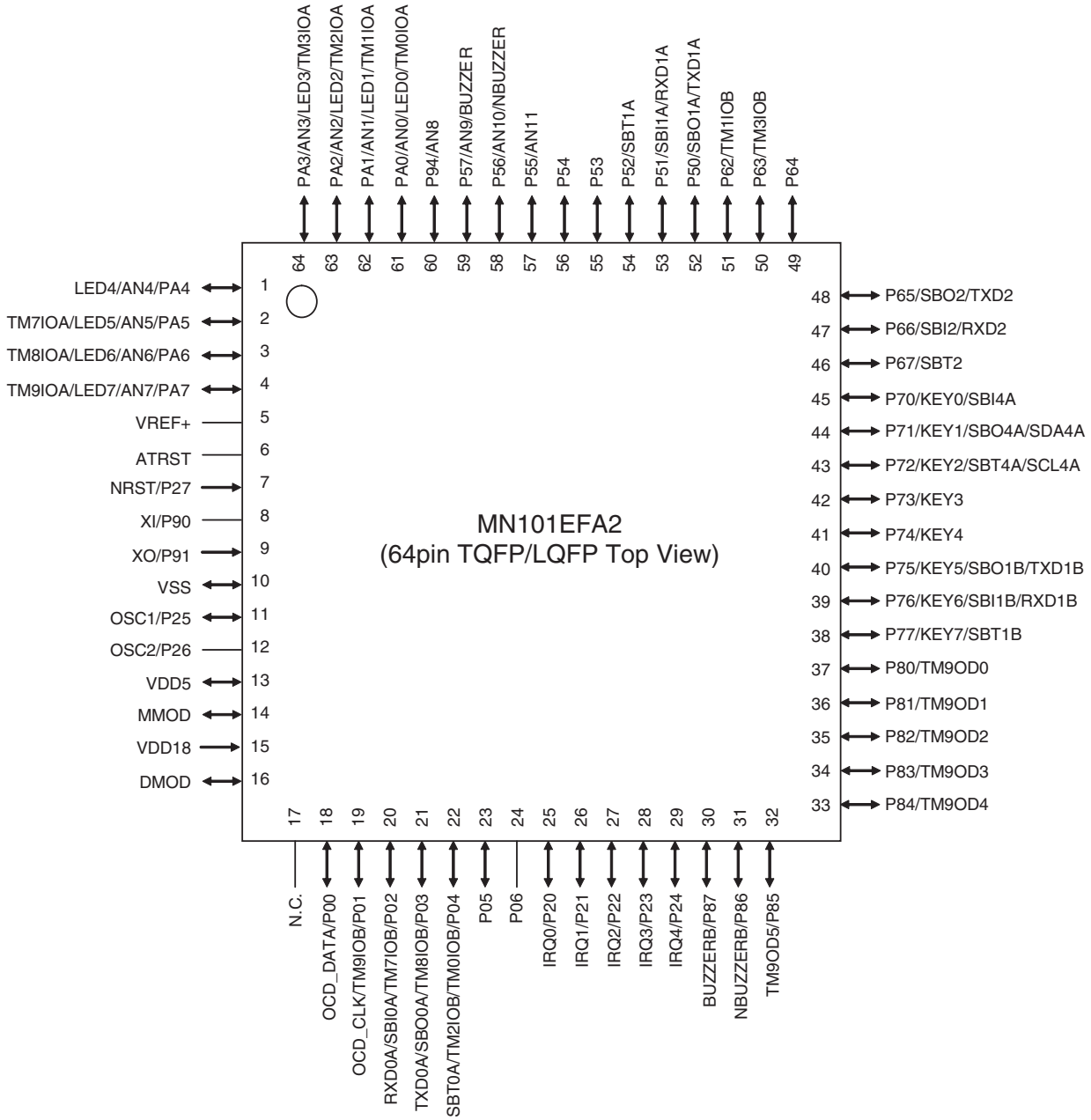
■ Pin Description (continued)

• MN101EFA3 (TQFP080-P-1212F, LQFP080-P-1414E)



■ Pin Description (continued)

• MN101EFA2 (TQFP064-P-1010D, LQFP064-P-1414)



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