Evaluation board circuit diagram and implementation MN63Y1212/1213

Ver. 1.0

Sep.5<sup>th</sup>,2013

Semiconductor Business Group Industrial Devices Company Panasonic Corporation

## 2 MN63Y1212/1213 Pin layout

Sep.5th,2013



Din No	Name		Innut/Output	10 turns	Function
Pin No.  1  2  3  4  5  6  7	MN63Y1212	MN63Y1213	Input/Output	ютуре	Function
1	VB	VB	I/O		Coil terminal
Pin No.     MI       1     -       2     -       3     -       4     -       5     -       6     -       7     -       8     -	N.C.	VDDEX		/ Power	MN63Y1212: Open or Connect to Ground
					MN63Y1213: External Power Supply
3	VSS	VSS		GND	Ground
4	VA	VA	I/O		Coil terminal
-	NIRQ	NIRQ	Output	Open Drain	USE : Pull up to VDD
5					NOT USE : Open or Connect to Ground (same as Pin No.2)
6	N.C.	SCL	/ Input	/ Open Drain	MN63Y1212: Open or Connect to Ground (same as Pin No.2)
					MN63Y1213: I2C Clock input
7	N.C.	SDA	/ I/O	/ Open Drain	MN63Y1212: Open or Connect to Ground (same as Pin No.2)
					MN63Y1213: I2C Data input/output
0				Bower	Internal analog power supply
0	VUDA	VDDA		Fower	(Connect a capacitor between this pin and VSS shortest as possible.)

### 3 Pattern of the evaluation board (40mm x 30mm Antenna)

Sep.5th,2013



※ Substrate size may differ from the substrate which exists to a visitor.
※ I connect pulling up resistance (R,R2,R3) to the microcomputer board of our offer.

External parts	Recommended Value	Detail explanation
R2,R3	3.3kΩ	These are pull up resistor for I2C signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board "ANT4030_02_0505_B0_L," it is not implemented.
R4	3.3kΩ	This is pull up resistor for interrupt signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board "ANT4030_02_0505_B0_L," it is not implemented.
C1、C2	2.2µF	It is a fixed value at the capacity between the power supply for operation stabilization of the tag LSI. C2 is connected to VDDD, and C3 is connected to VDDA and C4 is connected to VDDEX.
R1	200Ω	Please set 200 ohm when use VDEEX between 2.5 to 3.6 V ( Default value ) Please set 0 ohm when use VDEEX between 1.7V to 2.5V ( Short JP1 )

# 4 Pattern of the evaluation board (20mm x 20mm Antenna)

Sep.5th,2013



※ Substrate size may differ from the substrate which exists to a visitor.
 ※ I connect pulling up resistance (R,R2,R3) to the microcomputer board of our offer.

External parts	Recommended Value	Detail explanation
R2,R3	3.3kΩ	These are pull up resistor for I2C signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board "ANT4030_02_0505_B0_L ," it is not implemented.
R4	3.3kΩ	This is pull up resistor for interrupt signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board "ANT4030_02_0505_B0_L ," it is not implemented.
C1、C2	2.2µF	It is a fixed value at the capacity between the power supply for operation stabilization of the tag LSI. C2 is connected to VDDD, and C3 is connected to VDDA and C4 is connected to VDDEX.
R1	200Ω	Please set 200 ohm when use VDEEX between 2.5 to 3.6 V ( Default value ) Please set 0 ohm when use VDEEX between 1.7V to 2.5V ( Short JP1 )

#### ■ ANT2020 02 0505 B0 L 1213 V0

### Connection with host micon

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#### NFC tag system constitution







## Connecter specification(1)

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Micon board [BTPB101-B]



DF11CZ-8DP-2V(27) (Hirose Electric)

2		VSS	1
4	SDA	SCL	3
6	NIRQ		5
8	VDDEX		7

-			_	1
8	VDDEX		7	
6	NIRQ		5	
4	SDA	SCL	3	
2		VSS	1	

HRS DF11CZ- 8DS-2V (Hirose Electric)

#### Antenna board [ANT4030\_02\_0505\_B0\_L\_1213\_V0]





Sep.5th,2013



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