



PJA3419

20V P-Channel Enhancement Mode MOSFET– ESD Protected

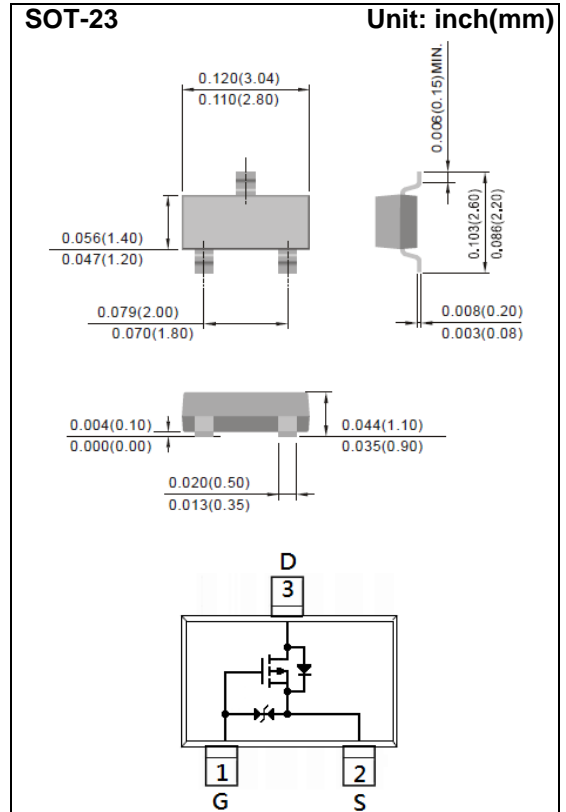
Voltage **-20 V** **Current** **-4.0A**

Features

- RDS(ON) , VGS@-10V, ID@-4.0A<60mΩ
- RDS(ON) , VGS@-4.5V, ID@-3.3A<70mΩ
- RDS(ON) , VGS@-2.5V, ID@-2.0A<96mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case : SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0003 ounces, 0.0084 grams
- Marking : A19



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±12	V
Continuous Drain Current	I _D	-4.0	A
Pulsed Drain Current ^(Note 4)	I _{DM}	-16	A
Power Dissipation	P _D	T _a =25°C	1.25
		Derate above 25°C	10
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Typical Thermal resistance	R _{θJA}	100	°C/W
- Junction to Ambient ^(Note 3)			



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.77	-1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4.0A$	-	50	60	m Ω
		$V_{GS}=-4.5V, I_D=-3.3A$	-	58	70	
		$V_{GS}=-2.5V, I_D=-2.0A$	-	80	96	
		$V_{GS}=-1.8V, I_D=-0.5A$	-	140	180	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$	-	-	± 10	μA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-4.0A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	6.9	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	1.9	-	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	602	-	pF
Output Capacitance	C_{oss}		-	70	-	
Reverse Transfer Capacitance	C_{rss}		-	47	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-4.0A,$ $V_{GS}=-4.5V,$ $R_G=3\Omega$ (Note 1,2)	-	8.8	-	ns
Turn-On Rise Time	t_r		-	66	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Turn-Off Fall Time	t_f		-	14	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$	-	-0.79	-1.0	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing



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TYPICAL CHARACTERISTIC CURVES

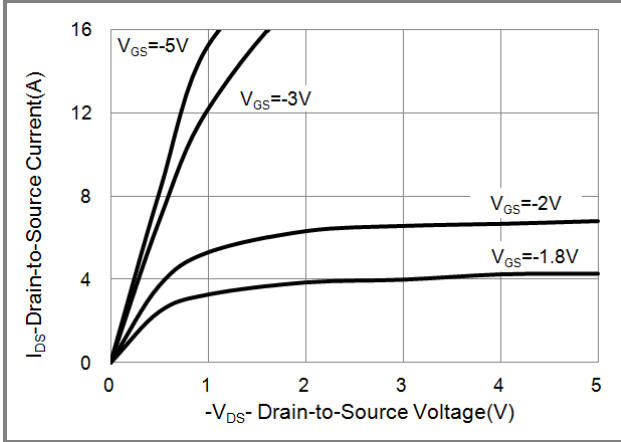


Fig.1 On-Region Characteristics

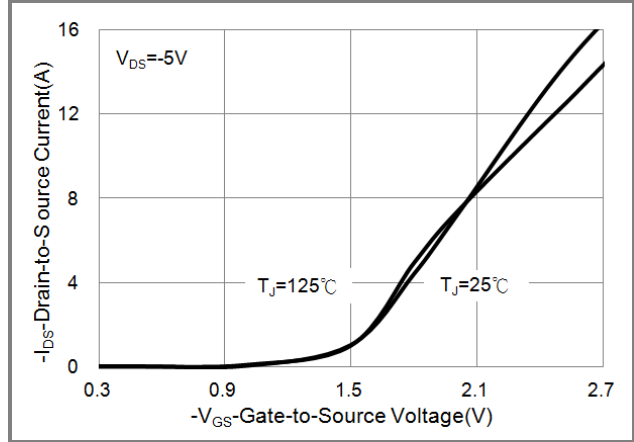


Fig.2 Transfer Characteristics

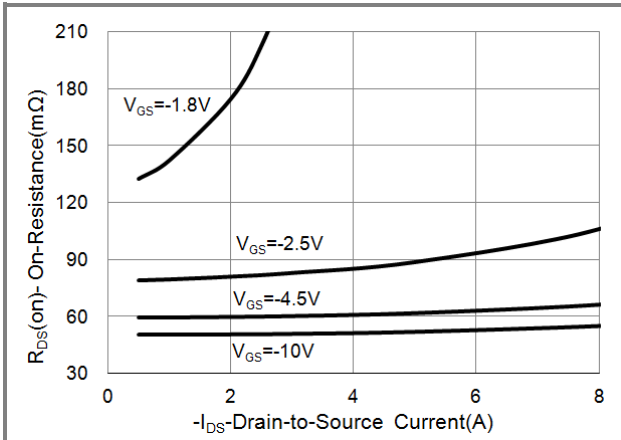


Fig.3 On-Resistance vs. Drain Current

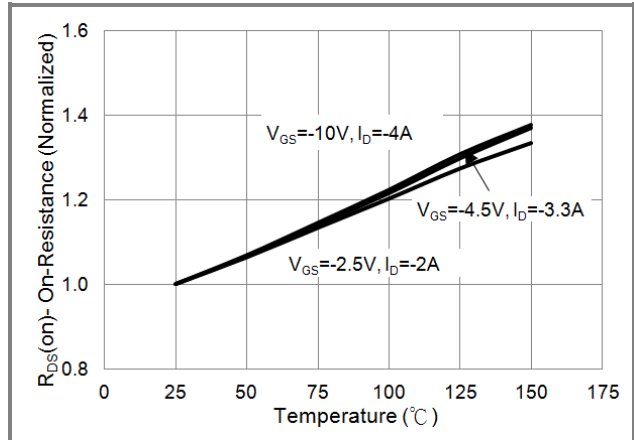


Fig.4 On-Resistance vs. Junction temperature

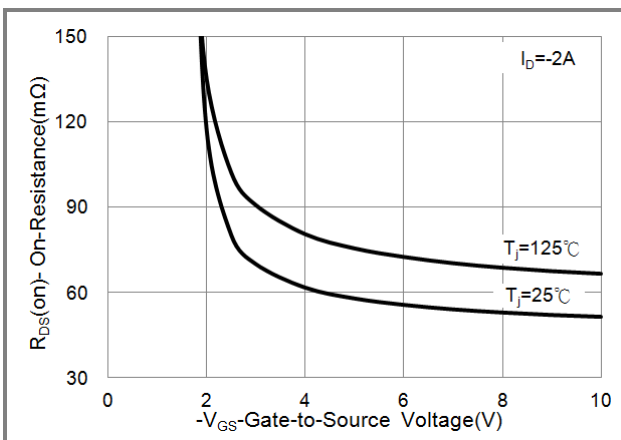


Fig.5 On-Resistance Variation with VGS.

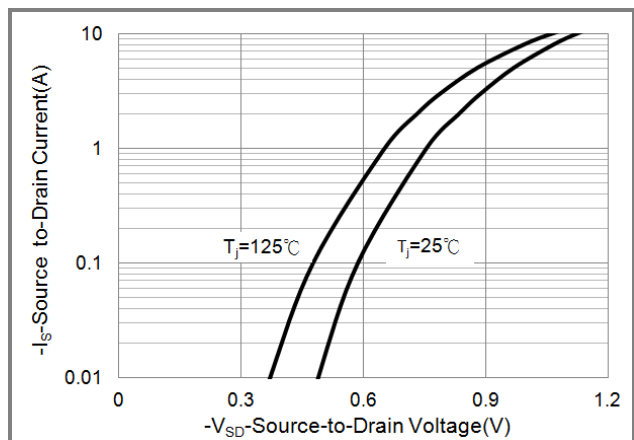


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

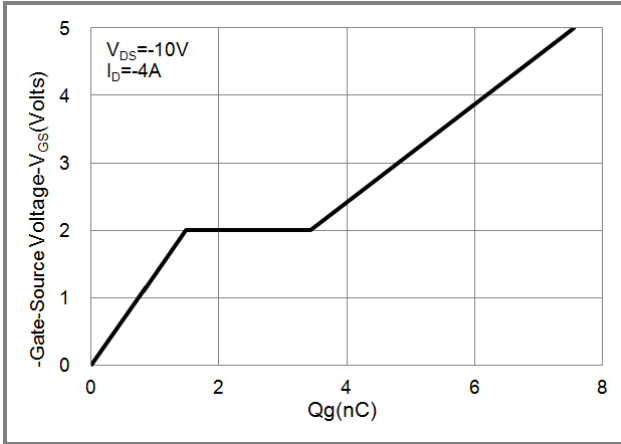


Fig.7 Gate-Charge Characteristics

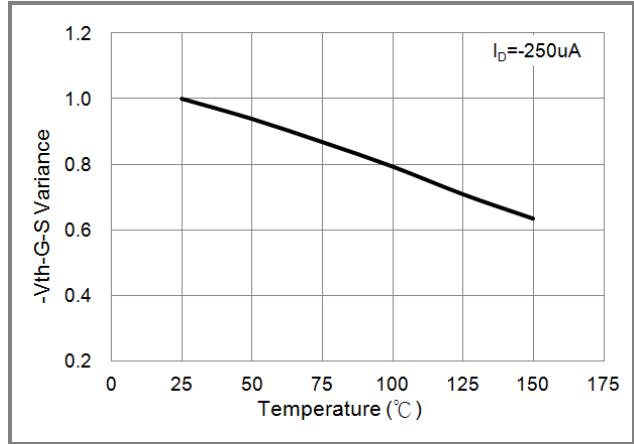


Fig.8 Threshold Voltage Variation with Temperature.

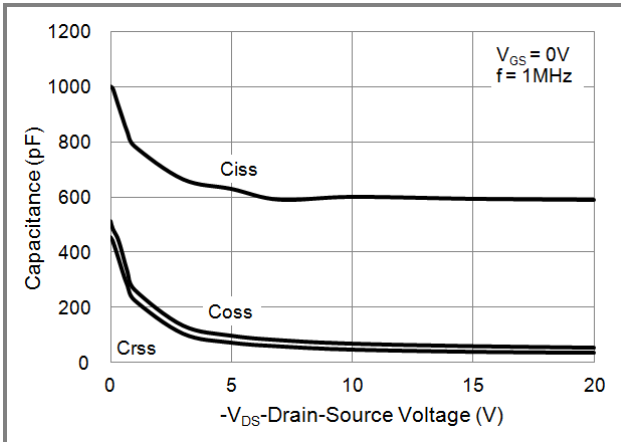


Fig.9 Capacitance vs. Drain-Source Voltage.

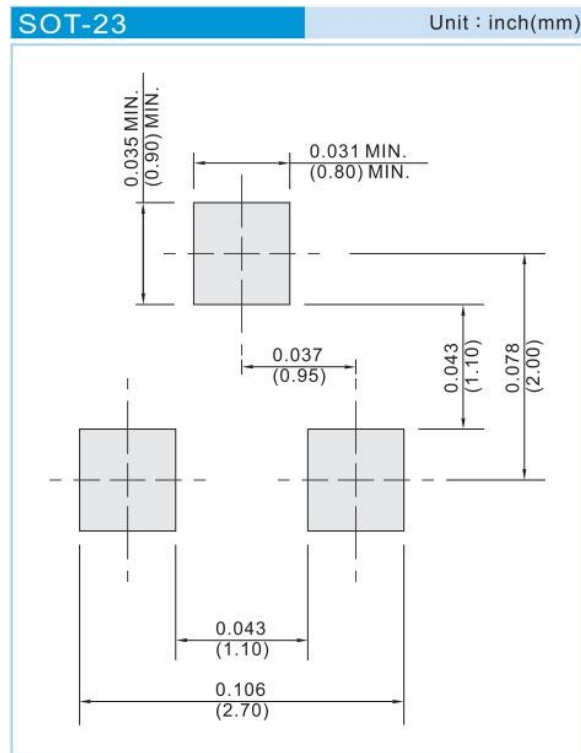


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PART NO PACKING CODE VERSION

PART NO PACKING CODE	Package Type	Packing type	Marking	Version
PJA3419_R1_00001	SOT-23	3K pcs / 7" reel	A19	Halogen free
PJA3419_R2_00001	SOT-23	12K pcs / 13" reel	A19	Halogen free

MOUNTING PAD LAYOUT





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