ΡΛΝ	JIT
	SEMI
	CONDUCTOR

40V N-Channel Enhancement Mode MOSFET

Current

40 A

Voltage

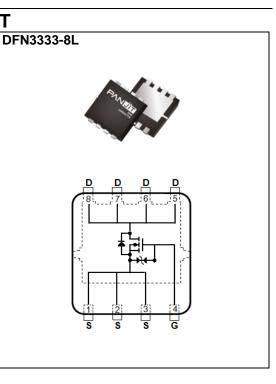
40 V

Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@10A<10.4m\Omega$
- Rds(ON), Vgs@7V, Id@6A<12.7mΩ
- Excellent FOM
- Standard Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETE	R	SYMBOL	LIMIT	UNITS
Prain-Source Voltage		V _{DS}	40	
Gate-Source Voltage		V _{GS}	±20	V
O (Note 2)	Tc=25°C		40	
Continuous Drain Current ^(Note 3)	Tc=100°C	I _D	28	А
Pulsed Drain Current(Note 1)	T _C =25°C	I _{DM}	160	
Power Dissipation	T _C =25°C	2	30	
	Tc=100°C	PD	15	W
Question of Duration Querran (Note 4)	T _A =25°C		11.6	
Continuous Drain Current ^(Note 4) T _A =70 ^o C	T _A =70°C	I _D	9.7	— A
De la Dischartier	T _A =25°C	5	2.5	
Power Dissipation	T _A =70°C	PD	1.8	W
Single Pulse Avalanche Energy ^{(Note}	e 5)	Eas	36	mJ
Operating Junction and Storage Te	emperature Range	TJ,TSTG	-55~175	°C
Thermal Resistance ^(Note 4)	Junction to Case	R _{θJC}	5	°C/W
	Junction to Ambient	R _{θJA}	60	C/W



Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS	
Static		·					
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =50uA	2	2.8	3.5		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =10A	-	8.3	10.4	mΩ	
		V _{GS} =7V, I _D =6A	-	9.8	12.7		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	uA	
Onto Course London of Current		V _{GS} =±20V, V _{DS} =0V	-	-	±10	uA	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±1		
Dynamic ^(Note 6)	-	-	-		-		
Total Gate Charge	Qg		-	9.5	-	nC	
Gate-Source Charge	Qgs	V _{DS} =32V, I _D =10A, V _{GS} =10V	-	4.2	-		
Gate-Drain Charge	Q_gd	V _{GS} =10V	-	2.6	-		
Input Capacitance	Ciss		-	673	-		
Output Capacitance	Coss	V _{DS} =25V, V _{GS} =0V,	-	176	-	pF	
Reverse Transfer Capacitance	Crss	f=1MHz	-	29	-		
Gate resistance	Rg	f=1MHz	-	1.4	-	Ω	
Turn-On Delay Time	td _(on)		-	10	-		
Turn-On Rise Time	tr	V _{DS} =32V, I _D =10A,	-	3	-		
Turn-Off Delay Time	td _(off)	V _{GS} =10V, R _G =3Ω (Note 2)	-	18	-	ns	
Turn-Off Fall Time	tf		-	3	-	1	
Drain-Source Diode							
Diode Forward Current	I _S	T _c =25°C	-	-	40		
Pulsed Diode Forward Current	I _{SM}	1 _C =25 C	-	-	160	A	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.9	1.3	V	
Reverse Recovery Time	Trr	V _{GS} =0V, I _S =20A	-	17	-	ns	
Reverse Recovery Charge	Qrr	dls/dt=100A/us	-	9	-	nC	

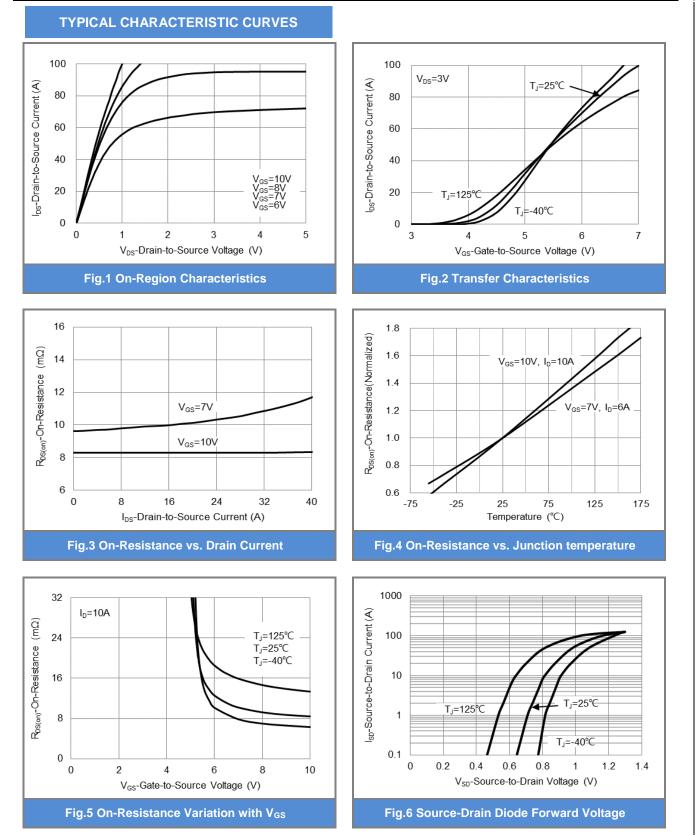
NOTES :

- 1. Pulse width100us, Duty cycle<2%.</td>
- 2. Essentially independent of operating temperature typical characteristics.
- 3. Chip capability with an $R_{\theta JC}=5^{\circ}C/W$.
- 4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 5. The test condition is L=0.5mH, I_{AS} =12A, V_{DD} =30V, V_{GS} =10V, Starting T_J=25°C.
- 6. Guaranteed by design, not subject to production testing.

February 18,2023

PJQ4548VP-AU-REV.01





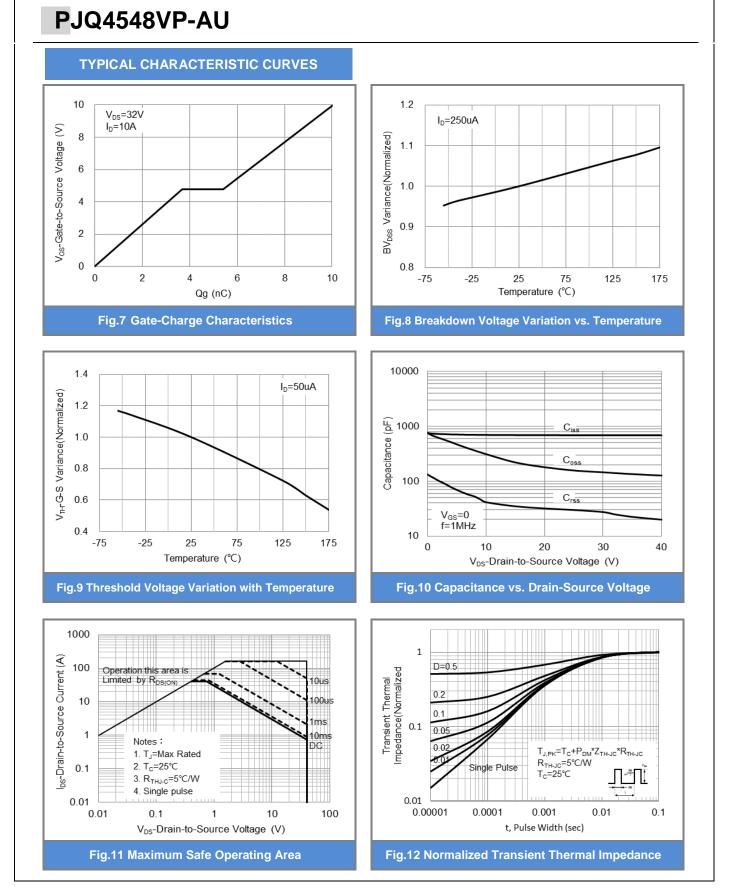
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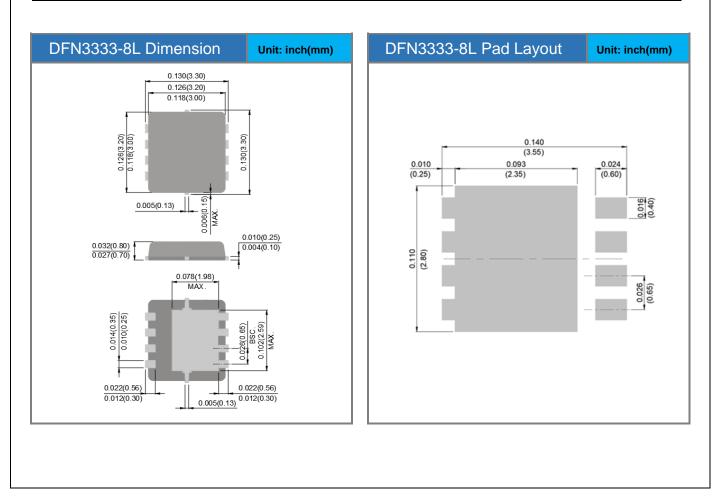




Product and Packing Information

Part No.	Package Type	ckage Type Packing Type	
PJQ4548VP-AU	DFN3333-8L	5K pcs / 13" reel	548V

Packaging Information & Mounting Pad Layout





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