

PS2403-D63

Low Capacitance ESD Protection

Voltage

3.3 V

Features

- IEC61000-4-2(ESD) : ± 24 kV Air, ± 20 kV Contact
- IEC61000-4-4(EFT) : 40A(5/50ns)
- IEC61000-4-5(Lightning) : 7A (8/20uS)
- Ultra-Low Capacitance : 0.42pF
- Low leakage current, maximum of 0.5uA at rated voltage
- Low clamping voltage
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

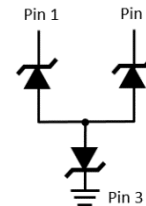
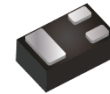
Mechanical Data

- Case : DFN1006T-3L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0007 grams

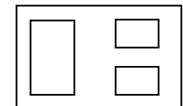
Applications

- USB 2.0 and 3.0/3.1/3.2
- Notebooks
- SATA ports

DFN1006T-3L



Top view



bottom view

Part Marking	Parameter
1bx	1b = Marking Code
	x = Tracking Code

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
ESD IEC61000-4-2(Air)	V _{ESD}	± 24	kV
ESD IEC61000-4-2(Contact)		± 20	
Operating Junction Temperature Range	T _J	-55~125	°C
Storage Temperature Range	T _{STG}	-55~150	°C

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Electrical Characteristics (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage (Note 1)	V _{RWM}	any I/O Pin to GND	-	-	3.3	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA, any I/O Pin to GND	5.5	-	11	V
Reverse Leakage Current	I _R	V _{RWM} = 3.3V, any I/O Pin to GND	-	0.4	0.5	uA
Surge Clamping Voltage (8/20 us)	V _{CL}	I _{PP} = 5A, any I/O Pin to GND	-	3	4	V
Clamping Voltage TLP (tperiod=100ns, tr=1 ns)(Note 2)	V _{CL}	I _{TLP} = 16A, any I/O Pin to GND	-	4.5	-	V
Off State Junction Capacitance (Note 3)	C _J	V _R = 1.65V, f = 1MHz, any I/O Pin to GND	-	0.42	0.47	pF

NOTES :

1. Mounted on a FR4 PCB, Single-sided copper, mini pad.
2. A transient suppressor is selected according to the working peak reverse voltage(V_{RWM}), which should be equal to or greater than the DC or continuous peak operation voltage level.
3. Testing using Transmission Line Pulse (TLP) conditions : Z₀ = 50 Ω, t_P = 100 ns.
4. This parameter is guaranteed by design.
5. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid the ESD protection device maintain in snap-back state after exceeding breakdown voltage.

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TYPICAL CHARACTERISTIC CURVES

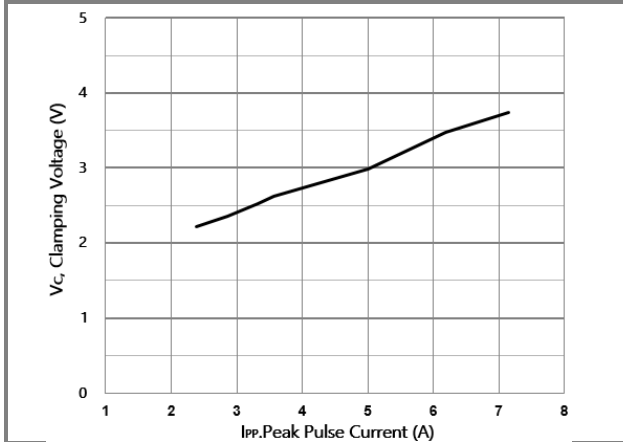


Fig.1 Typical Peak Clamping Voltage

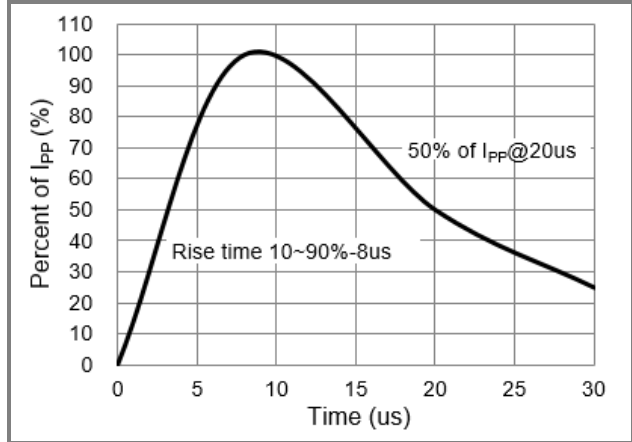


Fig.2 Pulse Waveform

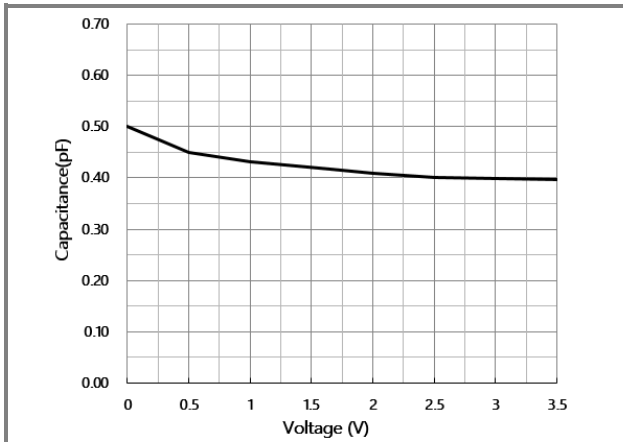


Fig.3 Typical Junction Capacitance

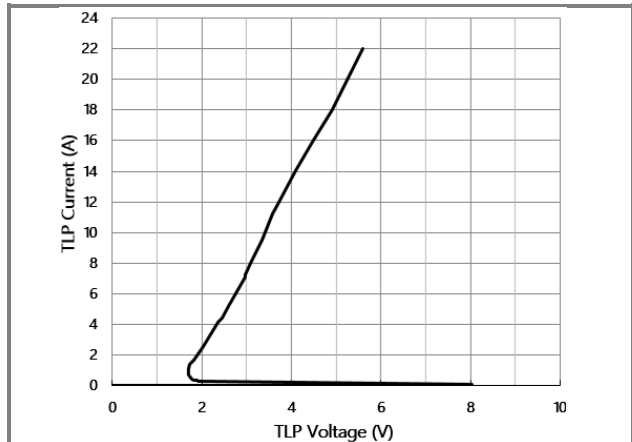


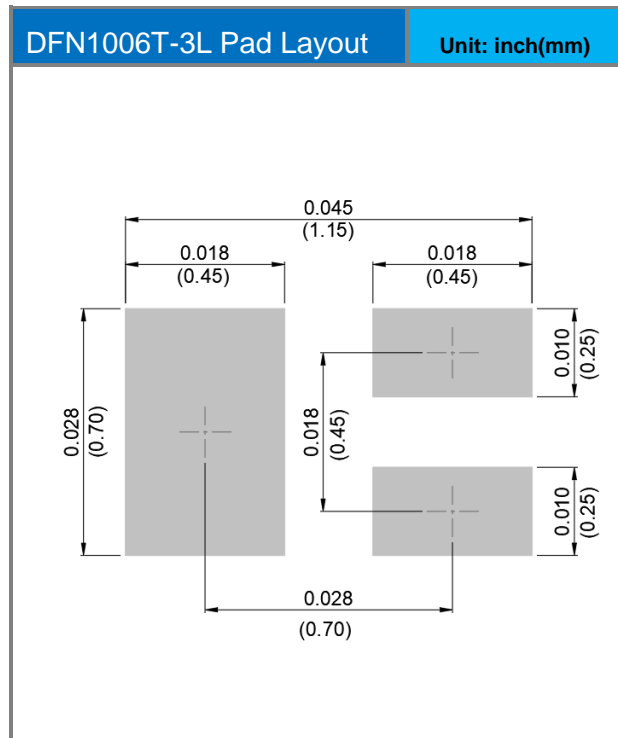
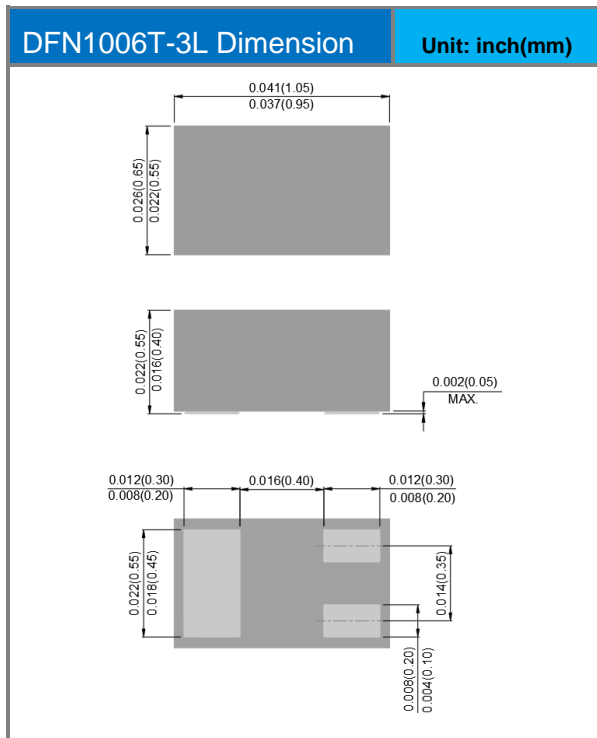
Fig.4 TLP Measurement

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Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PS2403-D63	DFN1006T-3L	10K pcs / 7" reel	1b

Packaging Information & Mounting Pad Layout



PS2403-D63

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