

**100V N-Channel Enhancement Mode MOSFET**

<b>Voltage</b>	<b>100 V</b>	<b>R<sub>DS(ON)</sub></b>	<b>4.4 mΩ</b>
<b>Current</b>	<b>122 A</b>	<b>Q<sub>G</sub> (TYP)</b>	<b>40.5 nC</b>

**Feature**

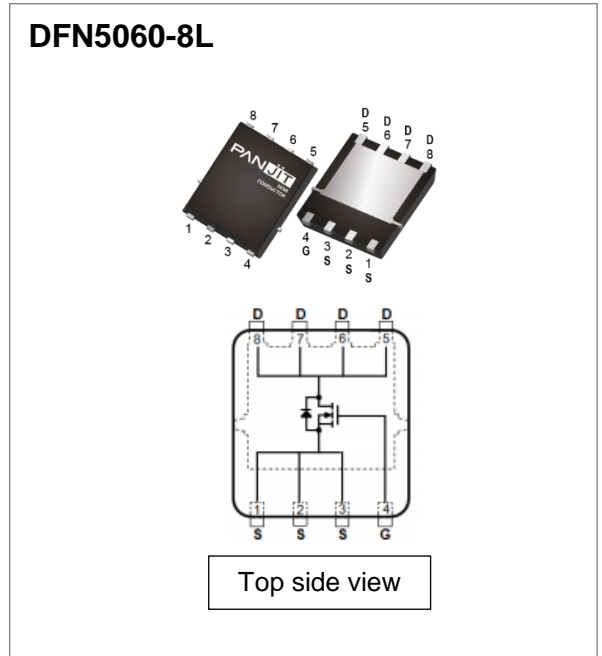
- R<sub>DS(ON)</sub> < 4.4 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 50 A
- R<sub>DS(ON)</sub> < 6.5 mΩ at V<sub>GS</sub> = 6 V, I<sub>D</sub> = 25 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

**Mechanical Data**

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.08 grams

**Application**

- SR solutions of PD Charger, Brick Power, 48V DC/DC converter



**Absolute Maximum Ratings** (T<sub>A</sub> = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	100	V
Gate-Source Voltage		V <sub>GS</sub>	±20	
Continuous Drain Current (Note 3)	T <sub>C</sub> =25 °C	I <sub>D</sub>	122	A
	T <sub>C</sub> =100 °C		77	
Pulsed Drain Current		I <sub>DM</sub>	488	A
Single Pulse Avalanche Current (Note 5)		I <sub>AS</sub>	50	A
Single Pulse Avalanche Energy (Note 5)		E <sub>AS</sub>	318	mJ
Power Dissipation	T <sub>C</sub> =25 °C	P <sub>D</sub>	125	W
	T <sub>C</sub> =100 °C		50	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55~150	°C

**Thermal Characteristics**

PARAMETER		SYMBOL	MAXIMUM	UNITS
Thermal Resistance	Junction-to-Case (Bottom)	R <sub>θJC</sub>	1.0	°C/W
	Junction-to-Ambient (Note 4)	R <sub>θJA</sub>	50	°C/W

## Electrical Characteristics (T<sub>A</sub> = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0 V, I <sub>D</sub> =250 μA	100	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =270 μA	1.8	2.8	3.8	
Drain-Source On-State Resistance (Note 1)	R <sub>DS(on)</sub>	V <sub>GS</sub> =10 V, I <sub>D</sub> =50 A	-	3.8	4.4	mΩ
		V <sub>GS</sub> =6 V, I <sub>D</sub> =25 A	-	5.0	6.5	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100 V, V <sub>GS</sub> =0 V	-	-	1	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20 V, V <sub>DS</sub> =0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g <sub>fs</sub>	V <sub>DS</sub> =10 V, I <sub>D</sub> =50 A	-	105	-	S
<b>Dynamic</b> (Note 6)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50 V, I <sub>D</sub> =50 A, V <sub>GS</sub> =10 V	-	40.5	53	nC
Gate-Source Charge	Q <sub>gs</sub>		-	15	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	6	-	
Gate Plateau Voltage	V <sub>plateau</sub>		-	5	-	V
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50 V, V <sub>GS</sub> =0 V, f=250 kHz	-	3010	3910	pF
Output Capacitance	C <sub>oss</sub>		-	1080	1400	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	14	-	
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> =50 V, V <sub>GS</sub> =0 V	-	85	110	nC
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50 V, I <sub>D</sub> =50 A, V <sub>GS</sub> =10 V, R <sub>G</sub> =6.0 Ω (Note 2)	-	11	-	ns
Rise Time	t <sub>r</sub>		-	6	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	22	-	
Fall Time	t <sub>f</sub>		-	8	-	
Gate Resistance	R <sub>g</sub>	f =1.0 MHz	-	0.8	1.6	Ω
<b>Drain-Source Diode</b>						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =50 A, V <sub>GS</sub> =0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =50 A, V <sub>DD</sub> =50 V di/dt=100 A/μs	-	85	-	nC
Reverse Recovery Time	T <sub>rr</sub>		-	56	-	ns

### NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
5. E<sub>AS</sub> is calculated based on the condition of L = 1.0 mH, I<sub>AS</sub> = 25.2 A, V<sub>DD</sub> = 50 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 50 A in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

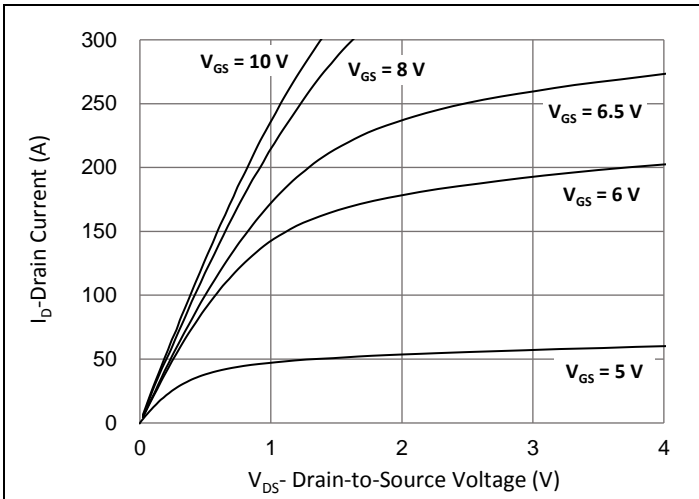


Fig.1 Output Characteristics

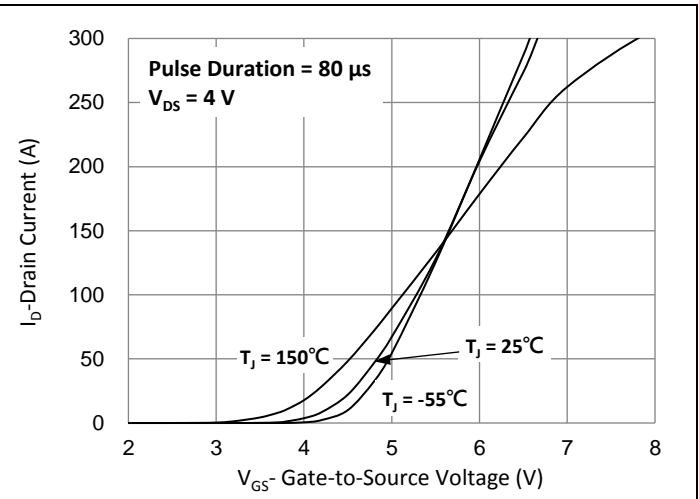


Fig.2 Transfer Characteristics

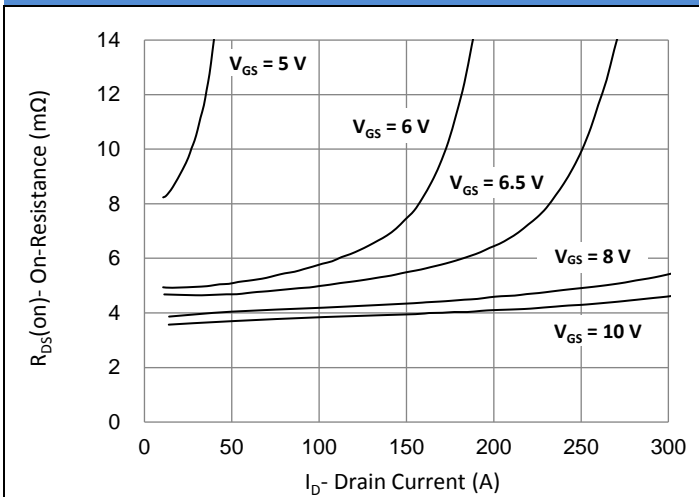


Fig.3 On-Resistance vs. Drain Current

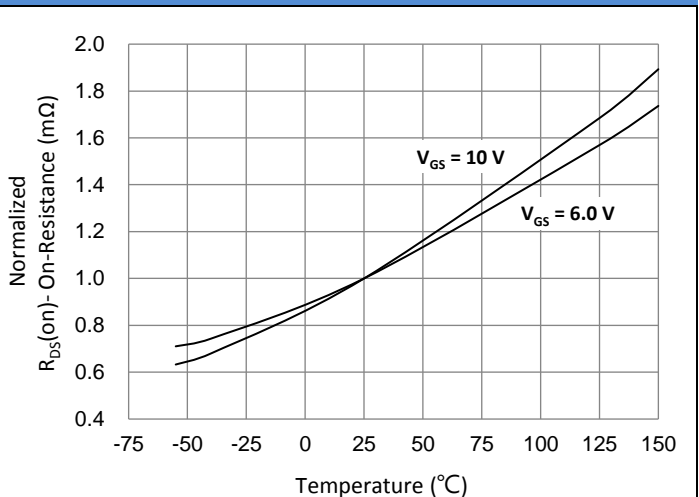


Fig.4 On-Resistance vs. Junction temperature

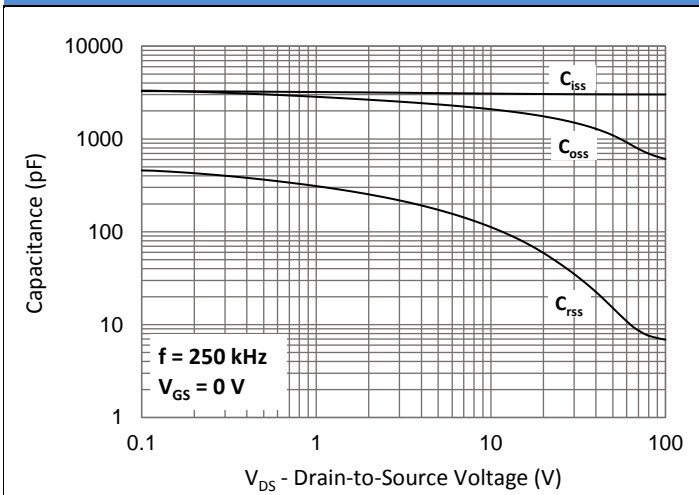


Fig.5 Capacitance vs. Drain-Source Voltage

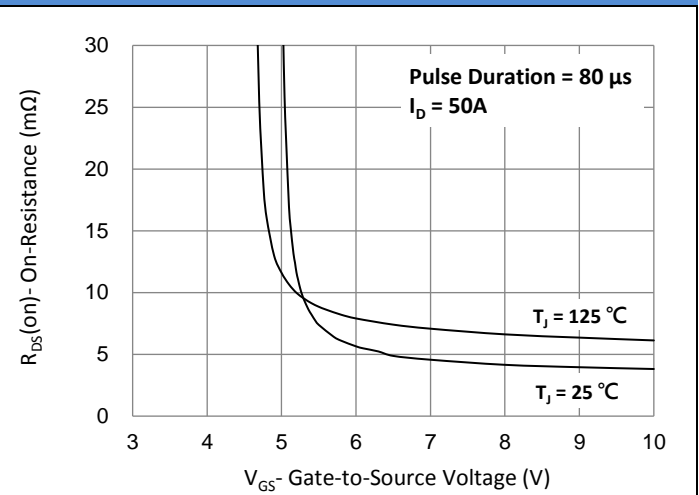


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

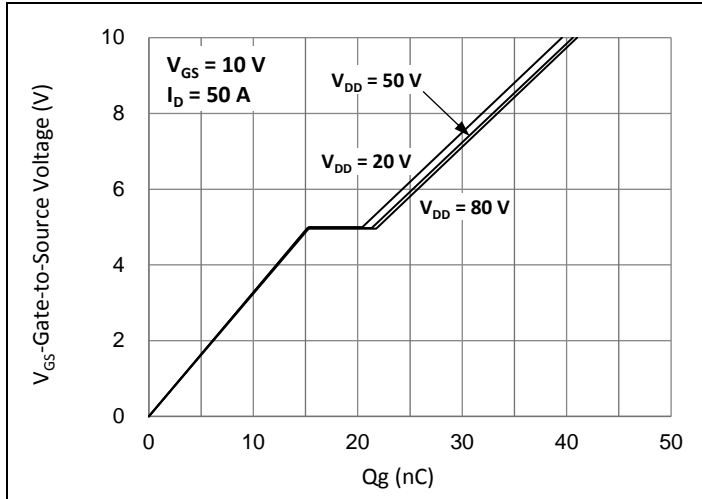


Fig.7 Gate-Charge Characteristics

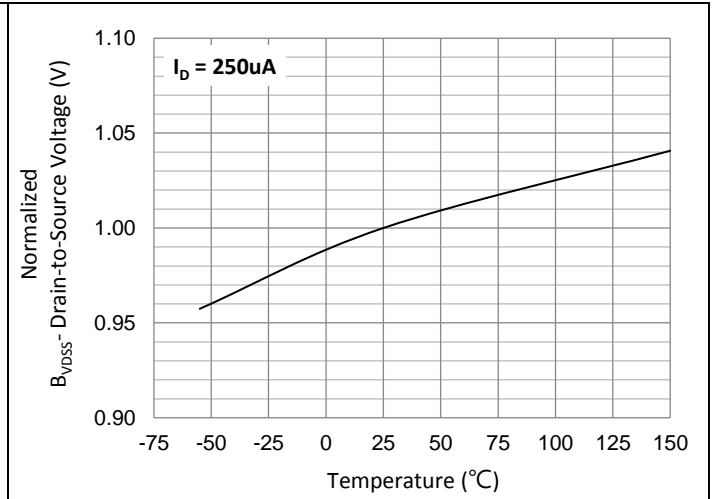


Fig.8 Breakdown Voltage Variation vs. Temperature

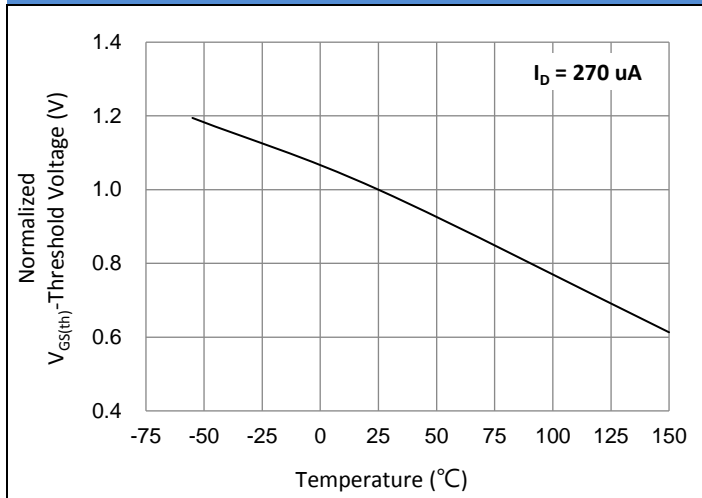


Fig.9 Threshold Voltage Variation with Temperature

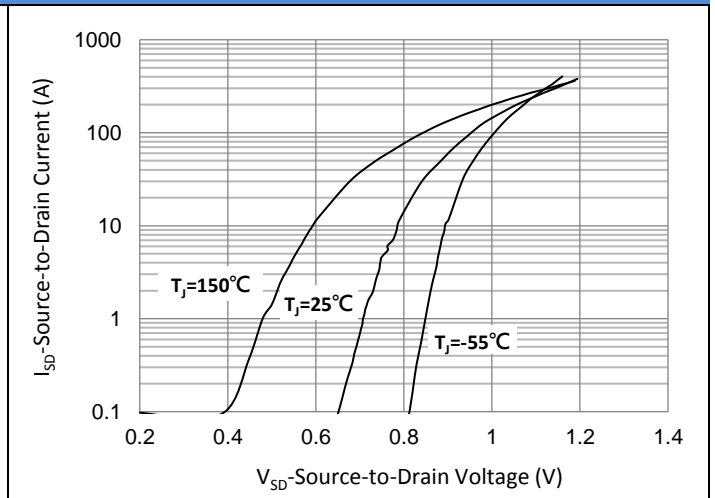


Fig.10 Source-Drain Diode Forward Voltage

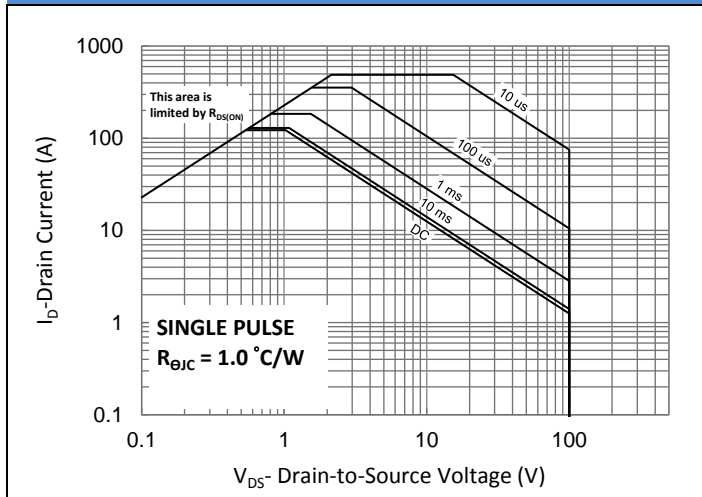


Fig.11 Maximum Safe Operating Area

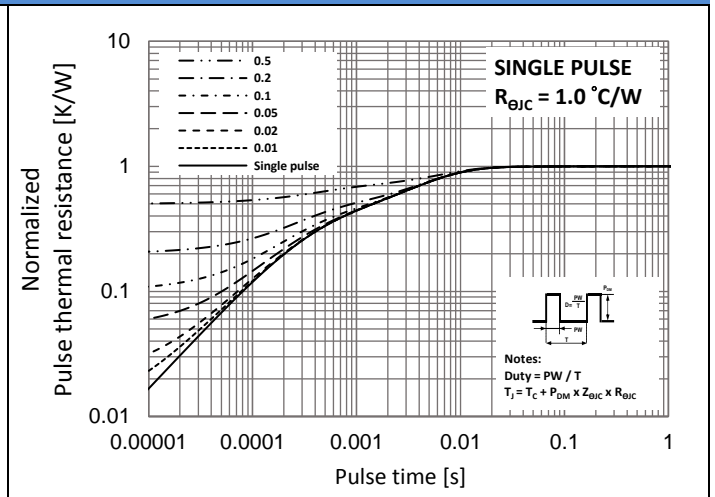


Fig.12 Normalized Transient Thermal Impedance

TYPICAL CHARACTERISTIC CURVES

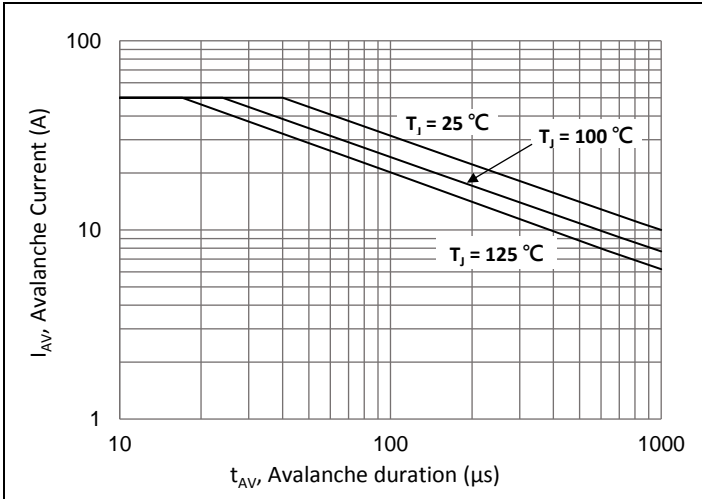


Fig.13 Avalanche Characteristics

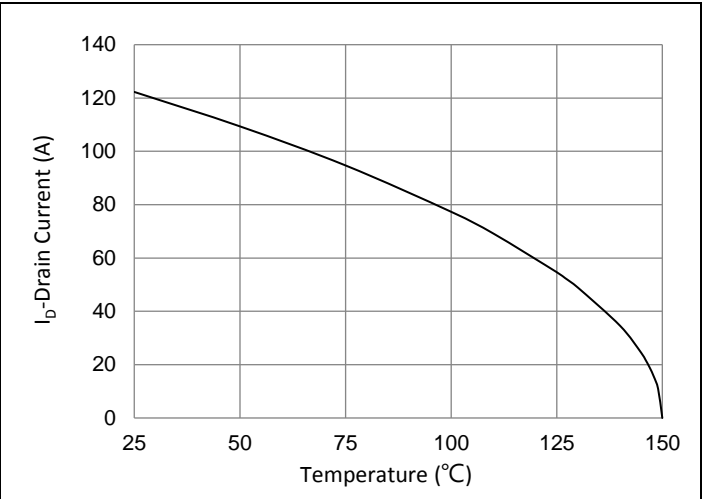
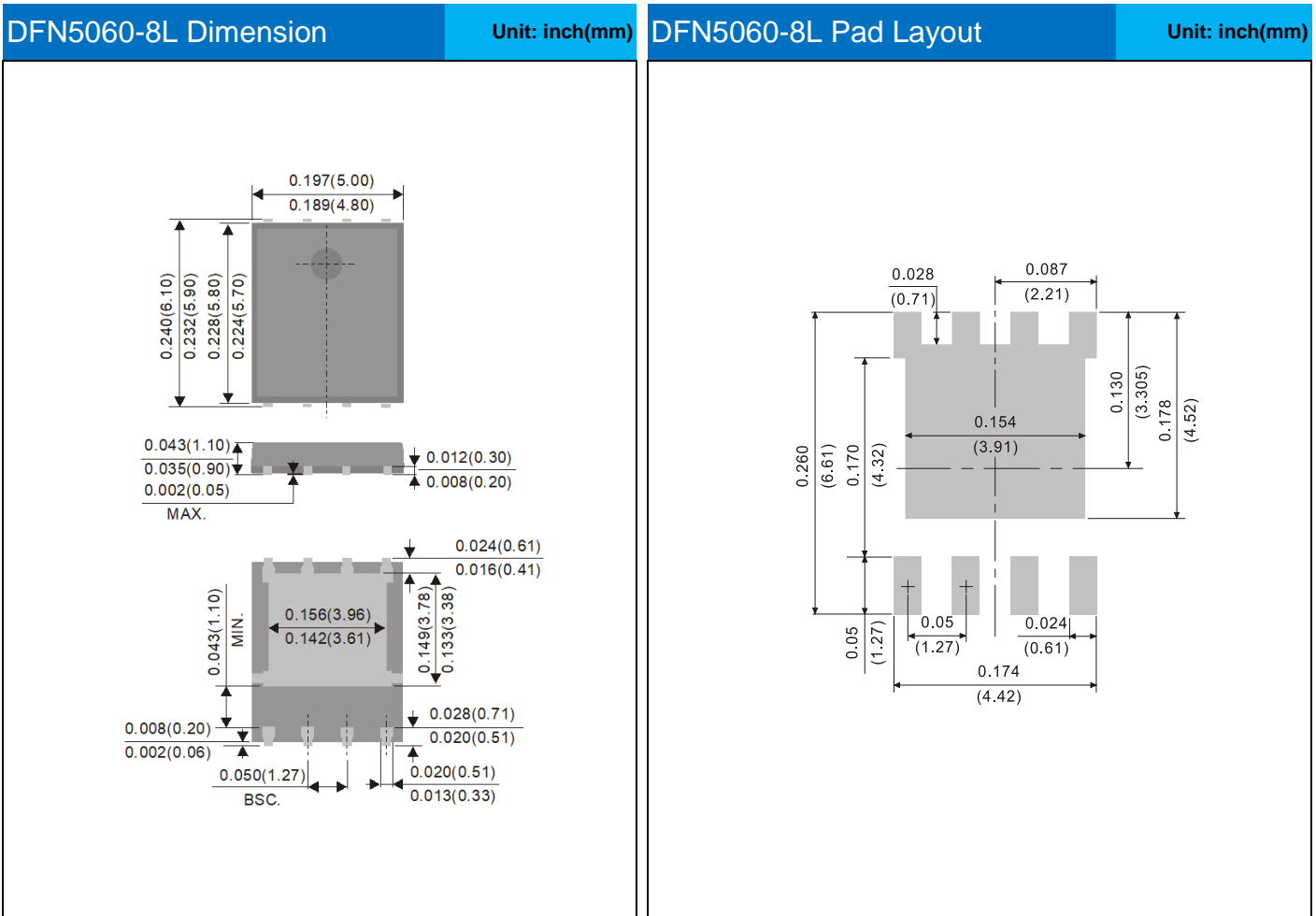


Fig.14 Drain Current vs. Case Temperature

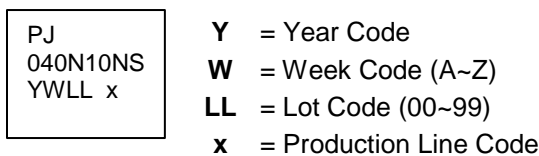
**Product and Packing Information**

Part No.	Package Type	Packing Type	Marking
PSMQC040N10NS2	DFN5060-8L	3000pcs / 13" reel	040N10NS

**Packaging Information & Mounting Pad Layout**



**Marking Diagram**



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[1.5SMCJ75CA\\_R1\\_00001](#) [1N4007\\_AY\\_10001](#) [1N4007G\\_AY\\_00101](#) [1N4007G\\_AY\\_10001](#) [1N4148-34\\_R2\\_10001](#) [1N4148-35\\_AX\\_10001](#)  
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[1N4148W\\_R1\\_000Z8](#) [1N4148W\\_R1\\_00101](#) [1N4148W\\_R2\\_00001](#) [1N4148WS](#) [1N4148WS-AU\\_R1\\_00001](#) [1N4148WS-AU\\_R1\\_000A1](#)  
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